Sipex Corporation

SIGNAL PROCESSING EXCELLENCE

SP9560

12-BIT 10 MHz SAMPLING A/D CONVERTER

FEATURES

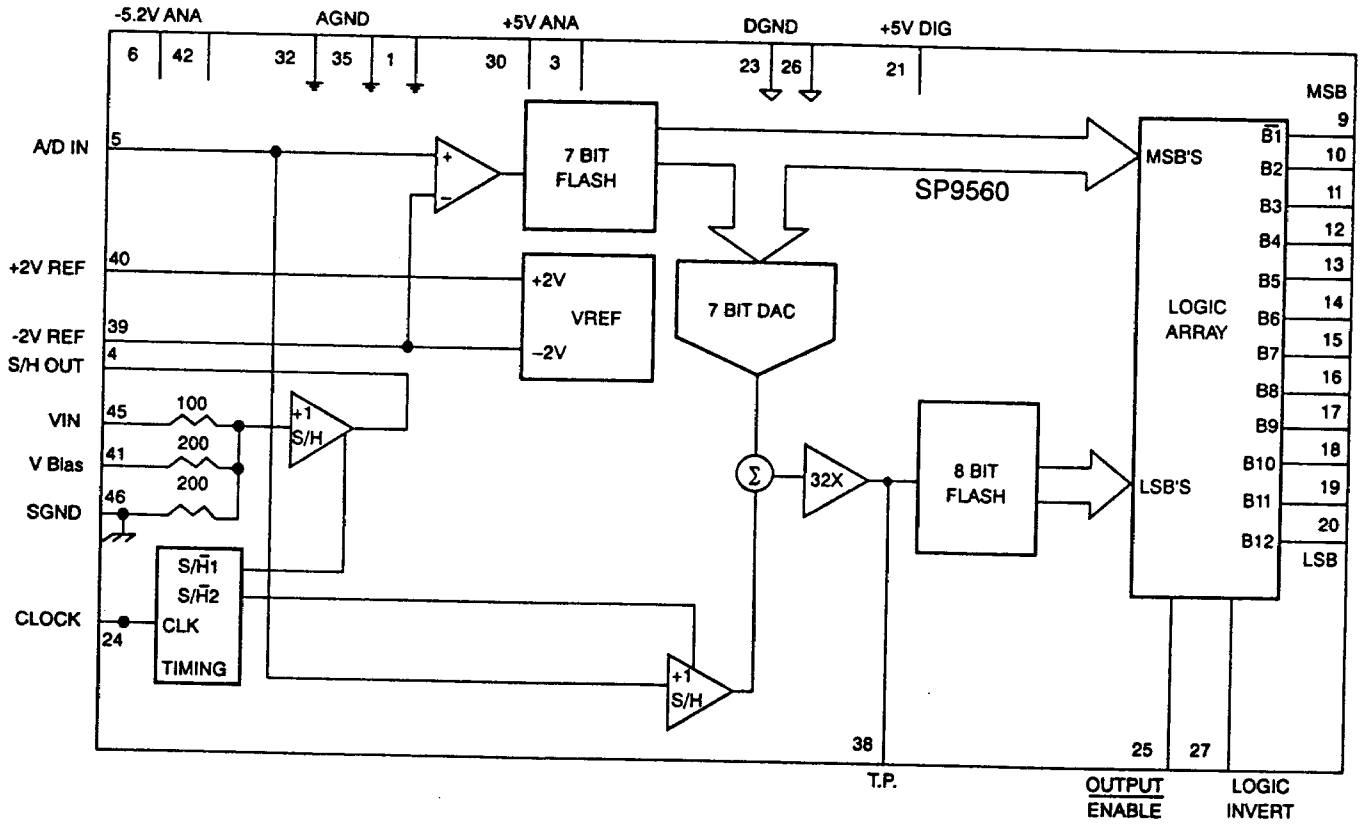
- 10 MHz Sampling Rate
- Complete with SHA and Reference
- High Signal/Noise Ratio: 69 dB
- High SINAD Ratio: 68 dB
- Low Harmonic Distortion: -72 dB
- Low Power Consumption: 3.6W
- 0°C to +70°C and -55°C to +125°C

PRELIMINARY INFORMATION

DESCRIPTION

The SP9560 is a 10 MHz sample rate, 12-Bit Analog-to-Digital converter which includes all components necessary to digitize an incoming analog signal. The SP9560 includes a 12-Bit A/D Converter, a sample and hold amplifier, an on-board reference and all of the control logic necessary for complete functionality. The SP9560 has very low power consumption of 3.6 Watts, can digitize signals up to 10 MHz, and has excellent Signal to Noise + Distortion performance of 68 dB with total harmonic distortion of -72 dB. The SP9560 uses two's complement or inverted two's complement coding and is designed to function over the military temperature range of -55°C to +125°C. All this is packaged in a 46-pin dual in-line package, and will be available with MIL-STD-883C screening.

FUNCTIONAL DIAGRAM



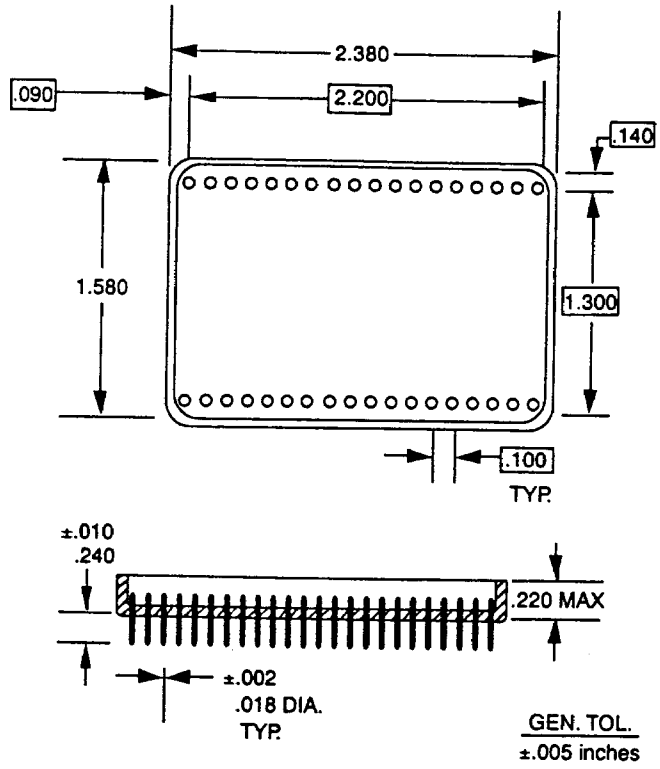
SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (Typical @ 25°C and Nominal Supply Voltages unless otherwise noted)					
PARAMETERS	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG INPUTS					
Voltage Range			±1.0V		Volts
DIGITAL INPUTS					
Logic Levels	Logic 1	2.4			Volts
	Logic 0			0.5	Volts
Logic Loading			1		TTL Load
STATIC PERFORMANCE					
Differential Linearity			±0.5		LSB
Integral Linearity			±0.5		LSB
No Missing Codes					Bits
Gain Error			±0.75		%FSR
Offset Error			±0.75		%FSR
DYNAMIC PERFORMANCE					
Signal to Noise Ratio	(10 MHz clock)				
Fin=100 kHz			69		dB
Fin=4.99 MHz			69		dB
Signal to Noise + Distortion	(10 MHz clock)				
Fin=100 kHz			68		dB
Fin=4.99 MHz			64		dB
Total Harmonic Distortion	(10 MHz clock)				
Fin=100 kHz	-0.5 dB		-72		dB
Fin=4.99 kHz	-0.5 dB		-68		dB
Dynamic Differential Linearity	(10 MHz clock)		±0.5		LSB
A.C. PARAMETERS					
Throughput			10		MHz
S/H Aperture Delay			5		nsec
S/H Aperture Time			1		nsec
S/H Aperture Jitter			10		psec RMS
DIGITAL OUTPUTS					
Coding					Two's Complement
					Inverted 2's Comp
Output Drive			2		TTL Loads
POWER SUPPLY REQUIREMENTS					
PSRR			±0.01		%/%
+5V Digital			193		mA
+5V Analog			350		mA
-5.2V Analog			280		mA
Dissipation			3.6		W

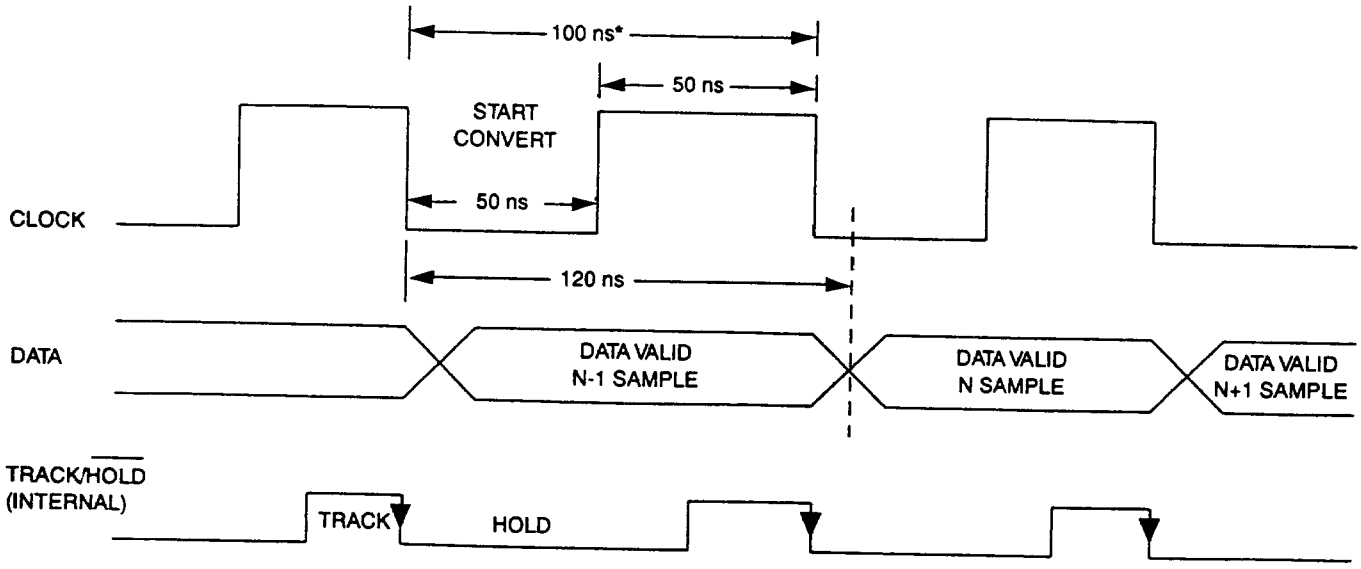
PIN ASSIGNMENTS

PIN	FUNCTION
1	AGND
2	N.C.
3	+5V Analog
4	S/H Out
5	A/D In
6	-5V Analog
7	N.C.
8	N.C.
9	Bit 1 $\overline{D11}$ (MSB)
10	Bit 2 D10
11	Bit 3 D9
12	Bit 4 D8
13	Bit 5 D7
14	Bit 6 D6
15	Bit 7 D5
16	Bit 8 D4
17	Bit 9 D3
18	Bit 10 D2
19	Bit 11 D1
20	Bit 12 D0
21	+5V Digital
22	N.C.
23	DGND
24	Clock
25	Output $\overline{\text{Enable}}$
26	DGND
27	Logic Invert
28	N.C.
29	N.C.
30	+5 VA
31	N.C.
32	AGND
33	N.C.
34	N.C.
35	AGND
36	N.C.
37	N.C.
38	Test Point
39	-2V Ref
40	+2V Ref
41	V Bias
42	-5.2V Analog
43	N.C.
44	N.C.
45	Vin
46	SGND

PACKAGE OUTLINE



TIMING DIAGRAM



*DUTY CYCLE MUST BE 50%

Sipex

SIGNAL PROCESSING EXCELLENCE

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