KM41C1001A CMOS DRAM

T-46-23-15

1M x 1 Bit Dynamic RAM with Nibble Mode

2

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C1001A- 7	70ns	20ns	130ns
KM41C1001A- 8	80ns	20ns	150ns
KM41C1001A-10	100ns	25ns	180ns

- **Nibble Mode Operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and output**
- **Common I/O using early write**
- **Single +5V ± 10% power supply**
- **512 cycle/8ms refresh**
- **256K x 4 fast test mode**
- **JEDEC standard pinout available in Plastic DIP, SOJ, ZIP packages.**

GENERAL DESCRIPTION

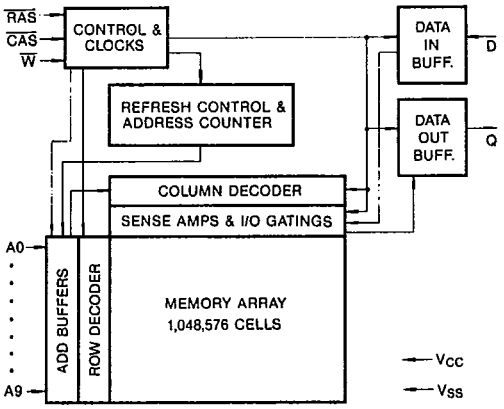
The Samsung KM41C1001A is a CMOS high speed 1,048,576 x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C1001A features Nibble Mode operation which allows high speed random access of up to 4-bits of data.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

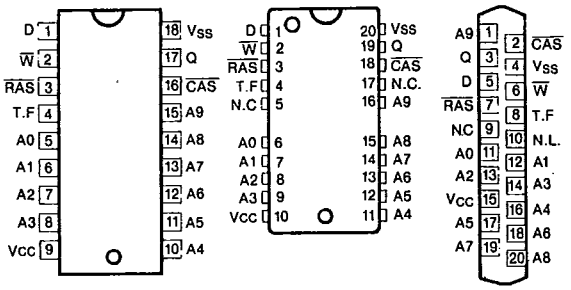
The KM41C1001A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

- **KM41C1001AP**
- **KM41C1001AJ**
- **KM41C1001AZ**



Pin Name	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D	Data In
Q	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
T.F	Test Function
N.C	No Connection
N.L	No Lead

T-46-23-15

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	0.6	W
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC} = min.)	KM41C1001A-7 KM41C1001A-8 KM41C1001A-10	I_{CC1}	—	85 75 65	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling @t_{RC} = min.)	KM41C1001A-7 KM41C1001A-8 KM41C1001A-10	I_{CC3}	—	85 75 65	mA
NIBBLE MODE CURRENT* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{NC} = min.)	KM41C1001A-7 KM41C1001A-8 KM41C1001A-10	I_{CC4}	—	70 60 50	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC} = min.)	KM41C1001A-7 KM41C1001A-8 KM41C1001A-10	I_{CC6}	—	85 75 65	mA
INPUT LEAKAGE CURRENT (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V		I_{OL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL (I_{OH} = −5mA)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

T-46-23-15

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance (A_0-A_9)	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM41C1001A-7		KM41C1001A-8		KM41C1001A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	30	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	20	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9

T-46-23-15

STANDARD OPERATION (Continued)

Parameter	Symbol	KM41C1001A-7		KM41C1001A-8		KM41C1001A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		20		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		65		75		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	20		20		25		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		80		100		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	8

NIBBLE MODE

Nibble Mode Cycle Time	t_{NC}	40		40		45		ns	
Nibble Mode Read-Write Cycle Time	t_{NRWC}	65		65		70		ns	
Nibble Mode Access Time	t_{NCAC}		20		20		25	ns	
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCAS}	20		20		25		ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	10		10		10		ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{NRSH}	20		20		25		ns	
Nibble Mode $\overline{CAS}$ to $\overline{W}$ Delay Time	t_{NCWD}	20		20		25		ns	
Nibble Mode $\overline{W}$ to $\overline{RAS}$ Lead Time	t_{NRWL}	20		20		25		ns	
Nibble Mode $\overline{W}$ to $\overline{CAS}$ Lead Time	t_{NCWL}	20		20		25		ns	

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

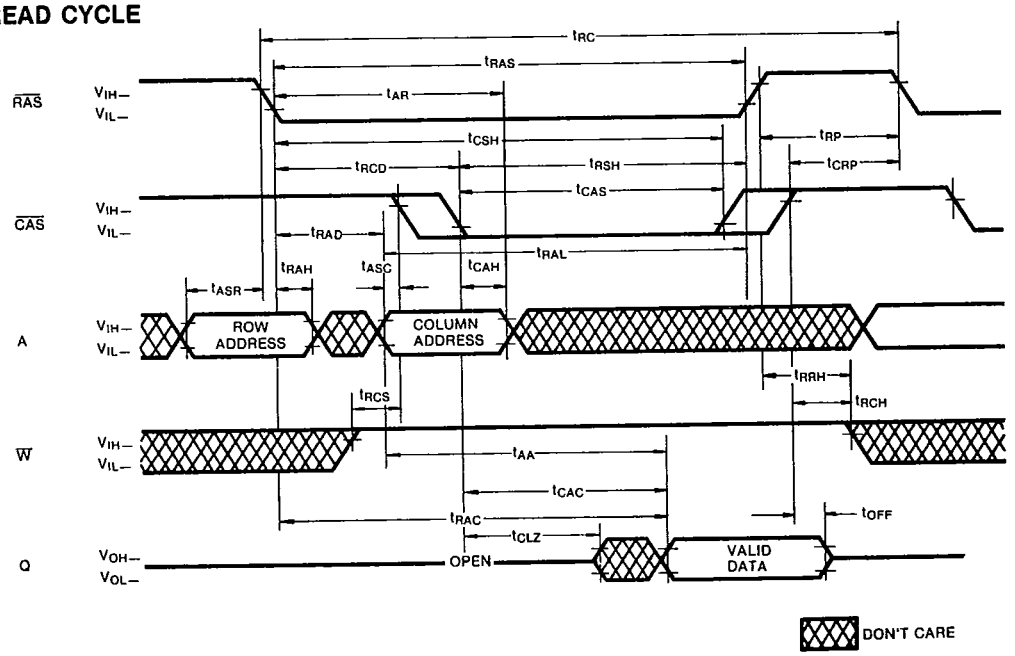
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		25		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	35		40		50		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Normal operation requires the "T.F" pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
13. When the "T.F" pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung for specific operational details of the "test function."

TIMING DIAGRAMS

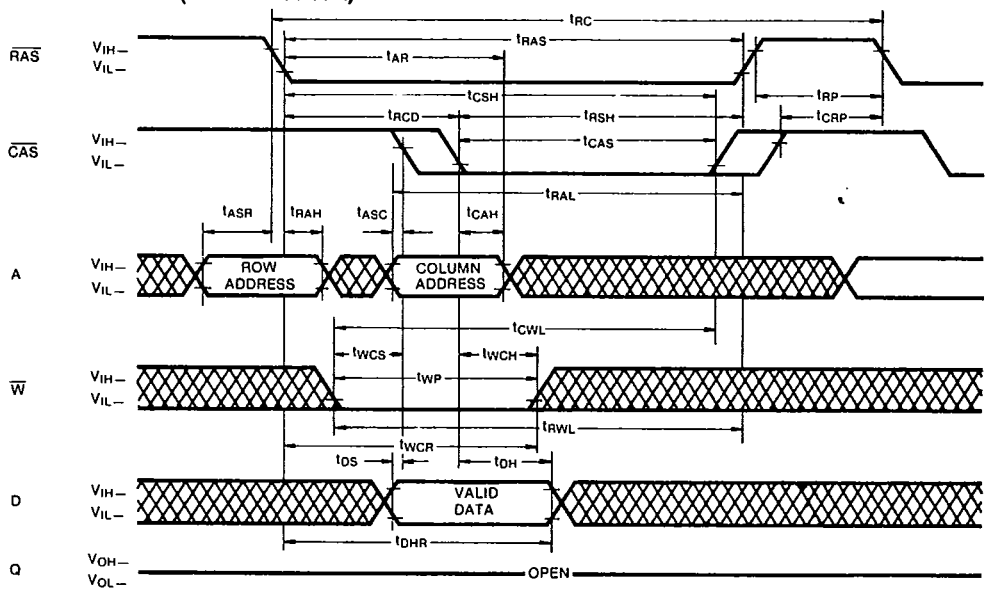
READ CYCLE



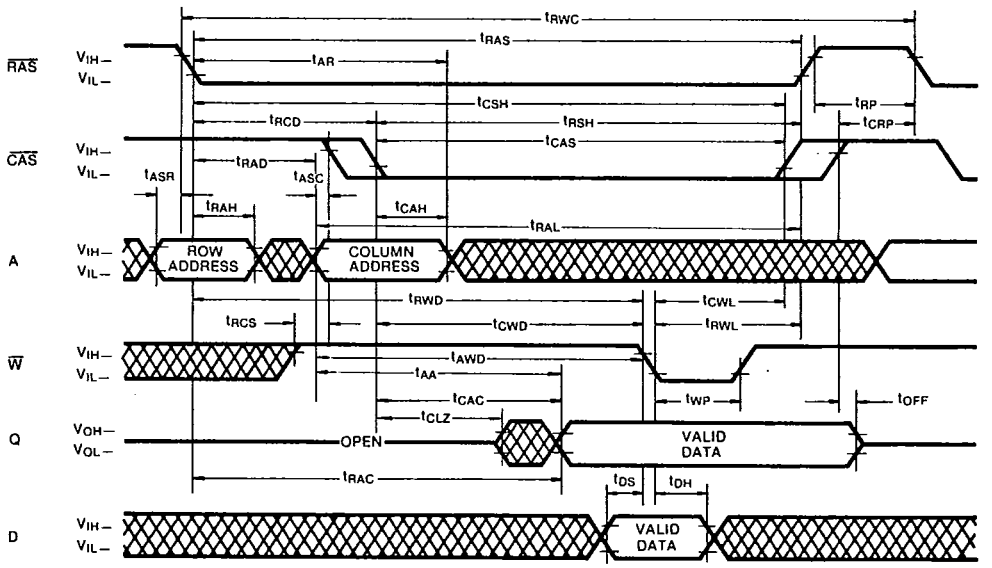
T-46-23-15

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



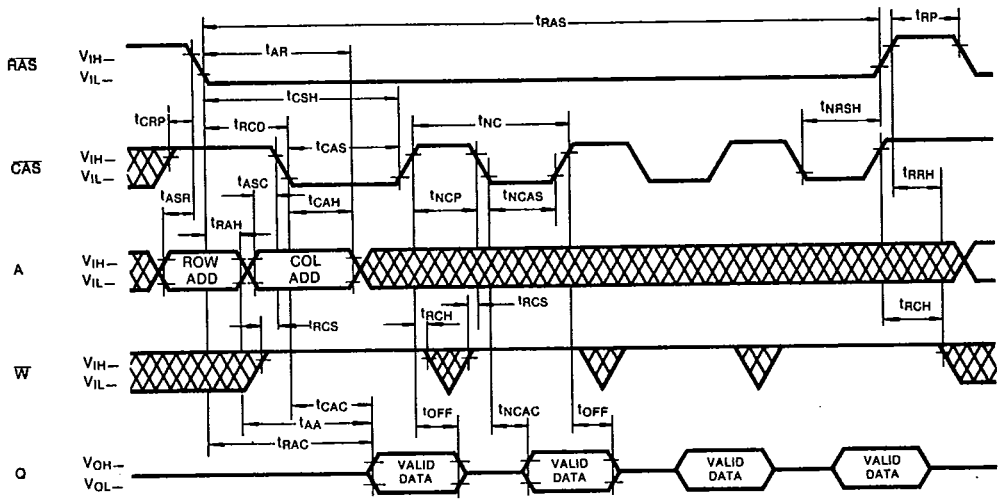
READ-WRITE/READ-MODIFY-WRITE CYCLE



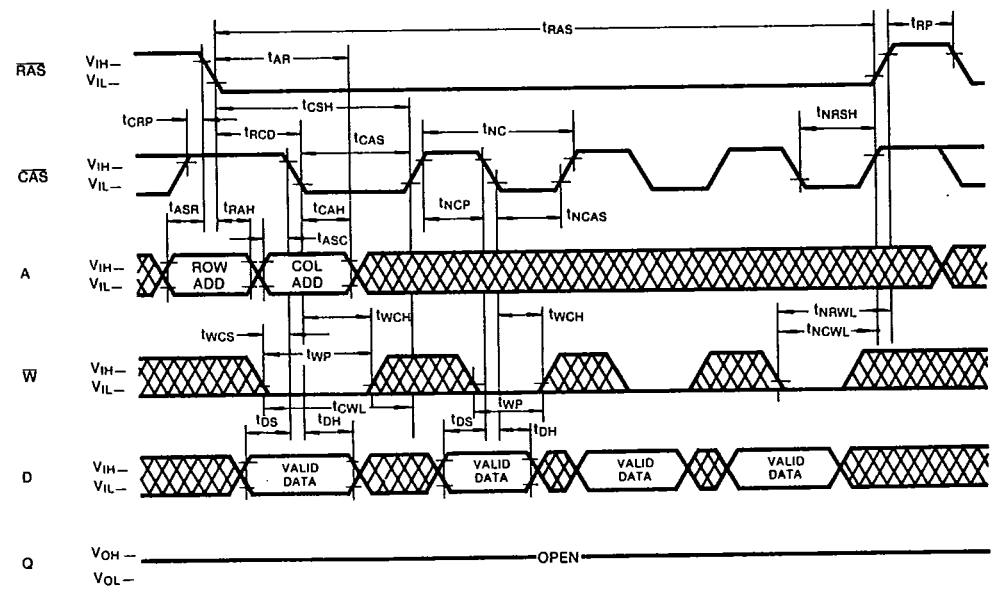
DON'T CARE

TIMING DIAGRAMS (Continued)

NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE

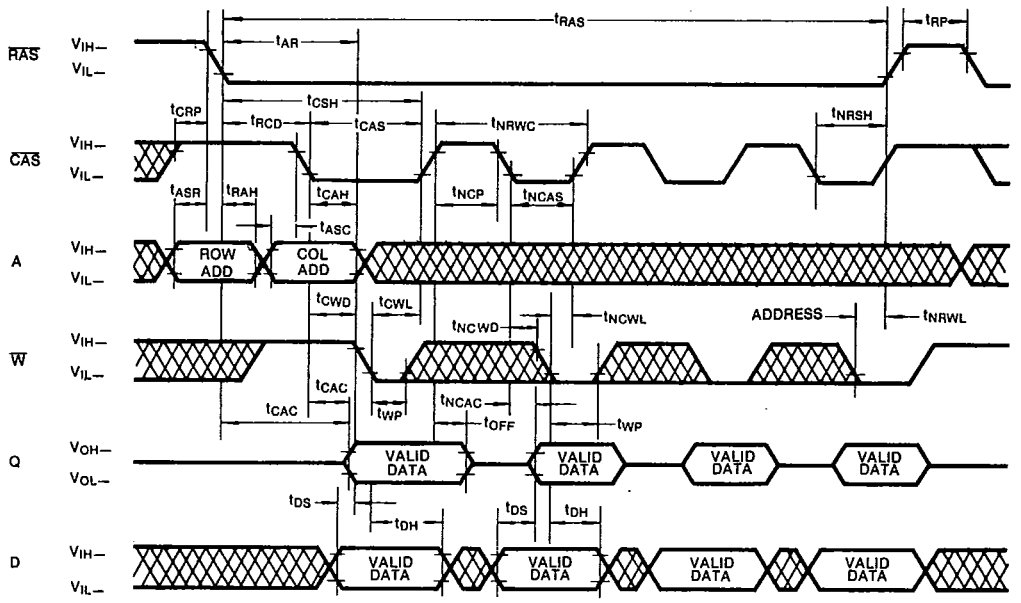


DON'T CARE

T-46-23-15

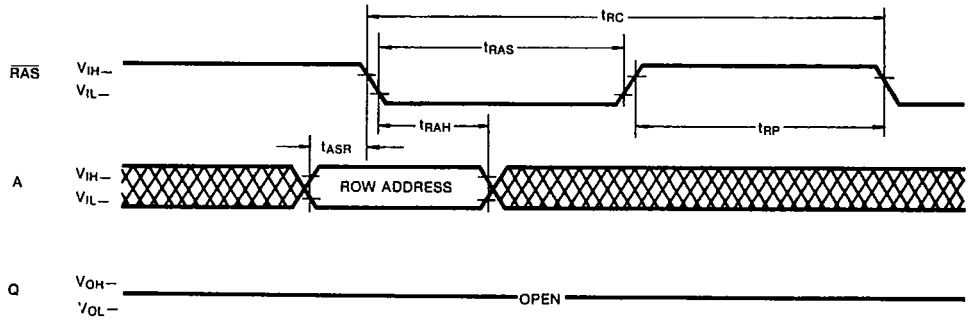
TIMING DIAGRAMS (Continued)

NIBBLE MODE READ-WRITE CYCLE



RAS-ONLY REFRESH CYCLE

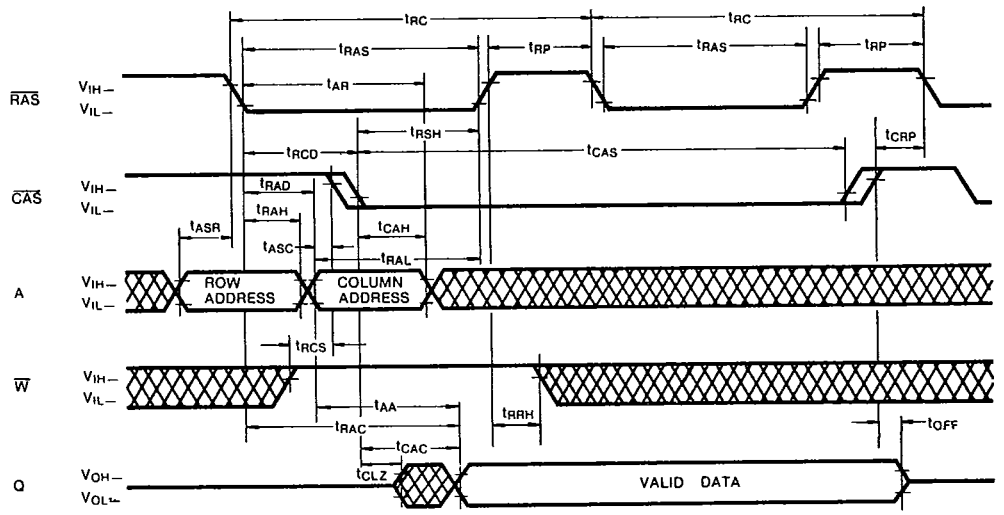
Note: $\overline{CAS}$ = V_{IH}, $\overline{W}$,D, A_9 = Don't Care



T-46-23-15

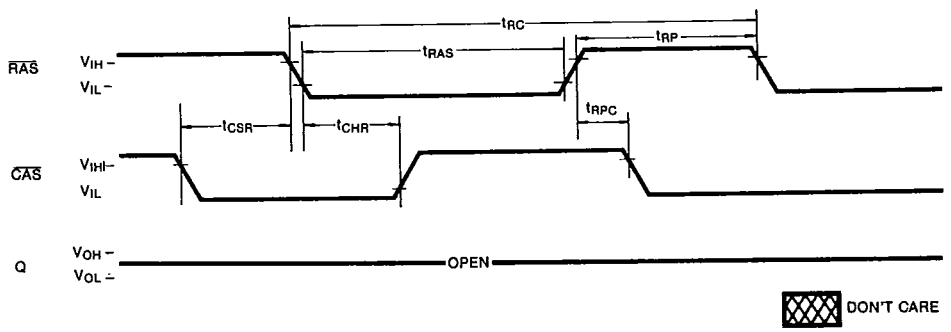
TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH CYCLE

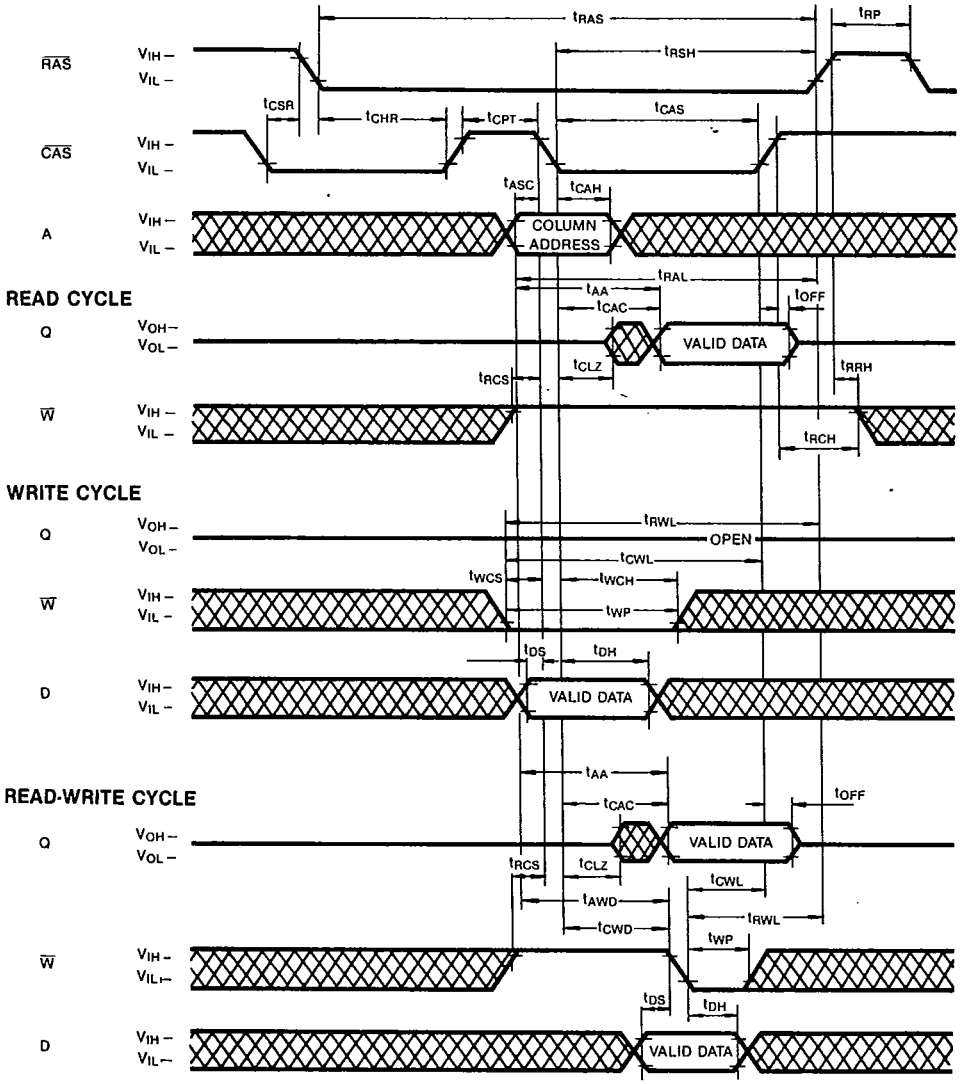
NOTE: $\overline{W}$ = Don't Care, A_0-A_9 = Don't Care



T-46-23-15

TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



T-46-23-15

2

KM41C1001A OPERATION

Device Operation

The KM41C1001A contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the KM41C1001A has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM41C1001A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C1001A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (tRP) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C1001A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CAS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

Write

The KM41C1001A can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters tCWD and tAWD are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C1001A has a tri-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (VIH) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C1001A operating cycles is listed below after the corresponding output state produced by the cycle.

T-46-23-15

Device Operation (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Nibble Mode Read, Nibble Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Nibble Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C1001A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0-A8). The state of address A9 is ignored during refresh.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C1001A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (tCSR) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C1001A hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C1001A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

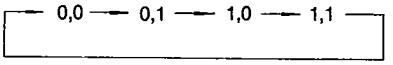
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter. The A9 bit is set low internally.

Nibble Mode

The KM41C1001A has Nibble mode capability. Nibble mode operation allows high speed serial read, write or read-modify-write access of 4 consecutive bits. The first of 4 bits is accessed in the usual manner. The remaining nibble bits are accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low.

The 4 bits of data that may be accessed during Nibble mode are determined by the lower 9 row address bits (R_{A0}-R_{A8}) and 9 column address bits (C_{A0}-C_{A8}). The two address bits, C_{A9} and R_{A9}, are used to select 1 of the 4 nibble bits for initial access. The remaining nibble bits are accessed by toggling $\overline{CAS}$ with $\overline{RAS}$ held low. Each high-low $\overline{CAS}$ transition will internally increment the nibble address (C_{A9}, R_{A9}) as shown in the following diagram with R_{A9} being the least significant bit.



If more than 4 bits are accessed during Nibble mode, the address sequence will wrap around and repeat. If any bit is written during Nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on a subsequent access, the new data will be written into the selected cell location.

A Nibble mode cycle can be a read, write, or read-modify-write cycle. Any combinations of reads and writes or read-modify-write are allowed.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C1001A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C1001A inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C1001A input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the VCC to VSS voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.3μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C1001A using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C1001A and they supply much of the current used by the KM41C1001A during cycling.

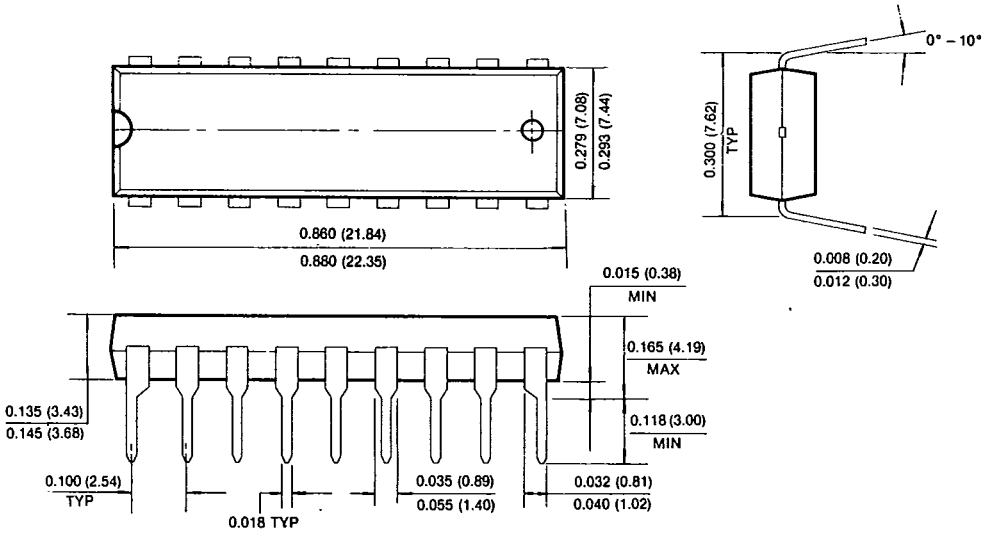
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

2

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (Millimeters)

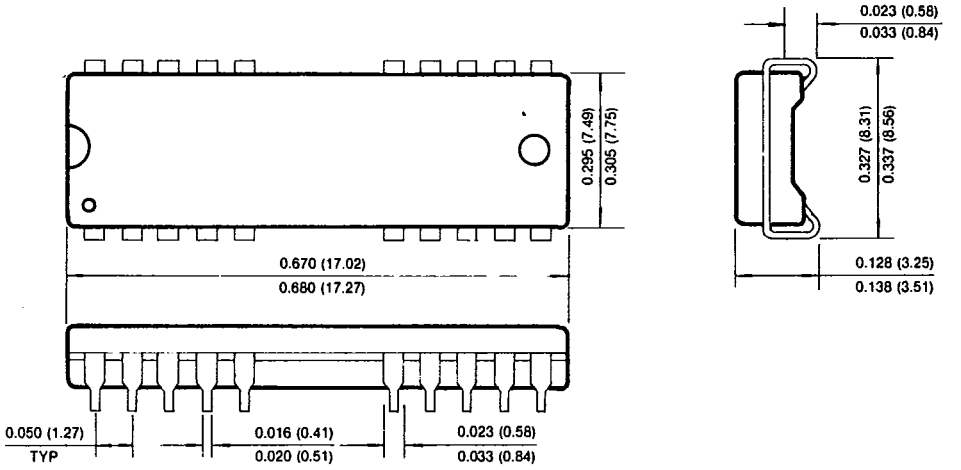


T-46-23-15

PACKAGE DIAGRAMS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-PIN PLASTIC ZIGZAG-IN-LINE PACKAGE