TYPES SN54HC4022, SN74HC4022
OCTAL COUNTERS/DIVIDERS

D2831, MARCH 1984

- **Carry-Out Output for Cascading**
- **Divide-by-N Counting**
- **DC Clock Input Circuit Allows Slow Rise Times**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

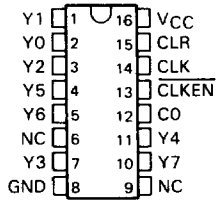
description

The 'HC4022 is a four-stage divide-by-8 Johnson counter with eight decoded outputs and a carry-out bit. High-speed operation and spike-free outputs are obtained by use of the Johnson octal counter configuration.

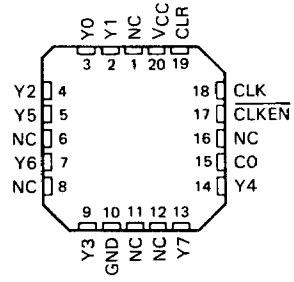
The eight decoded outputs are normally low and go high only at their respective octal time periods. A high signal on CLR asynchronously clears the octal counter and sets the carry output and Y0 high. With $\overline{\text{CLKEN}}$ low, the count is advanced on a low-to-high transition at CLK. Alternatively, if CLK is high, the count is advanced on a high-to-low transition at $\overline{\text{CLKEN}}$. Each decoded output remains high for one full clock cycle. The carry output C0 is high while Y0, Y1, Y2, or Y3 is high, then is low while Y4, Y5, Y6, or Y7 is high.

The SN54HC4022 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4022 is characterized for operation from −40°C to 85°C.

SN54HC4022 . . . J PACKAGE
SN74HC4022 . . . J OR N PACKAGE
(TOP VIEW)

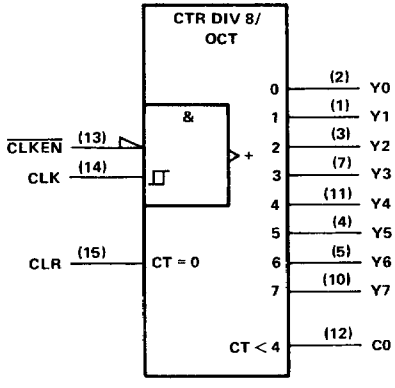


SN54HC4022 . . . FH OR FK PACKAGE
SN74HC4022 . . . FH OR FN PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol



Pin numbers shown are for J and N packages.

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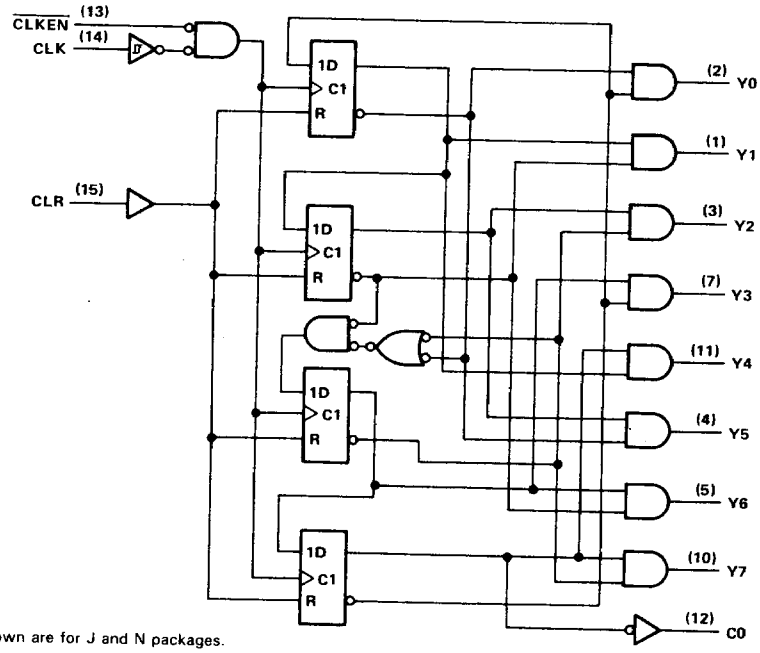
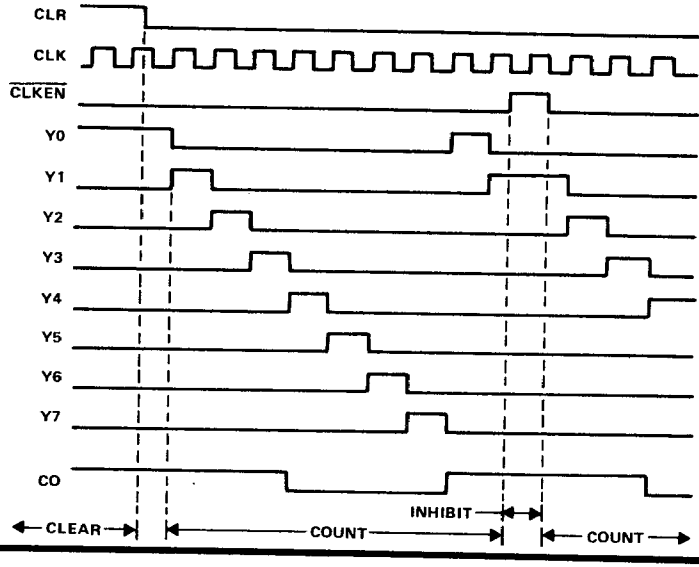
logic diagram (positive logic)



Pin numbers shown are for J and N packages.

typical clear, count, and inhibit sequences



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maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-10.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC4022		SN74HC4022		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t_w	Pulse duration, CLK high or low, $\overline{CLKEN}$ high or low, or CLR high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, $\overline{CLKEN}$ low or CLR inactive	2 V	50		75		65		ns
		4.5 V	10		15		13		
		6 V	9		13		11		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4022		SN74HC4022		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	10		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	55		25		29		
t_{pd}	CLK or CLR	Any Y	2 V		70	230		345		290	ns
			4.5 V		24	46		69		58	
			6 V		20	39		59		49	
t_{pd}	CLK or CLR	CO	2 V		60	230		345		290	ns
			4.5 V		19	46		69		58	
			6 V		16	39		59		49	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per counter	No load, T_A = 25°C	100 pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.