

XR-2211 FSK Demodulator/ Tone Decoder

accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal frequency within the passband, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set carrier frequency, bandwidth, and output delay.

Features

- Wide frequency range — 0.01 Hz to 300 kHz
- Wide supply voltage range — 4.5V to 20V
- DTL/TTL/ECL logic compatibility
- FSK demodulation with carrier-detector
- Wide dynamic range — 2 mV to 3 V_{RMS}
- Adjustable tracking range — ±1% to ±80%
- Excellent temperature stability — 20 ppm/°C typical

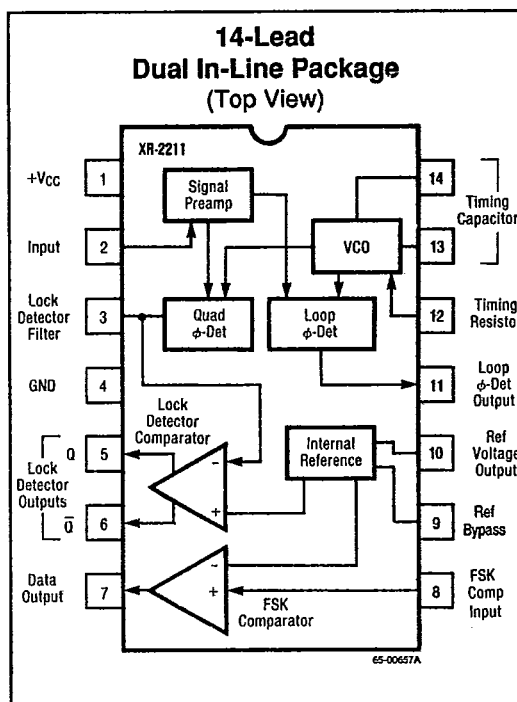
Applications

- FSK demodulation
- Data synchronization
- Tone decoding
- FM detection
- Carrier detection

Description

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications, and operates over a wide frequency range of 0.01 Hz to 300 kHz. It can

Connection Information



Absolute Maximum Ratings

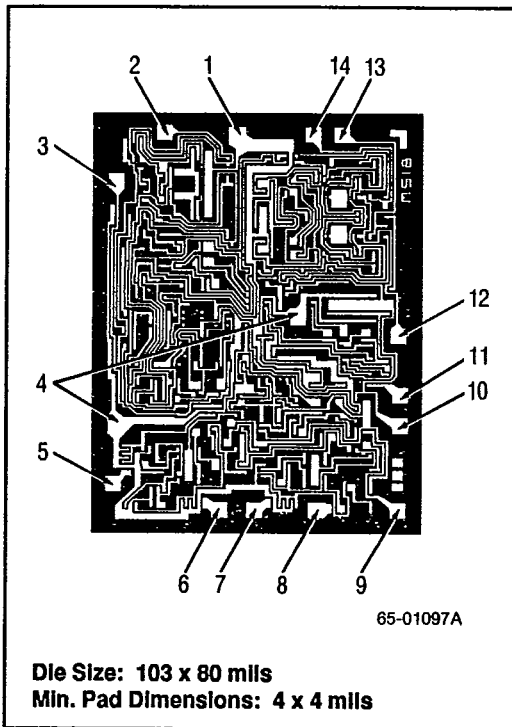
Supply Voltage+20V
 Input Signal Level3 V_{RMS}
 Storage Temperature
 Range-65°C to +150°C
 Operating Temperature Range
 XR2211MD-55°C to +125°C
 XR2211N-25°C to +85°C
 XR2211CN0°C to +70°C
 Lead Soldering Temperature
 (60 sec)+300°C

Ordering Information

| Part Number | Package | Operating Temperature Range |
|---------------|---------|-----------------------------|
| XR2211CN | N | 0°C to +70°C |
| XR2211N | N | -25°C to +85°C |
| XR2211MD | D | -55°C to +125°C |
| XR2211MD/883B | D | -55°C to +125°C |

Notes:
 /883B suffix denotes Mil-Std-883, Level B processing
 N = 14-lead plastic DIP
 D = 14-lead ceramic DIP
 Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

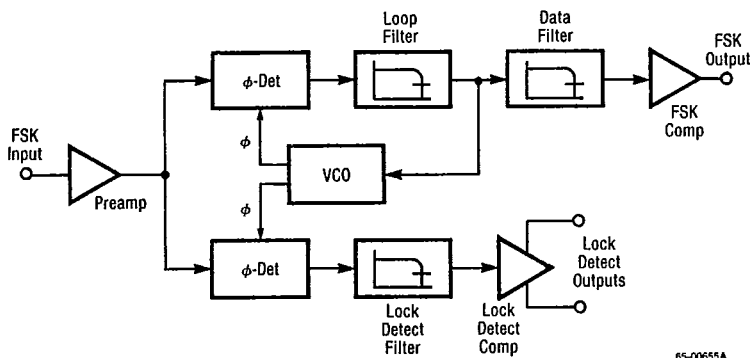
Mask Pattern



Thermal Characteristics

| | 14-Lead Plastic DIP | 14-Lead Ceramic DIP |
|--|---------------------|---------------------|
| Max. Junction Temp. | 125°C | 175°C |
| Max. P _D T _A <50°C | 468 mW | 1042 mW |
| Therm. Res. θ _{JC} | — | 50°C/W |
| Therm. Res. θ _{JA} | 160°C/W | 120°C/W |
| For T _A >50°C Derate at | 6.25 mW per °C | 8.33 mW per °C |

Functional Block Diagram



Electrical Characteristics (Test Conditions $+V_S = +12V$, $T_A = +25^\circ C$, $R_0 = 30k\Omega$, $C_0 = 0.033\mu F$. See Figure 1 for component designations.)

| Parameters | Test Conditions | XR-2211/M | | | XR-2211C | | | Units |
|---|---------------------------------------|-----------|-----------|-----------|----------|-----------|------|-----------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| General | | | | | | | | |
| Supply Voltage | | 4.5 | | 20 | 4.5 | | 20 | V |
| Supply Current | $R_0 \geq 10k\Omega$ | | 4.0 | 9.0 | | 5.0 | 11 | mA |
| Oscillator | | | | | | | | |
| Frequency Accuracy | Deviation from $f_0 = 1/ROC_0$ | | ± 1.0 | ± 3.0 | | ± 1.0 | | % |
| Frequency Stability ¹ Temperature Coefficient | $R_1 = \infty$ | | ± 20 | ± 50 | | ± 20 | | ppm/ $^\circ C$ |
| Power Supply Rejection | $+V_S = 12 \pm 1V$ | | 0.05 | 0.5 | | 0.05 | | %/V |
| | $+V_S = 5 \pm 0.5V$ | | 0.2 | | | 0.2 | | %/V |
| Upper Frequency Limit | $R_0 = 8.2k\Omega$, $C_0 = 400pF$ | 100 | 300 | | | 300 | | kHz |
| Lowest Practical Operating Frequency ¹ | $R_0 = 2M\Omega$ $C_0 = 50\mu F$ | | | 0.01 | | 0.01 | | Hz |
| Timing Resistor, R_0 Operating Range | | 5.0 | | 2000 | 5.0 | | 2000 | $k\Omega$ |
| | Recommended Range | 15 | | 100 | 15 | | 100 | $k\Omega$ |

Note: 1. Guaranteed by design.

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Electrical Characteristics (Continued)

($V_S = +12V$, $T_A = +25^\circ C$, $R_O = 30k\Omega$, $C_O = 0.033\mu F$. See Figure 1 for component designations.)

| Parameters | Test Conditions | XR-2211/M | | | XR-2211C | | | Units |
|--|---------------------|-----------|-----------|-----------|-----------|-----------|-----------|-------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Loop Phase Detector | | | | | | | | |
| Peak Output Current | Meas. at Pin 11 | ± 150 | ± 200 | ± 300 | ± 100 | ± 200 | ± 300 | μA |
| Output Offset Current | | | ± 1.0 | | | ± 2.0 | | μA |
| Output Impedance | | | 1.0 | | | 1.0 | | $M\Omega$ |
| Maximum Swing | Ref. to Pin 10 | ± 4.0 | ± 5.0 | | ± 4.0 | ± 5.0 | | V |
| Quadrature Phase Detector | | | | | | | | |
| Peak Output Current ² | Meas. at Pin 3 | 100 | 150 | | | 150 | | μA |
| Output Impedance | | | 1.0 | | | 1.0 | | $M\Omega$ |
| Maximum Swing | | | 11 | | | 11 | | V_{p-p} |
| Input Preamp | | | | | | | | |
| Input Impedance | Meas. at Pin 2 | | 20 | | | 20 | | $k\Omega$ |
| Input Signal Voltage Required to Cause Limiting ² | | | 2.0 | 10 | | 2.0 | | mV _{RMS} |
| Voltage Comparator | | | | | | | | |
| Input Impedance | Meas. at Pins 3 & 8 | | 2.0 | | | 2.0 | | $M\Omega$ |
| Input Bias Current | | | 100 | | | 100 | | nA |
| Voltage Gain ¹ | $R_L = 5.1k\Omega$ | 55 | 70 | | 55 | 70 | | dB |
| Output Voltage Low | $I_C = 3mA$ | | 300 | | | 300 | | mV |
| Output Leakage Current | $V_O = 12V$ | | 0.01 | | | 0.01 | | μA |
| Internal Reference | | | | | | | | |
| Voltage Level | Meas. at Pin 10 | 4.9 | 5.3 | 5.7 | 4.75 | 5.3 | 5.85 | V |
| Output Impedance | | | 100 | | | 100 | | Ω |

Notes:

1. Guaranteed by design.
2. Sample tested.

Description of Circuit Controls

Signal Input (Pin 2)

The input signal is AC coupled to this terminal. The internal impedance at pin 2 is 20 kΩ. Recommended input signal level is in the range of 10 mV_{RMS} to 3 V_{RMS}.

Quadrature Phase Detector Output (Pin 3)

This is the high-impedance output of the quadrature phase detector, and is internally connected to the input of lock-detect voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 1) to eliminate chatter at the lock-detect outputs. If this tone-detect section is not used, pin 3 can be left open circuited.

Lock-Detect Output, Q (Pin 5)

The output at pin 5 is at a "high" state when the PLL is out of lock and goes to a "low" or conducting stage when the PLL is locked. It is an open collector type output and requires a pull-up resistor, R_L, to +V_S for proper operation. In the "low" state it can sink up to 5 mA of load current.

Lock-Detect Complement, \bar{Q} (Pin 6)

The output at pin 6 is the logic complement of the lock-detect output at pin 5. This output is also an open collector type stage which can sink 5 mA of load current in the low or "on" state.

FSK Data Output (Pin 7)

This output is an open collector logic stage which requires a pull-up resistor, R_L, to +V_S for proper operation. It can sink 5 mA of load current. When decoding FSK signals the FSK data output will switch to a "high" or off state for low input frequency, and will switch to a "low" or on state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

FSK Comparator Input (Pin 8)

This is the high-impedance input to the FSK voltage comparator. Normally, an FSK post detection or data filter is connected between this terminal and the PLL phase-detector output (pin 11). This data filter is formed by R_F and C_F of Figure 1. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at pin 10.

Reference Bypass (Pin 9)

This pin can have an optional 0.1 μF capacitor connected to the ground.

Reference Voltage, V_R (Pin 10)

This pin is internally biased at the reference voltage level, V_R; V_R = V_S/2 - 650 mV. The dc voltage level at this pin forms an internal reference for the voltage levels at pin 3, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1 μF capacitor.

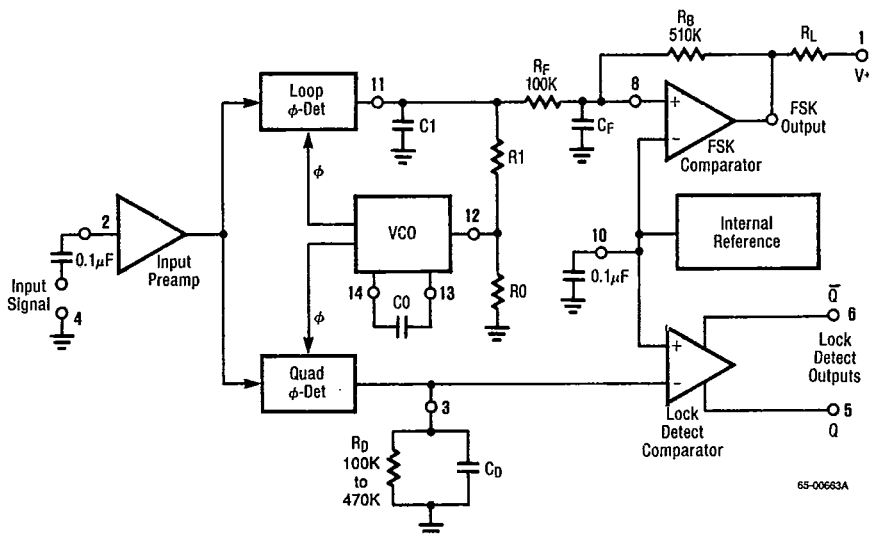


Figure 1. Generalized Circuit Connection for FSK and Tone Detection

Loop Phase Detector Output (Pin 11)

This terminal provides a high impedance output for the loop phase-detector. The PLL loop filter is formed by R1 and C1 connected to pin 11 (see Figure 1). With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to V_R . The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

VCO Control Input (Pin 12)

VCO free-running frequency is determined by external timing resistor, R0, connected from this terminal to ground. The VCO free-running frequency, f_0 , is given by:

$$f_0(\text{Hz}) = \frac{1}{R0C0}$$

where C0 is the timing capacitor across pins 13 and 14. For optimum temperature stability R0 must be in the range of 10k Ω to 100k Ω (see Typical Electrical Characteristics).

This terminal is a low impedance point, and is internally biased at a DC level equal to V_R . The maximum timing current drawn from pin 12 must be limited to $\leq 3\text{mA}$ for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14)

VCO frequency is inversely proportional to the external timing capacitor, C0, connected across these terminals. C0 must be non-polarized, and in the range of 200pF to 10 μF .

VCO Frequency Adjustment

VCO can be fine tuned by connecting a potentiometer, R_x , in series with R0 at pin 12 (see Figure 2).

VCO Free-Running Frequency, f_0

The XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase-detector sections of the circuit. However, for setup or adjustment purposes, the VCO free-running frequency can be measured at pin 3 (with C_D disconnected) with no input and with pin 2 shorted to pin 10.

Design Equations

See Figure 1 for Definitions of Components.

1. VCO Center Frequency, f_0 :

$$f_0(\text{Hz}) = \frac{1}{R0C0}$$

2. Internal Reference Voltage, V_R (measured at pin 10):

$$V_R = \left(\frac{+V_S}{2}\right) - 650\text{mV}$$

3. Loop Lowpass Filter Time Constant, τ :

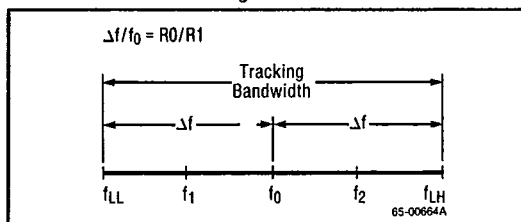
$$\tau = R1C1$$

4. Loop Damping, ζ :

$$\zeta = \left(\sqrt{\frac{C0}{C1}}\right) \left(\frac{1}{4}\right)$$

5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$:

$$\Delta f/f_0 = R0/R1$$



6. FSK Data Filter Time Constant, τ_F :

$$\tau_F = R_F C_F$$

7. Loop Phase Detector Conversion Gain, K_ϕ : (K_ϕ is the differential DC voltage across pins 10 and 11, per unit of phase error at phase-detector input):

$$K_\phi \text{ (in volts per radian)} = \frac{(-2)(V_R)}{\pi}$$

8. VCO Conversion Gain, K_0 , is the amount of change in VCO frequency per unit of DC voltage change at pin 11:

$$K_0 \text{ (in Hertz per volt)} = \frac{-1}{C0R1V_R}$$

9. Total Loop Gain, K_T :

$$K_T \text{ (in radians per second per volt)} = 2\pi K_\phi K_0 = 4/C0R1$$

10. Peak Phase-Detector Current, I_A :

$$I_A \text{ (mA)} = \frac{V_R}{25}$$

Applications

FSK Decoding

Figure 2 shows the basic circuit connection for FSK decoding. With reference to Figures 1 and 2, the functions of external components are defined as follows: R₀ and C₀ set the PLL center frequency, R₁ sets the system bandwidth, and C₁ sets the loop filter time constant and the loop damping factor. C_F and R_F form a one pole post-detection filter for the FSK data output. The resistor R_B (= 510kΩ) from pin 7 to pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bauds are given in Table 1.

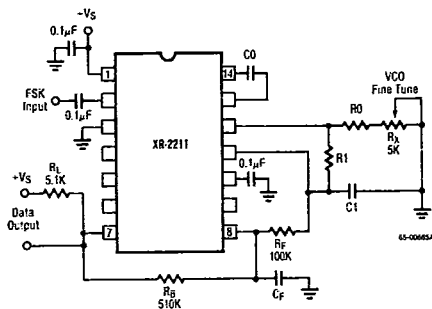


Figure 2. Circuit Connection for FSK Decoding

Table 1. Recommended Component Values for Commonly Used FSK Bands (See Circuit of Figure 2)

| FSK Band | Component Values |
|-------------------------|--|
| 300 Baud | C ₀ = 0.039µF C _F = 0.005µF |
| f ₁ = 1070Hz | C ₁ = 0.01µF R ₀ = 18kΩ |
| f ₂ = 1270Hz | R ₁ = 100kΩ |
| 300 Baud | C ₀ = 0.022µF C _F = 0.005µF |
| f ₁ = 2025Hz | C ₁ = 0.0047µF R ₁ = 18kΩ |
| f ₂ = 2225Hz | R ₁ = 200kΩ |
| 1200 Baud | C ₀ = 0.027µF C _F = 0.0022µF |
| f ₁ = 1200Hz | C ₁ = 0.01µF R ₀ = 18kΩ |
| f ₂ = 2200Hz | R ₁ = 30kΩ |

Design Instructions

The circuit of Figure 2 can be tailored for any FSK decoding application by the choice of five key circuit components; R₀, R₁, C₀, C₁ and C_F. For a given set of FSK mark and space frequencies, f₁ and f₂, these parameters can be calculated as follows:

1. Calculate PLL center frequency, f₀

$$f_0 = \frac{f_1 + f_2}{2}$$

2. Choose a value of timing resistor R₀ to be in the range of 10kΩ to 100kΩ. This choice is arbitrary. The recommended value is R₀ ≈ 20kΩ. The final value of R₀ is normally fine-tuned with the series potentiometer, R_X.

3. Calculate value of C₀ from Design Equation No. 1 or from Typical Performance Characteristics:

$$C_0 = 1/R_0 f_0$$

4. Calculate R₁ to give a Δf equal to the mark-space deviation:

$$R_1 = R_0 [f_0 / (f_1 - f_2)]$$

5. Calculate C₁ to set loop damping. (See Design Equation No. 4.)

Normally, ζ ≈ 1/2 is recommended

$$\text{Then: } C_1 = C_0/4 \text{ for } \zeta = 1/2$$

6. Calculate Data Filter Capacitance, C_F: For R_F = 100kΩ, R_B = 510kΩ, the recommended value of C_F is:

$$C_F \text{ (in } \mu\text{F)} = \frac{3}{\text{Baud Rate}}$$

Note: All calculated component values except R₀ can be rounded off to the nearest standard value, and R₀ can be varied to fine-tune center frequency through a series potentiometer, R_X (see Figure 2).

Design Example

75 Baud FSK demodulator with mark/space frequencies of 1110/1170Hz:

Step 1: Calculate f₀:

$$f_0 = (1110 + 1170) (1/2) = 1140\text{Hz}$$

Step 2: Choose R₀ = 20kΩ (18kΩ fixed resistor in series with 5kΩ potentiometer)

Step 3: Calculate C₀ from V_{CO} Frequency vs. Timing Capacitor: C₀ = 0.044µF

Step 4: Calculate R₁: R₁ = R₀ (2240/60) = 380kΩ

Step 5: Calculate C₁: C₁ = C₀/4 = 0.011µF

Note: All values except R₀ can be rounded off to nearest standard value.

FSK Decoding With Carrier Detect

The lock-detect section of the XR-2211 can be used as a carrier detect option for FSK decoding. The recommended circuit connection for this application is shown in Figure 3. The open-collector lock-detect output, pin 6, is shorted to the data output (pin 7). Thus, the data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL, and the pin 6 output goes "high" to enable the data output.

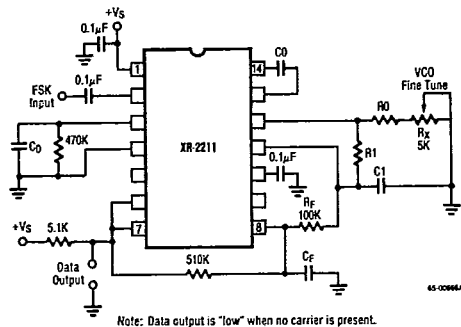


Figure 3. External Connections for FSK Demodulation With Carrier Detect Capability

The minimum value of the lock-detect filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta f_c$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1 . For most applications, $\Delta f_c < \Delta f/2$. For $R_D = 470k\Omega$, the approximate minimum value of C_D can be determined by:

$$C_D(\mu F) \geq 16/\text{capture range in Hz}$$

With values of C_D that are too small, chatter can be observed on the lock-detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock-detect output.

Tone Detection

Figure 4 shows the generalized circuit connection for tone detection. The logic outputs, Q and \bar{Q} at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is

present within the detection band of the PLL, the logic state at these outputs becomes reversed for the duration of the input tone. Each logic output can sink 5mA of load current.

Both logic outputs at pins 5 and 6 are open-collector type stages, and require external pull-up resistors R_{L1} and R_{L2} as shown in Figure 4.

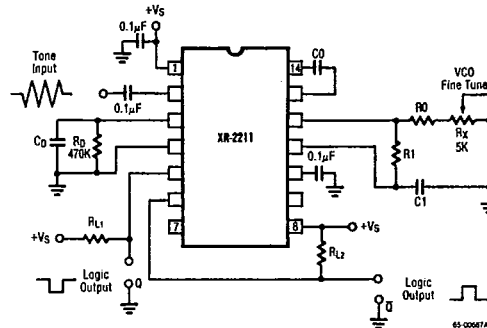


Figure 4. Circuit Connection for Tone Detection

With reference to Figures 1 and 4, the function of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency, R_1 sets the detection bandwidth, C_1 sets the lowpass-loop filter time constant and the loop damping factor, and R_{L1} and R_{L2} are the respective pull-up resistors for the Q and \bar{Q} logic outputs.

Design Instructions

The circuit of Figure 4 can be optimized for any tone-detection application by the choice of five key circuit components: R_0 , R_1 , C_0 , C_1 , and C_D . For a given input tone frequency, f_s , these parameters are calculated as follows:

1. Choose R_0 to be in the range of $15k\Omega$ to $100k\Omega$. This choice is arbitrary.
2. Calculate C_0 to set center frequency, f_0 equal to f_s : $C_0 = 1/R_0f_s$.
3. Calculate R_1 to set bandwidth $\pm\Delta f$ (see Design Equation No. 5): $R_1 = R_0(f_0/\Delta f)$

Note: The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$.

- Calculate value of C1 for a given loop damping factor:

$$C1 = C0/16\zeta^2$$

Normally $\zeta \approx 1/2$ is optimum for most tone-detector applications, giving $C1 = 0.25 C0$.

Increasing C1 improves the out-of-band signal rejection, but increases the PLL capture time.

- Calculate value of filter capacitor CD. To avoid chatter at the logic output, with RD = 470kΩ, CD must be:

$$CD(\mu F) \geq (16/\text{capture range in Hz})$$

Increasing CD slows the logic output response time.

Design Examples

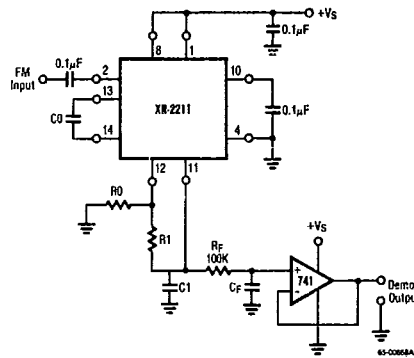
Tone detector with a detection band of 1kHz ±20Hz:

- Step 1: Choose R0 = 20kΩ (18kΩ in series with 5kΩ potentiometer).
- Step 2: Choose C0 for f0 = 1kHz: C0 = 0.05μF.
- Step 3: Calculate R1: R1 = (R0) (1000/20) = 1MΩ.
- Step 4: Calculate C1: for $\zeta = 1/2$, C1 = 0.25μF, C0 = 0.013μF.
- Step 5: Calculate CD: CD = 16/38 = 0.42μF.
- Step 6: Fine tune the center frequency with the 5kΩ potentiometer, RX.

Linear FM Detection

The XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for the application is shown

in Figure 5. The demodulated output is taken from the loop phase detector output (pin 11), through a post detection filter made up of RF and CF, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 5.



Note: See section on Design Equations for Component Values.

Figure 5. Linear FM Detector Using XR-2211 and an External Op Amp

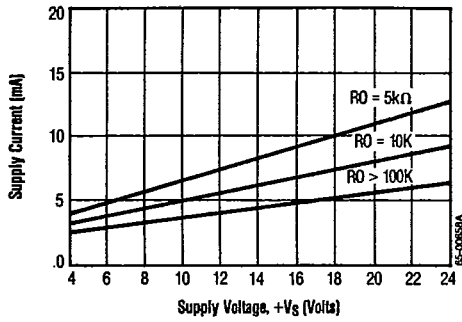
The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$$V_{OUT} = R1 V_R/100 R0 \text{ Volts/\% deviation}$$

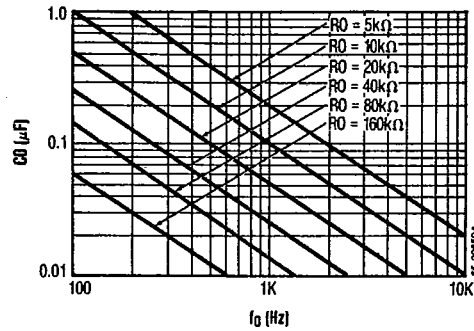
where VR is the internal reference voltage. For the choice of external components R1, R0, CD, C1 and CF, see the section on Design Equations.

Typical Performance Characteristics

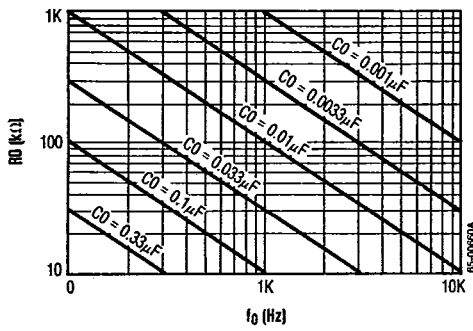
Typical Supply Current vs. +V_S (Logic Outputs Open Circuited)



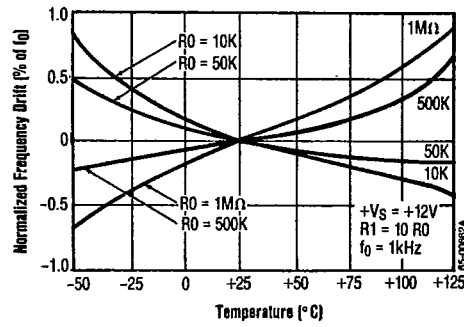
VCO Frequency vs. Timing Resistor



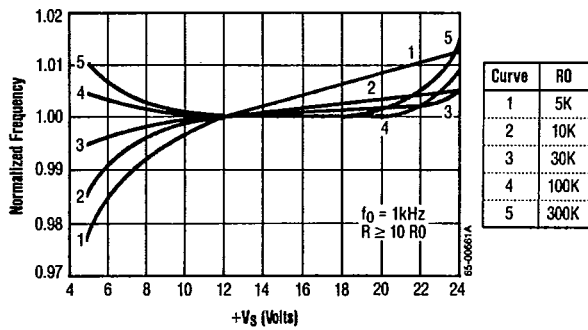
VCO Frequency vs. Timing Capacitor



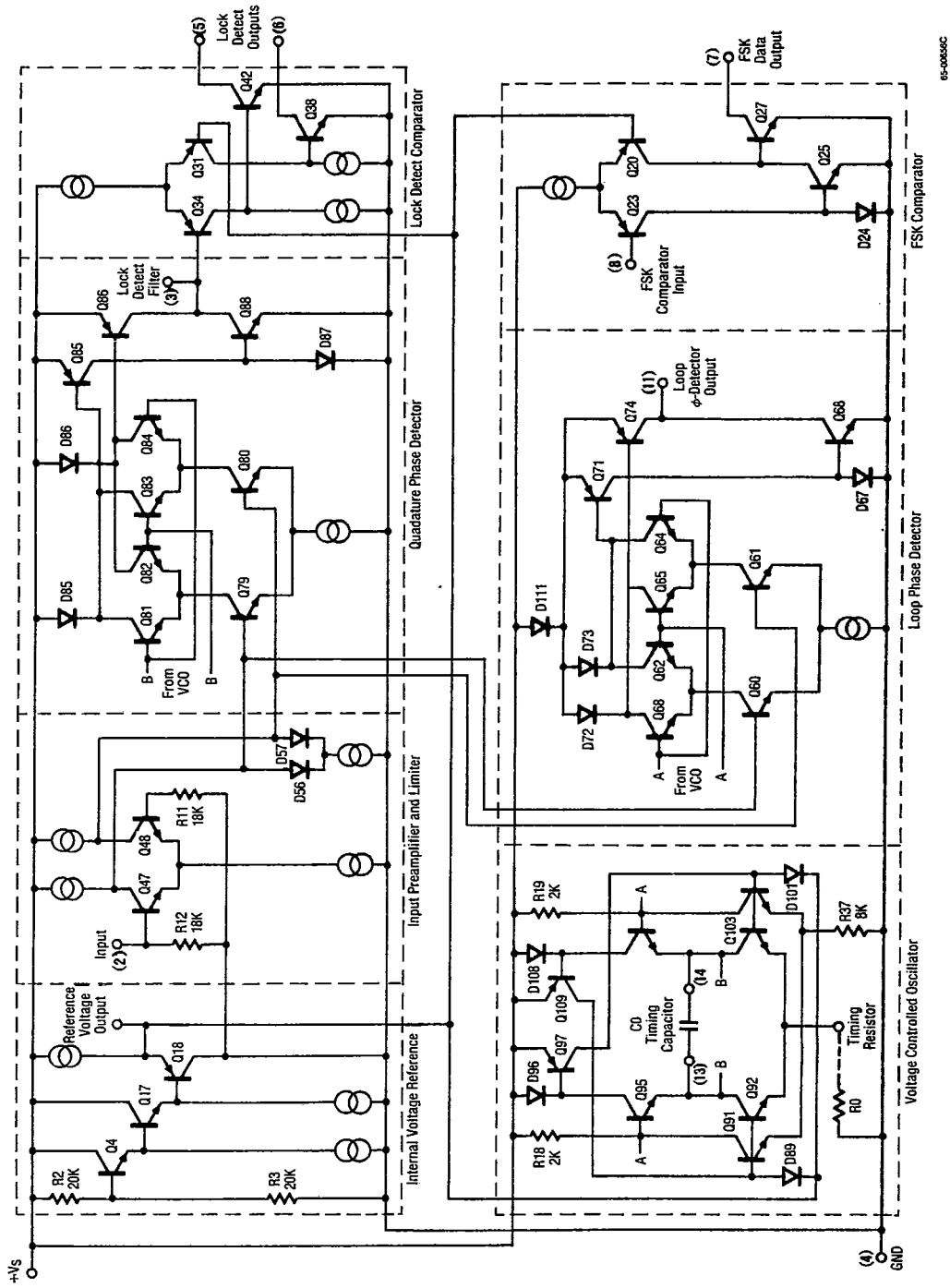
Typical Center Frequency Drift vs. Temperature



Typical f₀ vs. Power Supply Characteristics



Schematic Diagram



62-0085C