



CY54/74FCT646T CY54/74FCT648T

8-Bit Registered Transceivers

Features

- Function, pinout and drive compatible with FCT and F logic
- FCT-C speed at 5.4 ns max. (Com'1)
- FCT-A speed at 6.3 ns max. (Com'1)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V

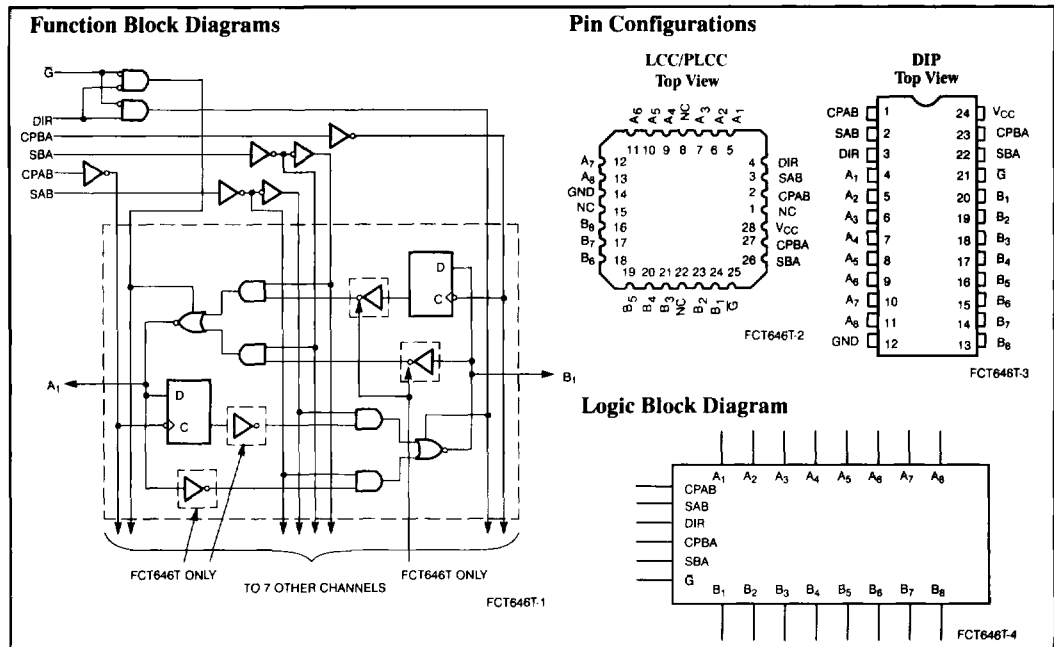
- Sink current 64 mA (Com'1), 48 mA (Mil)
- Source current 32 mA (Com'1), 12 mA (Mil)
- Independent register for A and B buses
- Three-state output

Functional Description

The FCT646T and FCT648T consist of a bus transceiver circuit with three-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH

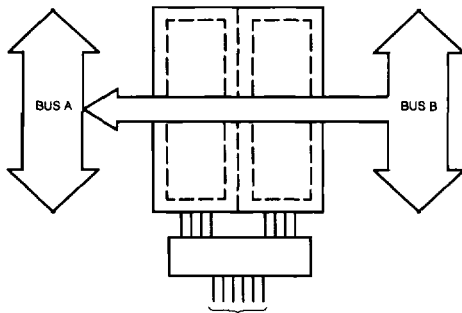
logic level. Enable Control \bar{G} and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control \bar{G} is Active LOW. In the isolation mode (enable Control \bar{G} HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.



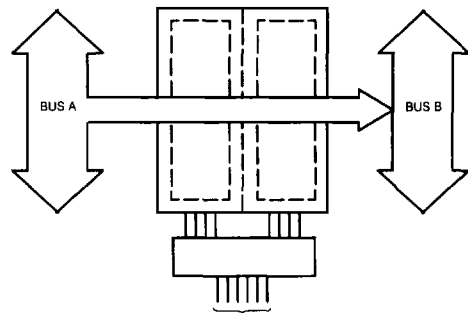
Pin Description

Name	Description
A	Data Register A Inputs, Data Register B Outputs
B	Data Register B Inputs, Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, \bar{G}	Output Enable Inputs



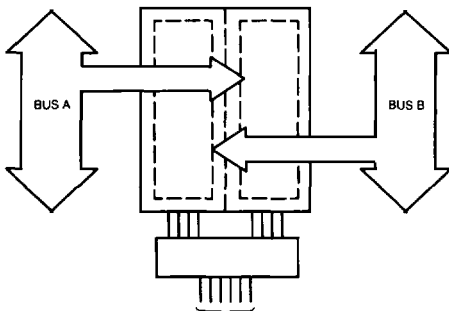
DIR	G	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus B to Bus A



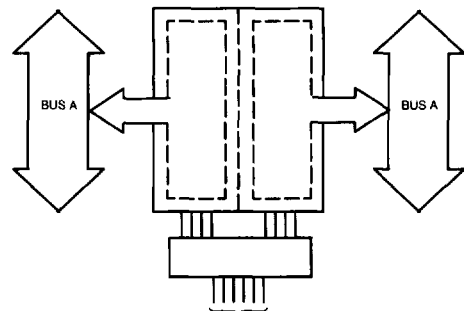
DIR	G	CPAB	CPBA	SAB	SBA
H	L	X	X	L	X

Real-Time Transfer
Bus A to Bus B



DIR	G	CPAB	CPBA	SAB	SBA
H	L	X	X	X	X
L	L	∩	∩	X	X
X	H	∩	∩	X	X

Storage from
A and/or B



DIR ^[1]	G	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

Transfer Stored Data
to A and/or B

Function Table^[2]

Inputs						Data I/O ^[3]		Operation or Function	
G	DIR	CPAB	CPBA	SAB	SBA	A ₁ thru A ₈	B ₁ thru B ₈	FCT646T	FCT648T
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	∩	∩	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time B̄ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored B̄ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time Ā Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored Ā Data to B Bus

Notes:

- Cannot transfer data to A bus and B bus simultaneously.
- H = HIGH Voltage Level, L = LOW Voltage Level, ∩ = LOW-to-HIGH Transition, X = Don't Care.
- The data output functions may be enabled or disabled by various signals at the G or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.



Maximum Ratings^[4, 5]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -65°C to +135°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage -0.5V to +7.0V
 DC Output Voltage -0.5V to +7.0V
 DC Output Current (Maximum Sink Current/Pin) 120 mA
 Power Dissipation 0.5W

Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	-40°C to +85°C	5V ± 5%
Military ^[6]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[7]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com ¹	2.0			V
		V _{CC} =Min., I _{OH} =-15 mA	Com ¹	2.4	3.3		V
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com ¹		0.3	0.55	V
		V _{CC} =Min., I _{OL} =48 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[8]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA			-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OS}	Output Short Circuit Current ^[9]	V _{CC} =Max., V _{OUT} =0.0V		-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Capacitance^[8]

Parameter	Description	Typ. ^[7]	Max.	Unit
C _{IN}	Input Capacitance	6	10	pF
C _{OUT}	Output Capacitance	8	12	pF

Notes:

4. Unless otherwise noted, these limits are over the operating free-air temperature range.
5. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
6. T_A is the "instant on" case temperature.
7. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
8. This parameter is guaranteed but not tested.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[7]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max., V _{IN} =3.4V, ^[10] f _I =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[11]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, G=DIR=GND, GAB=GBA=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.06	0.12	mA/ MHz
I _C	Total Power Supply Current ^[12]	V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f _I =5 MHz, G=DIR=GND, GAB=GBA=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f _I =5 MHz, G=DIR=GND, GAB=GBA=GND, V _{IN} =3.4V or V _{IN} =GND	1.2	3.4	mA
		V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f _I =5 MHz, G=DIR=GND, GAB=GBA=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	2.8	5.6 ^[13]	mA
		V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f _I =5 MHz, G=DIR=GND, GAB=GBA=GND, V _{IN} =3.4V or V _{IN} =GND	5.1	14.6 ^[13]	mA

Notes:

10. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.

11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

12. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f_IN_I)

I_{CC} = Quiescent Current with CMOS input levels

ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)

D_H = Duty Cycle for TTL inputs HIGH

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)

f₀ = Clock frequency for registered devices, otherwise zero

f_I = Input signal frequency

N_I = Number of inputs changing at f_I

All currents are in milliamps and all frequencies are in megahertz.

13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



Switching Characteristics Over the Operating Range

Parameter	Description	FCT646T/FCT648T				FCT646AT/FCT648AT				Unit	Fig. No. ^[15]
		Military		Commercial		Military		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	2.0	11.0	1.5	9.0	2.0	7.7	1.5	6.3	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time Enable to Bus and DIR to A _n or B _n	2.0	15.0	1.5	14.0	2.0	10.5	1.5	9.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time G to Bus and DIR to Bus	2.0	11.0	1.5	9.0	2.0	7.7	1.5	6.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus	2.0	10.0	1.5	9.0	2.0	7.0	1.5	6.3	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to A or B	2.0	12.0	1.5	11.0	2.0	8.4	1.5	7.7	ns	1, 5
t _S	Set-Up Time HIGH or LOW, Bus to Clock	4.5		4.0		2.0		2.0		ns	4
t _H	Hold Time HIGH or LOW, Bus to Clock	2.0		2.0		1.5		1.5		ns	4
t _w	Pulse Width, ^[6] HIGH or LOW	6.0		6.0		5.0		5.0		ns	5

Parameter	Description	FCT646CT/FCT648CT				Unit	Fig. No. ^[15]
		Military		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	1.5	6.0	1.5	5.4	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time Enable to Bus and DIR to A _n or B _n	1.5	8.9	1.5	7.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time G to Bus and DIR to Bus	1.5	7.7	1.5	6.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus	1.5	6.3	1.5	5.7	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to A or B	1.5	7.0	1.5	6.2	ns	1, 5
t _S	Set-Up Time, HIGH or LOW, Bus to Clock	2.0		2.0		ns	4
t _H	Hold Time, HIGH or LOW, Bus to Clock	1.5		1.5		ns	4
t _w	Pulse Width, ^[6] HIGH or LOW	5.0		5.0		ns	5

Notes:

14. Minimum limits are guaranteed but not tested on Propagation Delays.

15. See "Parameter Measurement Information" in the General Information Section.



Ordering Information – FCT646T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT646CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT646CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT646CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT646CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT646CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT646ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT646ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT646ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT646ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT646ATLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT646TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT646TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT646TSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT646TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT646TLMB	L64	28-Square Leadless Chip Carrier	

Ordering Information—FCT648T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT648CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT648CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT648CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT648CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT648CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT648ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT648ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT648ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT648ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT648ATLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT648TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT648TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT648TSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT648TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT648TLMB	L64	28-Square Leadless Chip Carrier	

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