

DESCRIPTION

The M5L8212P is an input/output port consisting of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also a service request flip-flop for the generation and control of interrupts to a microprocessor is included.

FEATURES

- Parallel 8-bit data register and buffer
- Service request flip-flop for interrupt generation
- Three-state outputs
- Low input load current: $I_{IL} = -250\mu\text{A}$ (max.)
- High output sink current: $I_{OL} = 16\text{mA}$ (max.)
- High-level output voltage for direct interface to a M5L8085AP, CPU: $V_{OH} = 3.65\text{V}$ (min.)

APPLICATION

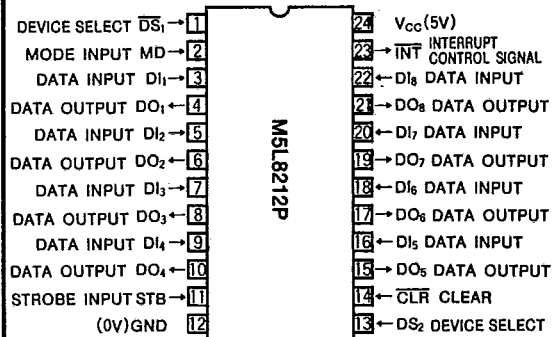
Input/output port for a M5L8085AP

Latches, gate buffers or multiplexers

Peripheral and input/output functions for microcomputer systems

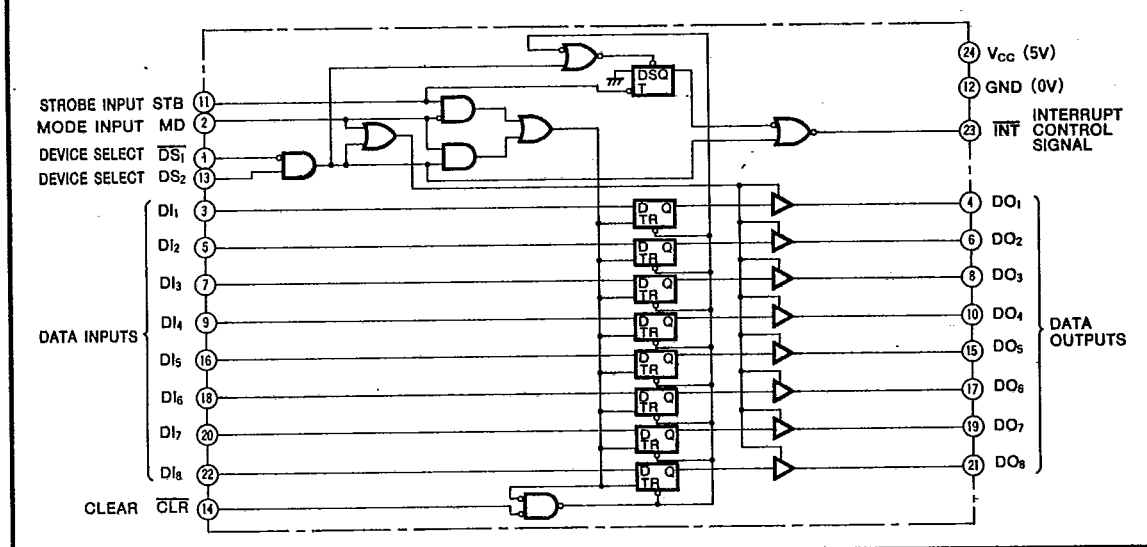
FUNCTION

Device select 1 (\overline{DS}_1) and device select 2 (DS_2) are used for chip selection when the mode input MD is low. When \overline{DS}_1 is low and DS_2 is high, the data in the latches is transferred to the data outputs $DO_1 \sim DO_8$, and the service request flip-flop SR is set. Also, the strobed input STB is active, the data inputs $DI_1 \sim DI_8$ are latched in the data latches, and the service request flip-flop SR is reset.

PIN CONFIGURATION (TOP VIEW)

Outline 24P4

When MD is high, the data in the data latches is transferred to the data outputs. When \overline{DS}_1 is low and DS_2 is high, the data inputs are latched in the data latches. The low-level clear input \overline{CLR} resets the data latches and sets the service request flip-flop SR, but the state of the output buffers is not changed.

BLOCK DIAGRAM

MITSUBISHI (MICMPTR/MIPRC)

M5L8212P

T-52-33-53

8-BIT INPUT/OUTPUT PORT WITH 3-STATE OUTPUT

ABSOLUTE MAXIMUM RATINGS ($T_a=0\sim 75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply voltage		7.0	V
V_I	Input voltage \overline{DS}_1 , MD inputs		V_{CC}	V
V_I	Input voltage all other inputs except \overline{DS}_1 , MD		5.5	V
V_O	Output voltage		V_{CC}	V
P_d	Power dissipation		800	mW
T_{opr}	Operating free-air temperature range		0~75	$^\circ\text{C}$
T_{stg}	Storage temperature range		-55~125	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a=0\sim 75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			16	mA

ELECTRICAL CHARACTERISTICS ($T_a=0\sim 75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.85	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75\text{V}$, $I_C=-5\text{mA}$			-1	V
V_{OH}	High-level output voltage	$V_{CC}=4.75\text{V}$, $V_{IH}=2\text{V}$ $V_{IL}=0.85\text{V}$, $I_{OH}=-1\text{mA}$	3.65			V
V_{OL}	Low-level output voltage	$V_{CC}=4.75\text{V}$, $V_{IH}=2\text{V}$, $V_{IL}=0.85\text{V}$, $I_{OL}=15\text{mA}$			0.45	V
I_{OZ}	Three-state output current	$V_{CC}=5.25\text{V}$, $V_{IH}=2\text{V}$, $V_{IL}=0.85\text{V}$, $V_C=5.25\text{V}$			20	μA
I_{OZ}	Three-state output current	$V_{CC}=5.25\text{V}$, $V_{IH}=2\text{V}$, $V_{IL}=0.85\text{V}$, $V_O=0.45\text{V}$			-20	μA
I_{IH}	High-level input current, STB, \overline{DS}_2 , CLR, $D_1\sim D_6$ inputs	$V_{CC}=5.25\text{V}$, $V_I=5.25\text{V}$			10	μA
I_{IH}	High-level input current, MD input	$V_{CC}=5.25\text{V}$, $V_I=5.25\text{V}$			30	μA
I_{IH}	High-level input current, \overline{DS}_1 input	$V_{CC}=5.25\text{V}$, $V_I=5.25\text{V}$			40	μA
I_{IL}	Low-level input current, STB, \overline{DS}_2 , CLR, $D_1\sim D_6$ inputs	$V_{CC}=5.25\text{V}$, $V_I=0.5\text{V}$			-0.25	mA
I_{IL}	Low-level input current, MD input	$V_{CC}=5.25\text{V}$, $V_I=0.5\text{V}$			-0.75	mA
I_{IL}	Low-level input current, \overline{DS}_1 input	$V_{CC}=5.25\text{V}$, $V_I=0.5\text{V}$			-1	mA
I_{OS}	Short-circuit output current (Note 3)	$V_{CC}=5.0\text{V}$	-15		-75	mA
I_{CC}	Supply current from V_{CC}	$V_{CC}=5.25\text{V}$			130	mA

Note 1 : All voltage are with respect to GND terminal. Reference voltage (pin 12) is considered as 0V and all maximum and minimum values are defined in absolute values.

2 : Current flowing into an IC is positive, out is negative. The maximum and minimum values are defined in absolute values.

3 : All measurements should be done quickly, and two outputs should not be measured at the same time.

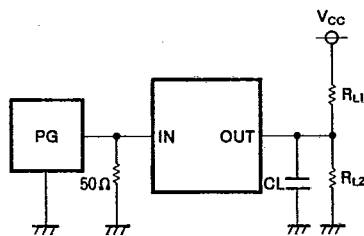
TIMING REQUIREMENTS ($T_a=0\sim 75^\circ\text{C}$, $V_{CC}=5\text{V}\pm 5\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(DS2)}$	Input pulse width, \overline{DS}_1 , \overline{DS}_2 and STB		30			ns
$t_{SU(DA)}$	Data setup time with respect to \overline{DS}_1 , \overline{DS}_2 and STB		15			ns
$t_{h(DA)}$	Data hold time with respect to \overline{DS}_1 , \overline{DS}_2 and STB		20			ns

SWITCHING CHARACTERISTICS ($T_a=0\sim 75^\circ\text{C}$, $V_{CC}=5V\pm 5\%$, unless otherwise noted)

Symbol	Parameter	Test conditions (Note 4)	Limits			Unit
			Min	Typ	Max	
$t_{PHL}(DI-DO)$ $t_{PLH}(DI-DO)$	High-to-low-level and low-to-high-level output propagation time, from Input DI to output DO	$C_L=30\text{pF}$, $R_{L1}=300\Omega$, $R_{L2}=600\Omega$			30	ns
$t_{PHL}(DS2-DO)$ $t_{PLH}(DS2-DO)$	High-to-low-level and low-to-high-level output propagation time, from Input $\overline{DS1}$, DS2 and STB to output DO				40	ns
$t_{PHL}(STB-\overline{INT})$	High-to-low-level output propagation time, from Input STB to output \overline{INT}				40	ns
$t_{PZL}(MD-DO)$ $t_{PZH}(MD-DO)$	Z-to-low-level and Z-to-high-level output propagation time, from Inputs MD, $\overline{DS1}$ and DS2 to output DO	$C_L=30\text{pF}$, $R_{L1}=300\Omega$, $R_{L2}=600\Omega$			45	ns
$t_{PHZ}(MD-DO)$ $t_{PLZ}(MD-DO)$	High-to-Z-level and low-to-Z-level output propagation time, from Inputs MD, $\overline{DS1}$ and DS2 to output DO	$C_L=30\text{pF}$, $R_{L1}=10\text{k}\Omega$, $R_{L2}=1\text{k}\Omega$			45	ns
$t_{PHL}(\overline{CLR}-DO)$	High-to-low-level output propagation time, from input \overline{CLR} to output DO	$C_L=30\text{pF}$, $R_{L1}=300\Omega$, $R_{L2}=600\Omega$			55	ns

Note 4 : Test circuit



TIMING DIAGRAMS REFERENCE LEVEL=1.5V

