Signetics

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Status	Product Specification
FAST Products	

FAST 74F604

Latch

Dual Octal Latch (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F604	7.5ns	75mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Stores 16-bit-wide Data inputs, multiplexed 8-bit outputs**
- **3-state outputs**
- **Power supply current 75mA typical**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP	N74F604N
28-Pin Plastic SOL	N74F604D

DESCRIPTION

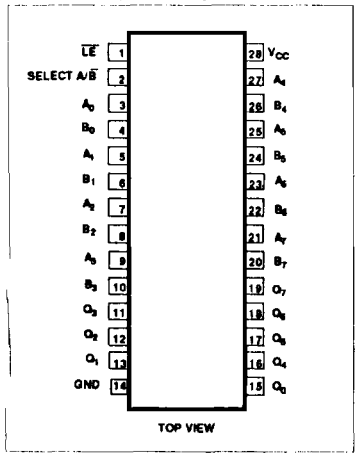
The 74F604 multiplexed latch is ideal for storing data from two input buses, A or B, and providing data from either the A or B latches to the output bus. Organized as 8-bit A and B latches, the latch outputs are connected by pairs to eight 2-input multiplexers. A Select (SELECT A/$\overline{B}$) input determines whether the A or B latch contents are multiplexed to the eight 3-state outputs. Data entered from the B inputs are selected when SELECT A/$\overline{B}$ is Low; data from the A inputs are selected when SELECT A/$\overline{B}$ is High. Data enters the latches when the Latch Enable ($\overline{LE}$) input is Low and is latched on the $\overline{LE}$ rising edge. The outputs are enabled when $\overline{LE}$ is High and disabled when $\overline{LE}$ is Low.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

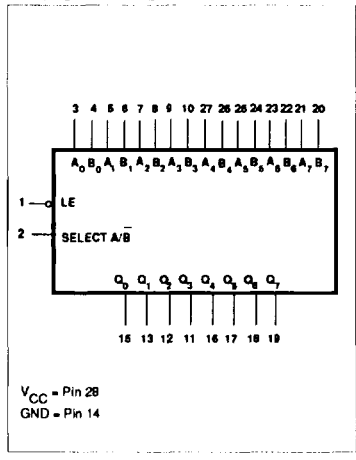
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_7, B_0-B_7	Data inputs	1.0/0.033	20μA/20μA
SELECT A/$\overline{B}$	Select input	1.0/0.033	20μA/20μA
$\overline{LE}$	Latch Enable Input (active Low)	1.0/0.033	20μA/20μA
O_0-O_7	Data outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

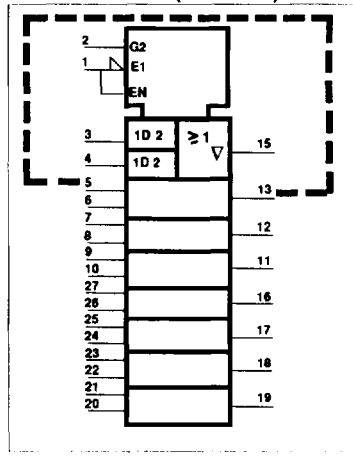
PIN CONFIGURATION



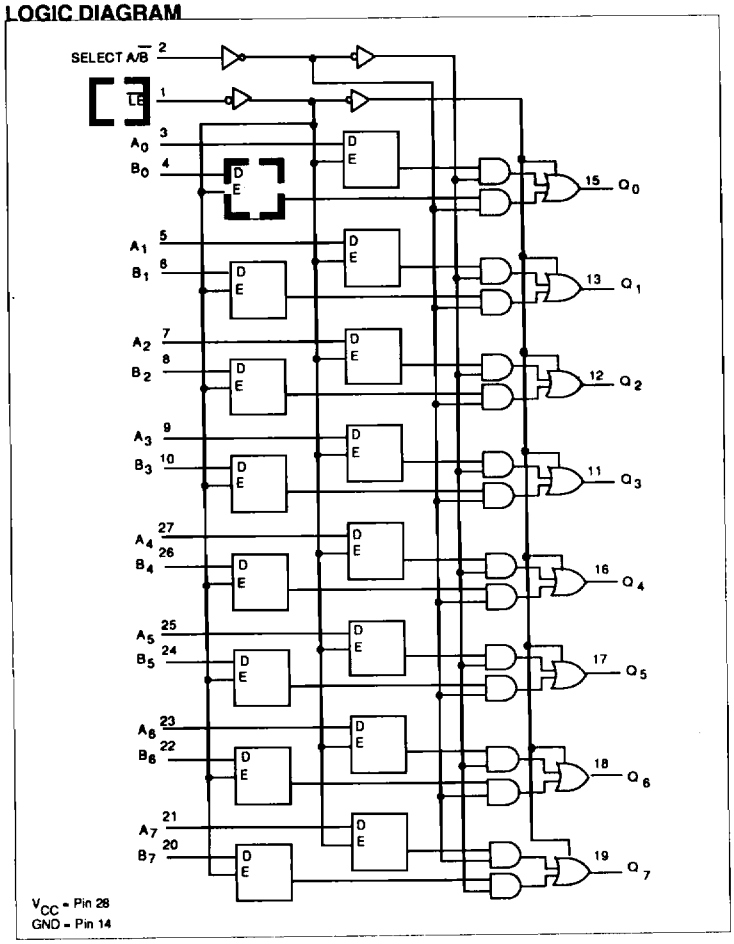
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS
A_0-A_7	B_0-B_7	SELECT A/$\overline{B}$	$\overline{LE}$	Q_0-Q_7
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z
X	X	L	H	B latched data
X	X	H	H	A latched data

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High transition

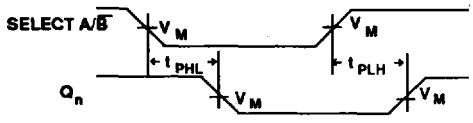
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (B latch)	Waveform 1	5.0 6.0	7.0 8.5	9.0 10.5	4.5 5.5	10.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (A latch)	Waveform 2	6.0 4.0	8.0 6.5	10.0 8.5	5.5 3.5	11.5 9.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	5.0 5.0	7.5 7.5	9.5 9.5	4.5 4.5	10.5 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 4 Waveform 5	5.0 5.0	7.0 7.0	9.5 9.5	4.5 4.5	11.0 11.0	ns

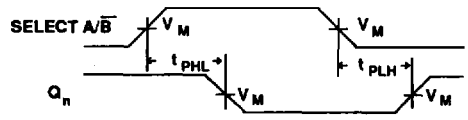
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n, B_n to $\overline{LE}$	Waveform 3	1.0 2.0			2.0 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n, B_n to $\overline{LE}$	Waveform 3	0 1.0			0 1.5		ns
t_w(L)	$\overline{LE}$ Pulse width, Low	Waveform 3	5.0			6.0		ns

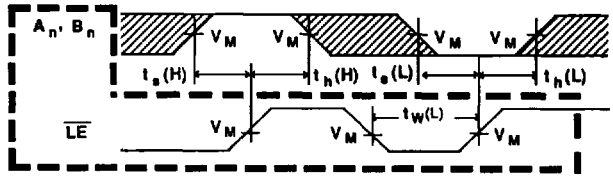
AC WAVEFORMS



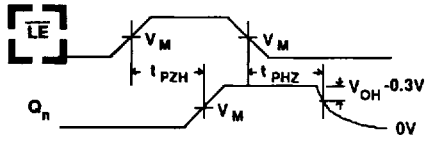
Waveform 1. Propagation Delay, SELECT A/B To Output (B latched data=Low. LE=H)



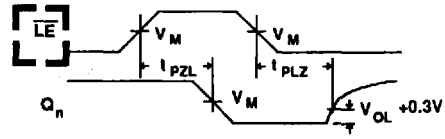
Waveform 2. Propagation Delay, SELECT A/B To Output (A latched data=Low. LE=H)



Waveform 3. Data Setup And Hold Times ,Latch Enable pulse width



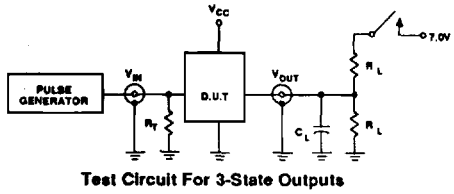
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



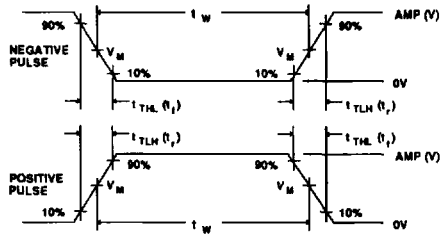
Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns