M-967 DTMF Receiver

The Teltone® M-967 tone and rotary dial decoder IC is an LSI implementation of the circuitry needed to form the heart of a DTMF or rotary dial receiver circuit. When combined with filters for separation of the dual tones, the M-967 will provide high-quality detection of DTMF signals.

The crystal-controlled time base in the M-967 accurately measures the frequencies of the tone signals, provides precise supervision of telephone hook status, and validates dial pulse digits with digital repeatability. When the decoder has validated a signal, the information is presented along with a strobe in binary. The outputs can be blanked, and separate pins are provided for * and # detection.

To operate, the M-967 requires a single 12-volt DC supply and an 895-kHz crystal or clock input (895 kHz = 3.58 MHz/4).

Features

- Decodes all 16 DTMF signals
- Contains timing and counting circuitry for loop hook status and 10 pps dial pulse decoding
- Tone-only, or mixed mode operation
- Selectable output formats
- Two inputs with hysteresis for accepting the output of a DTMF bandsplit filter
- Meets or exceeds common foreign and domestic telephone central office requirements for DTMF recognition and speech immunity

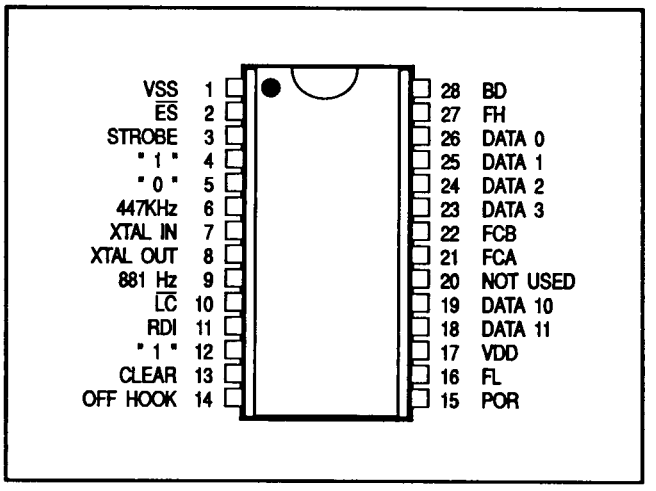

Figure 1 Pin Diagram

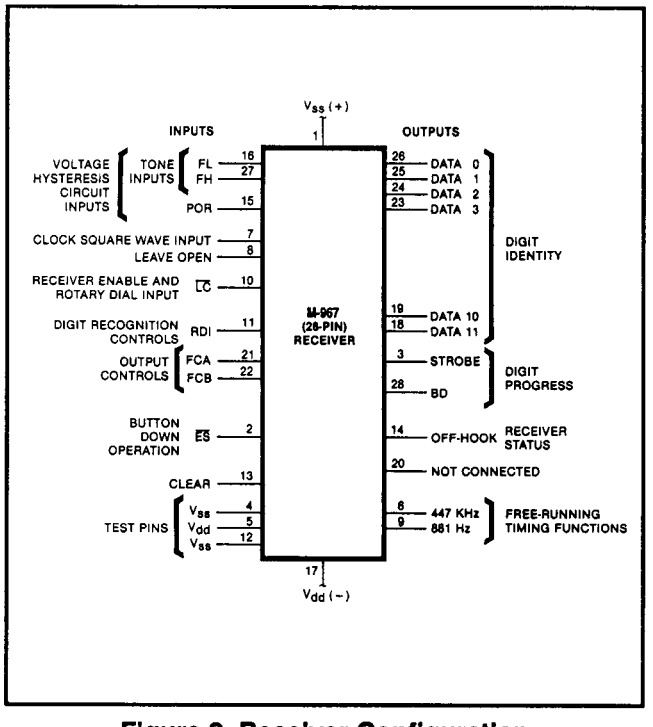

Figure 2 Receiver Configuration

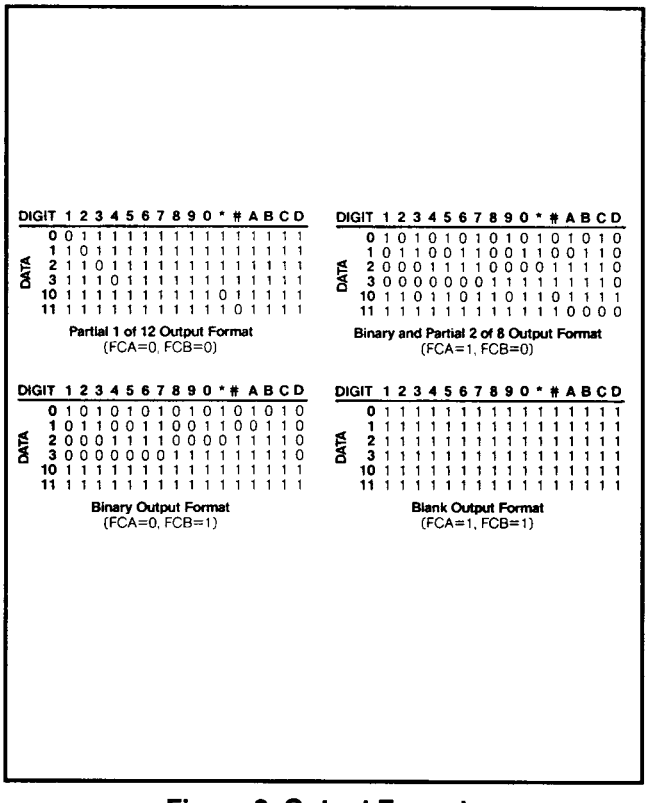

Figure 3 Output Formats

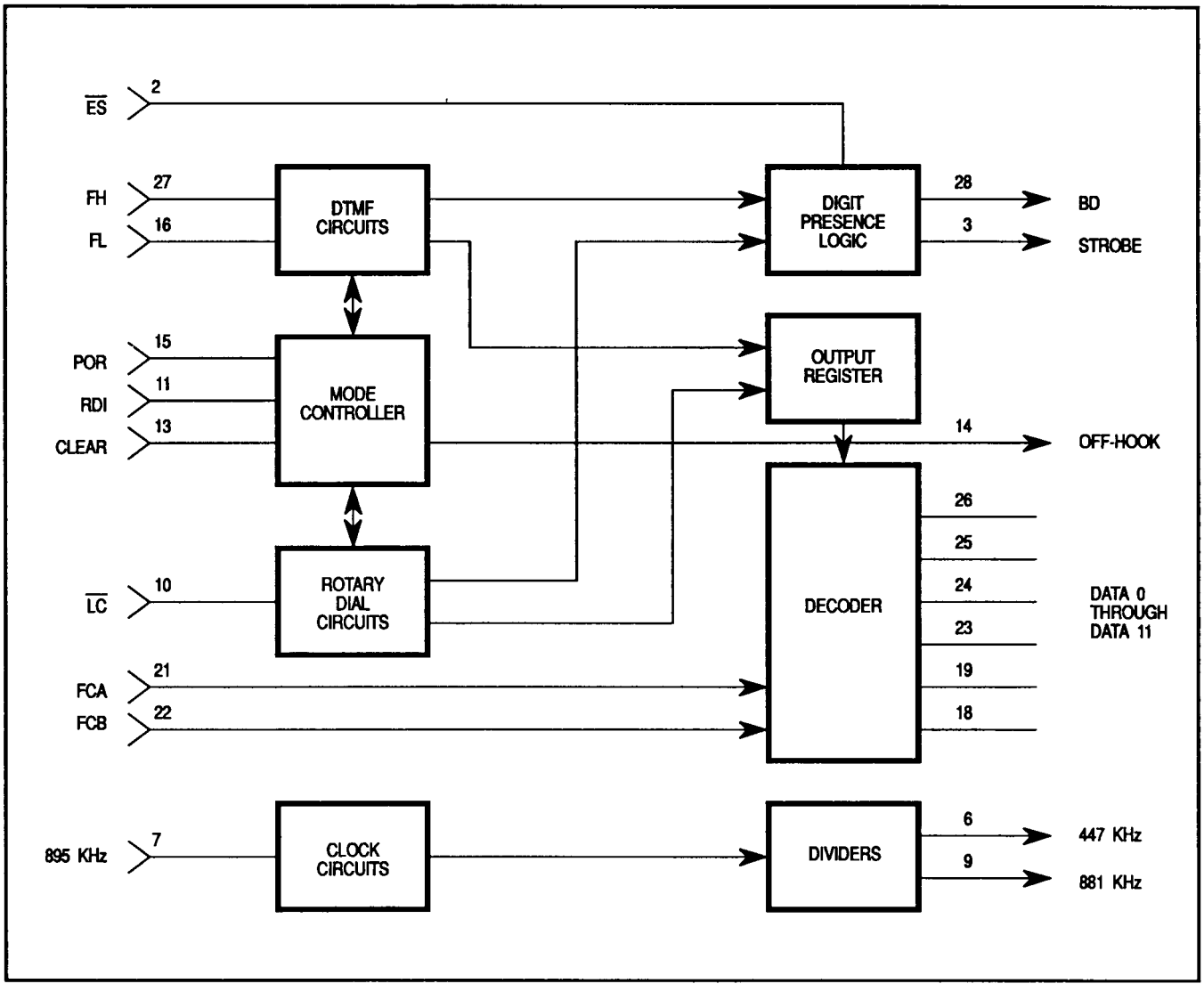

Figure 4 Block Diagram

Table 1 Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	14.5 V
Power Dissipation	600 mW
Voltage on Any Pin	$(V_2 + 0.3\ V)$ to $(V_1 - 0.3\ V)$
Storage Temperature	−40° to 150° C
Operating Temperature	0° to 70° C ambient air
Lead Soldering Temperature	260° C for 5 seconds at 0.035 inches from package

Notes:
1. Exceeding these ratings may cause permanent damage.
2. V_2 (positive supply) referenced to V_1 (negative supply). V_2 may be at ground.

Table 2 Pin Functions

Pin Number	Function	Description
1	V_{SS}	Positive power supply (V_2)
2	$\overline{ES}$	Early split not input. When pulled to logic 0 (V_1), $\overline{ES}$ enables the early tone presence (BD) output.
3	STROBE	Valid data output. When DTMF digits are being detected, STROBE goes to the logic 1 state 10 microseconds after the DATA outputs change and returns to the logic 0 state 25 milliseconds (ms) after the end of DTMF detection. When rotary dial digits are being detected, STROBE goes to logic 1 for 200 ms after the interdigital pause is recognized. To read DATA during DTMF signal presence, use the leading edge of STROBE (button-down operation). To read DATA after DTMF signal presence, use the trailing edge of STROBE (button-up operation).
4		Test input. Connect to logic 1.
5		Test input. Connect to logic 0.
6	447 kHz	50 percent duty cycle. PMOS logic level signal for external use. Actual frequency is the clock frequency divided by 2.
7	CLOCK IN	895-kHz input from the filter.
8	XTAL OUT	Not used. Leave open.
9	881 Hz	50 percent duty cycle. PMOS logic level signal for external use. Actual frequency is the clock frequency divided by 1016.
10	$\overline{LC}$	Loop current not input. $\overline{LC}$ is both a receiver enable/disable input and the rotary dial pulse input. The M-967 interprets a logic 0 as an off-hook condition, interdigital pause, or a make period. The M-967 interprets a logic 1 as an on-hook condition or break period. For DTMF operation only, $\overline{LC}$ can be connected to V_1; then, with POR connected as described below, the receiver is enabled as long as CLEAR is at logic 0.
11	RDI	Rotary dial inhibit input. For mixed DTMF and rotary dial operation, connect RDI to logic 0. For DTMF operation only, connect RDI to logic 1.
12		Test input. Connect to logic 1.
13	CLEAR	Receiver enable/disable input. A logic 1 applied to the CLEAR input instantaneously resets all detection circuits and forces the DATA outputs to the D column of the currently enabled output format (see Figure 3).
14	OFF-HOOK	Output OFF-HOOK goes to the logic 1 state 100 ms after $\overline{LC}$ is pulled to logic 0. OFF-HOOK goes to the logic 0 state 300 ms after LC is pulled to logic 1.
15	POR	Power-on reset, receiver enable/disable input. A 0.01 µf capacitor connected to V_2 and POR causes POROUT to go to logic 1 (V2) for approximately 10 ms after power is applied. This pulse resets all detection circuits and forces the DATA outputs to the D column of the currently enabled output format (see Figure 3).
16	FL	FLSQ input from the filter.
17	V_{dd}	Negative power supply (V_1).
18	DATA 11	Data outputs. See Figure 3 for the outputs associated with each output format. A DTMF digit is output when it has persisted for 35 ms. A rotary dial digit is output when an interdigital pause is recognized.
19	DATA 10	
20		Not used.
21 and 22	FCA and FCB	Format control A and B inputs. As shown in Figure 3, FCA and FCB determine the DATA output format. FCA and FCB can also be used as a data strobe. By holding both inputs at logic 1, all data outputs will remain at logic 1 until FCA and/or FCB are poulled to logic 0.
23	DATA 3	See description to DATA 10 and 11.
24	DATA 2	
25	DATA 1	
26	DATA 0	
27	FH	FHSQ input from the filter.
28	BD	Button down output. When enabled by $\overline{ES}$ being at logic 0, BD goes to the logic 1 state within 16 ms after a tone pair is detected. BD then returns to the logic 0 state 25 ms after the tone pair ends.

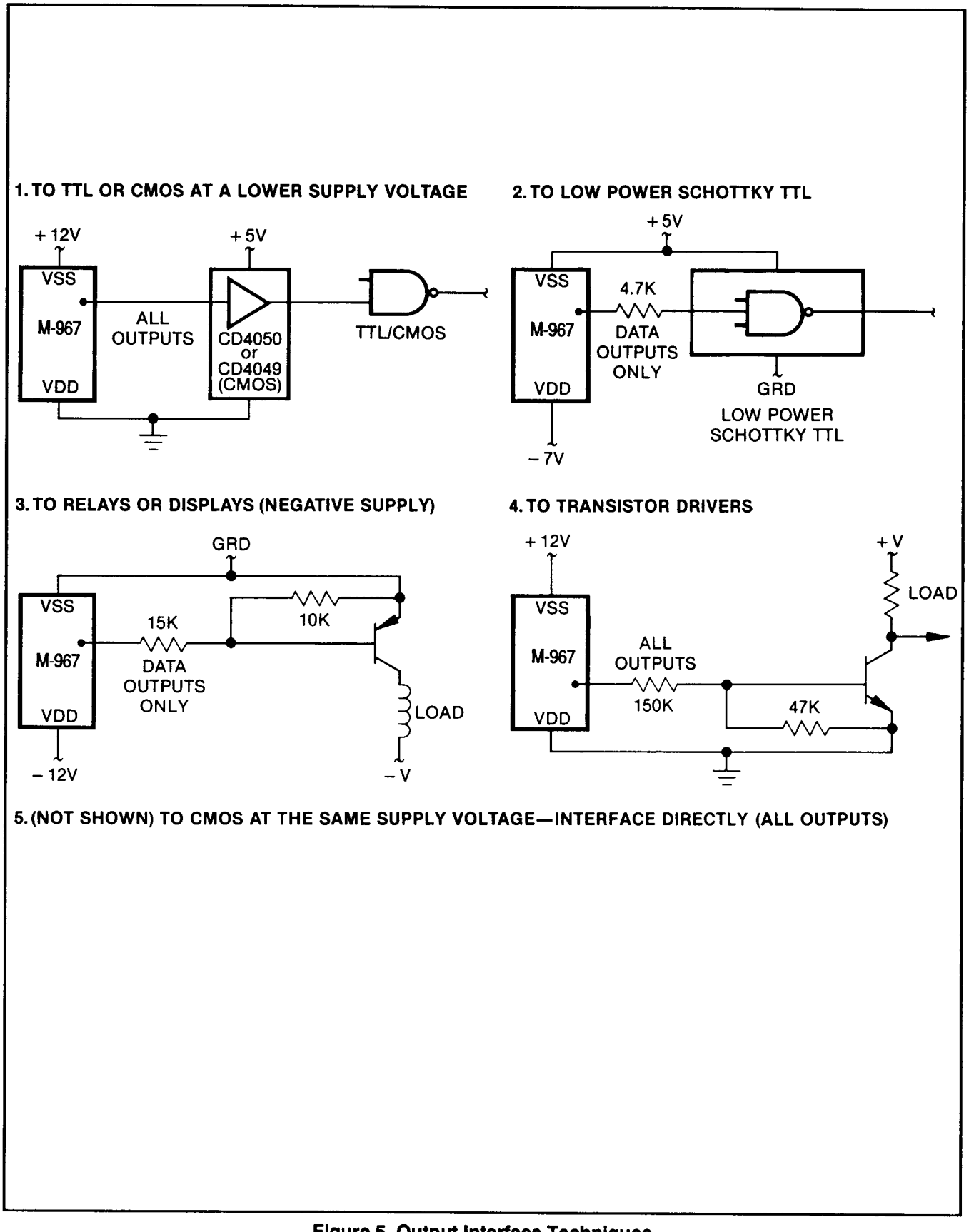

Figure 5 Output Interface Techniques

Table 3 DC Electrical Characteristics

	Parameter	Min	Typ	Max	Units	Conditions
Supply Requirements	Supply Voltage	+11	+12	+14.5	V	V_2 referenced to V_1 (Note 1)
	Ripple Voltage			250	mV	Measured peak-to-peak at 120 Hz
	Supply Current		25	35	mA	14.5 V at 0°C
Logic Inputs	Logic 0 Level			V_1 + 3.2	V	
	Logic 1 Level	V_2 – 2.5			V	
	Capacitance			15	pF	
	Input Current (Note 2)			50	μA	
Analog Inputs	Logic 0 Threshold	0.57 (ΔV)	0.65 (ΔV)	0.73 (ΔV)	V	ΔV = $V_2 - V_1$
	Logic 1 Threshold	0.43 (ΔV)	0.35 (ΔV)	0.27 (ΔV)	V	ΔV = $V_2 - V_1$
	Capacitance			15	pF	
	Input Current (Note 2)			±50	μA	
Data Outputs	Logic 0 Current Sink			1	mA	Output at V_1 + 7 V
	Logic 1 Current Source			100	μA	Output at V_2 – 2 V
Non-Data Outputs	Logic 0 Current Sink			100	μA	Output at V_1 + 2 V
	Logic 1 Current Source			100	μA	Output at V_2 – 2 V

Notes:
1. V_2 more positive than V_1. V_2 may be at ground.
2. The load current must be sourced or sunk to drive an input to its opposite state.

Table 4 AC (Dynamic) Electrical Characteristics

	Parameter	Min	Typ	Max	Units	Conditions
FL and FH Inputs	Signal Detect Time	27		30	ms	
	Interdigital Pause Detect Time (Note 1)	26		34	ms	
	Interdigital Pause Reject Time (Note 1)	26			ms	
	Signal Detect Bandwidth	– 1.5% – 2 Hz		+ 1.5% + 2 Hz	Hz	Of each nominal DTMF frequency
	Signal Reject Bandwidth	– 3.5%		+ 3.5%	Hz	Of each nominal DTMF frequency
Inputs Other Than FL and FH	Pulse Width Required to Reset with CLEAR or POR Inputs			25	μs	
	Off-Hook Recognition	95	100	105	ms	$\overline{LC}$ at Logic 0
	Off-Hook Blanking (Note 2)	285	300	315	ms	$\overline{LC}$ at Logic 0
	Break Recognition	24.5		29.5	ms	$\overline{LC}$ at Logic 1
	Make Recognition	7	9	11	ms	$\overline{LC}$ at Logic 0
	End of Digit Recognition	95	100	105	ms	$\overline{LC}$ at Logic 0
	Rotary Interdigital Blanking	190	200	210	ms	
	On-Hook Recognition	290	300	310	ms	$\overline{LC}$ at Logic 1
Available Frequencies	447.433 kHz Pulse Width	2.232	2.234	2.237	μs	
	881 Hz Pulse Width	0.567	0.568	0.569	ms	
	20 Hz Pulse Width (Note 3)	24.95	24.98	25	ms	

Notes:
1. The Interdigital Pause Detect Time is that interval of loss of tones after which the return of the valid tone pair is considered a new digit. The Interdigital Pause Reject Time is the interval a valid tone pair can be interrupted without being treated as a new digit when it returns.
2. Off-Hook Blanking is the delay between $\overline{LC}$ going to logic 0, from being at logic 1 longer than 300 ms, and enabling the digit detection circuits.
3. 40-pin receivers only.

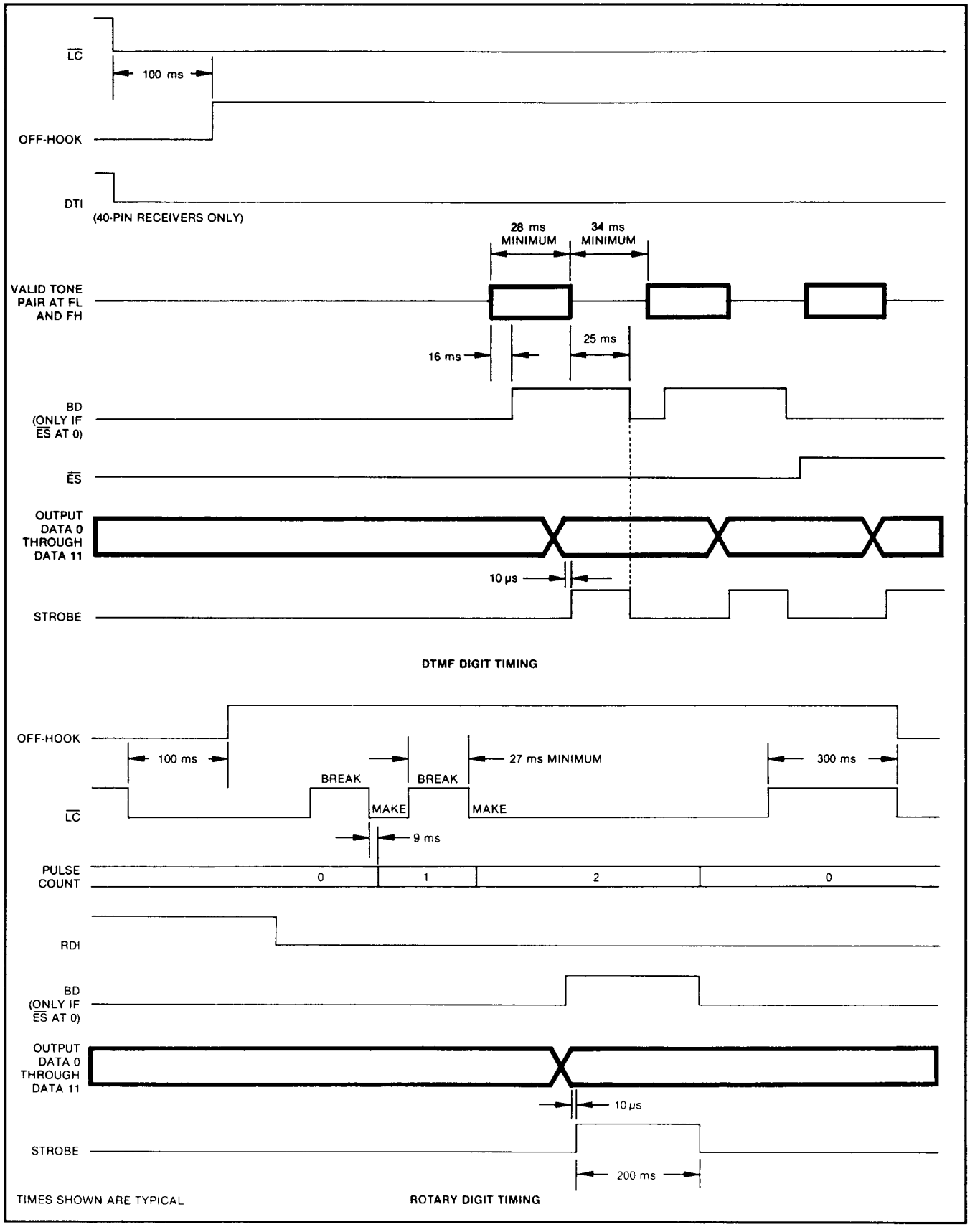

Figure 6 Timing Diagram

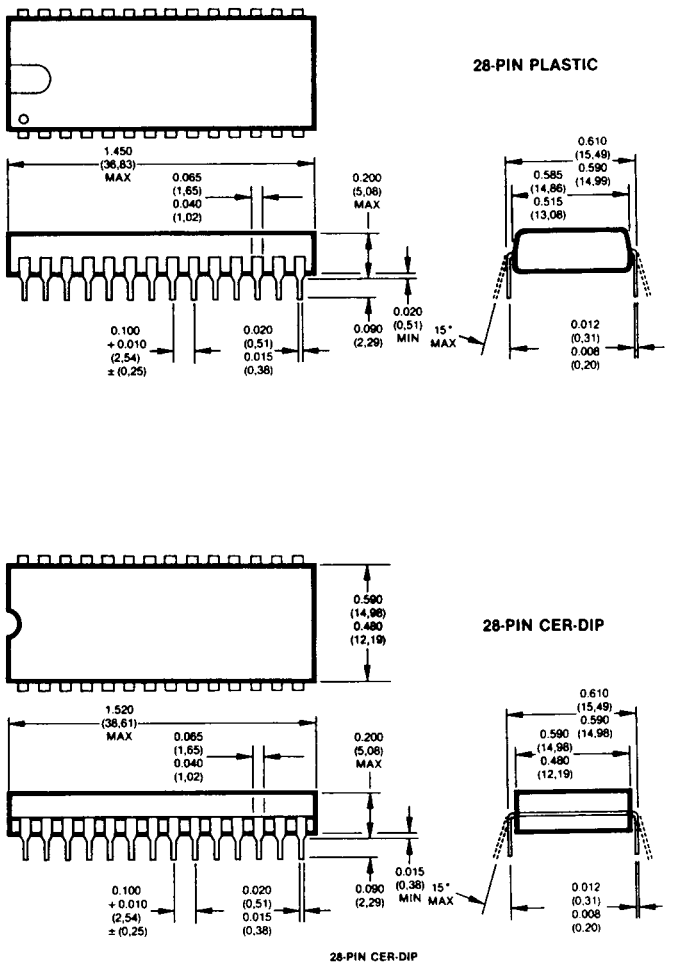

Figure 7 Package Dimensions