SDH/SONET STM4/OC12 optical receiver TZA3000

FEATURES

- Low equivalent input noise, typically 3.5 pA/√Hz
- Wide dynamic range, typically 1 μA to 1.5 mA
- On-chip low-pass filter. The bandwidth can be varied between 370 and 600 MHz using an external resistor. Default value is 470 MHz.
- Differential transimpedance of 1.8 MΩ
- On-chip AGC (Automatic Gain Control)
- PECL (Positive Emitter-Coupled Logic) or CML (Current-Mode Logic) compatible data outputs
- LOS (Loss-Of-Signal) detection
- LOS threshold level can be adjusted using a single external resistor
- On-chip DC offset compensation
- Single supply voltage from 3.0 to 5.5 V
- Bias voltage for PIN diode.

APPLICATIONS

- Digital fibre optic receiver in short, medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wideband RF gain block.

DESCRIPTION

The TZA3000 optical receiver is a low-noise transimpedance amplifier with AGC plus a limiting amplifier designed to be used in SDH/SONET fibre optic links. The TZA3000 amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3000HL	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1
TZA3000U	naked die	die in waffle pack carriers; die dimensions 1.58 × 1.58 mm	–

BLOCK DIAGRAM

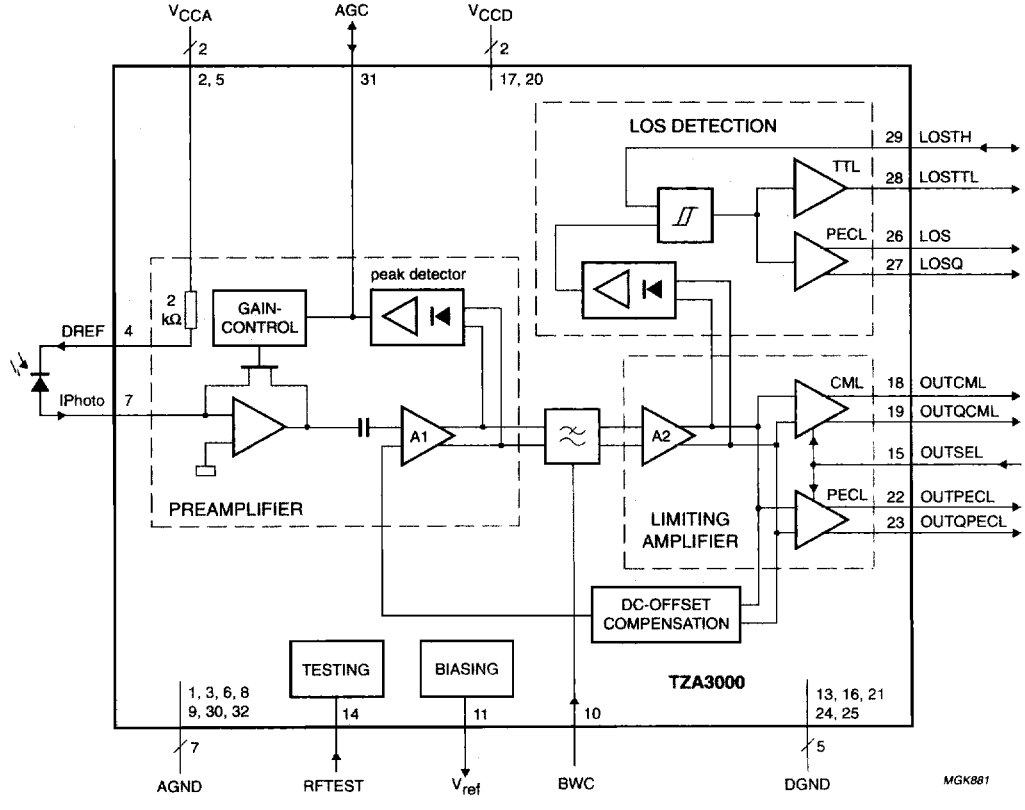

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
AGND	1	ground	analog ground
V_{CCA}	2	supply	analog supply voltage
AGND	3	ground	analog ground
DREF	4	analog output	bias voltage for PIN diode (V_{CCA}); cathode should be connected to this pin
V_{CCA}	5	supply	analog supply voltage
AGND	6	ground	analog ground
IPhoto	7	analog input	current input; connect the anode of PIN diode to this pin; DC bias level is 800 mV, one diode voltage above ground
AGND	8	ground	analog ground
AGND	9	ground	analog ground
BWC	10	analog input	bandwidth control pin; default bandwidth is 470 MHz; a resistor should be connected between V_{ref} (pin 11) and BWC (pin 10) to decrease bandwidth, or between BWC (pin 10) and AGND to increase bandwidth
V_{ref}	11	analog output	band gap reference voltage; nominal value approximately 1.2 V
SUB	12	substrate	substrate pin; to be connected to AGND
DGND	13	ground	digital ground
RFTEST	14	analog input	test pin; not used in application; not connected
OUTSEL	15	CMOS input	output select pin; when OUTSEL is HIGH, CML data outputs are active and PECL data outputs are disabled; OUTSEL is pulled LOW if left unconnected, PECL data outputs will then be active and CML data outputs disabled
DGND	16	ground	digital ground
V_{CCD}	17	supply	digital supply voltage
OUTCML	18	CML output	CML data output; OUTCML goes HIGH when current flows into IPhoto (pin 7)
OUTQCML	19	CML output	CML compliment of OUTCML (pin 18)
V_{CCD}	20	supply	digital supply voltage
DGND	21	ground	digital ground
OUTPECL	22	PECL output	PECL data output; OUTPECL goes HIGH when current flows into IPhoto (pin 7)
OUTQPECL	23	PECL output	PECL compliment of OUTPECL (pin 22)
DGND	24	ground	digital ground
DGND	25	ground	digital ground
LOS	26	PECL output	PECL-compatible LOS detection pin; LOS output is HIGH when the input signal is below the user programmable threshold level
LOSQ	27	PECL output	PECL compliment of LOS
LOSTTL	28	TTL output	CMOS-compatible LOS detection pin; the LOSTTL output is HIGH when the input signal is below the user programmable threshold level
LOSTH	29	analog I/O	pin for setting input threshold level; nominal DC voltage is V_{CCA} – 1.5 V; threshold level set by connecting an external resistor between LOSTH and V_{CCA} or by forcing a current into LOSTH; default value for this resistor is 86 kΩ
AGND	30	ground	analog ground
AGC	31	analog I/O	AGC monitor voltage; the internal AGC circuit can be disabled by applying an external voltage to this pin
AGND	32	ground	analog ground

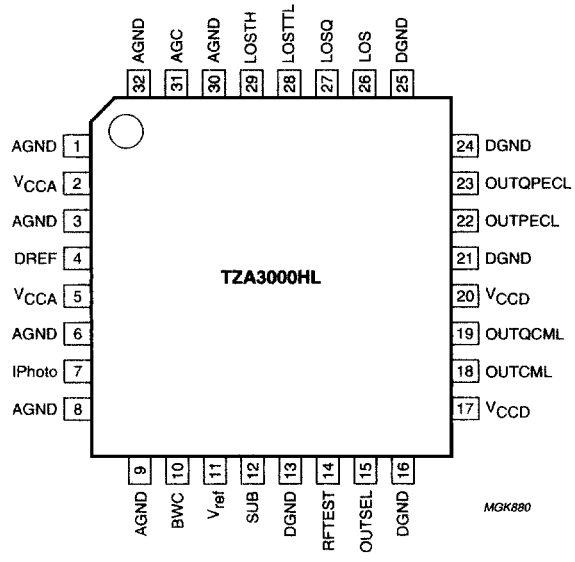

Fig.2 Pin configuration.