F10416
256 x 4-Bit Programmable Read Only Memory

F10K ECL Product

Description

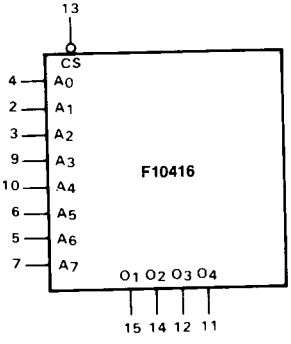
The F10416 is a 1024-bit field Programmable Read Only Memory (PROM), organized 256 words by four bits per word. It is designed for high-speed control, mapping, code conversion, and logic replacement. The device includes full on-chip address decoding, non-inverting Data output lines, and an active-LOW Chip Select line for easy memory expansion. The device is manufactured with all bits in the logic-HIGH state. Programmed bits will furnish LOW levels at corresponding outputs.

- **Address Access Time - 20 ns Max**
- **Chip Select Access Time - 8.0 ns Max**
- **Chip Select Input and Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation - 0.56 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{CS}$	Chip Select Input (Active LOW)
A_0-A_7	Address Inputs
O_1-O_4	Data Outputs

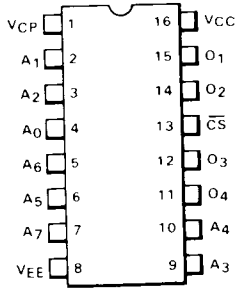
Logic Symbol



V_{CP} = Pin 1
V_{CC} = Pin 16
V_{EE} = Pin 8

Connection Diagram

16-Pin DIP (Top View)



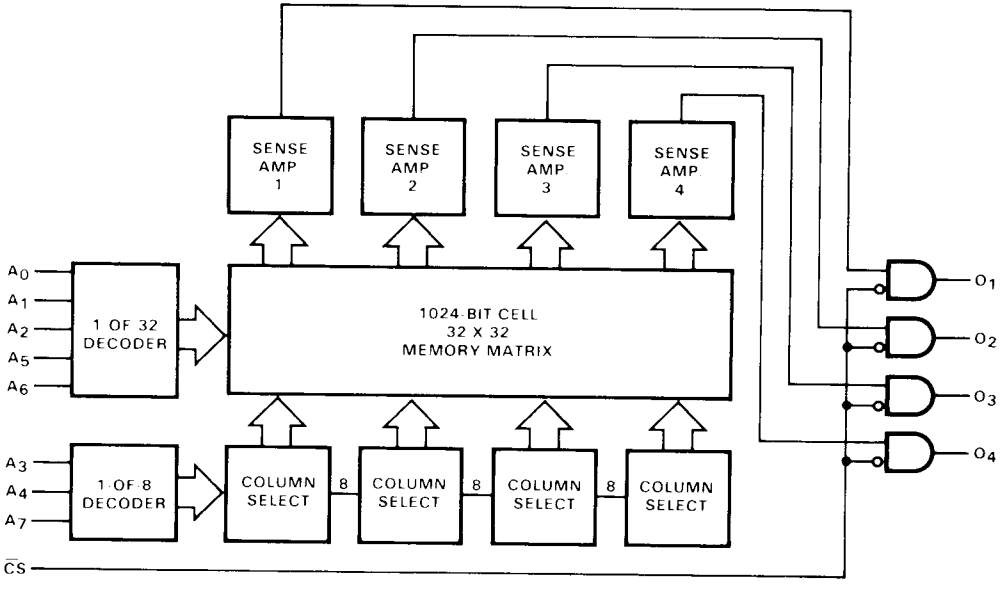
Notes

V_{CP} (Pin 1) is connected to the Programmer (+10.5 V) during programming only; otherwise, it should be grounded.
The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package.

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6D	DC
Plastic DIP	9B	PC
Flatpak	3L	FC

Logic Diagram



Functional Description

The F10416 is a fully decoded bipolar field programmable read only memory organized 256 words by four bits per word. An unterminated emitter-follower output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F10416 devices can be tied together. An external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is off.

One Chip Select ($\overline{CS}$) input is provided for memory array expansion up to 512 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of $\overline{CS}$ from the address without increasing address access time. The device is enabled when $\overline{CS}$ is LOW. When the device is disabled ($\overline{CS}$ = HIGH), all outputs are forced LOW.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_7 inputs, the chip is selected and data is valid at the outputs after t_{AA}.

In the unprogrammed state the outputs are HIGH. To program LOW levels follow the procedure outlined in the *Programming Specifications* table.

Programming

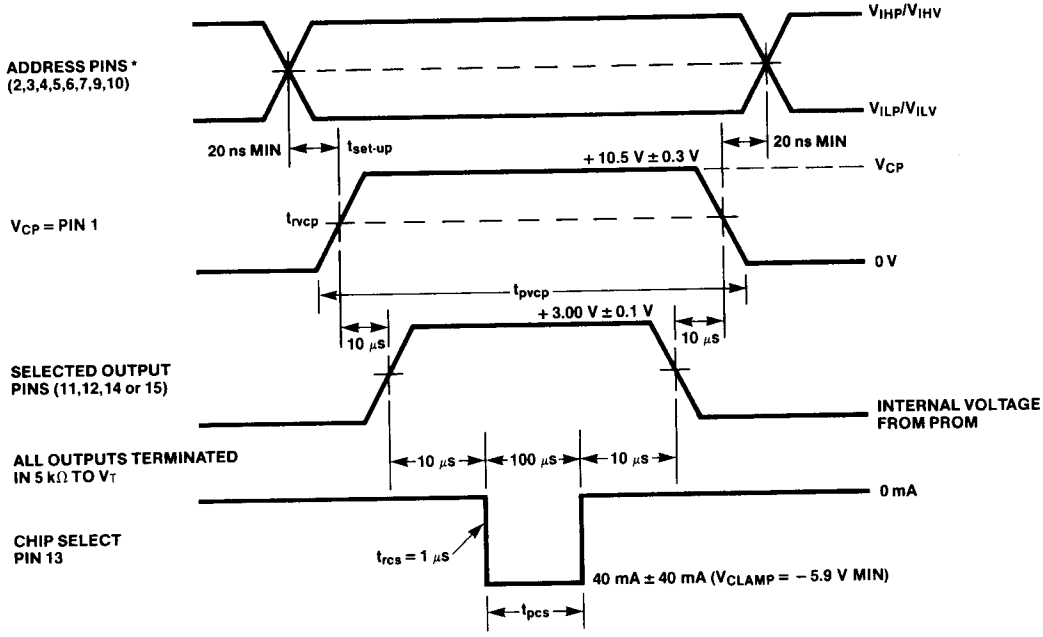
The F10416 is manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown below. One may build a programmer to satisfy the specifications or purchase any of the commercially available programmers which meet these specifications.

Programming Sequence

1. Apply power to the part: V_{CC} = pin 16 = GND; V_{EE} = pin 8 = −5.2 V ± 5%.
2. Terminate all outputs (pins 11, 12, 14 and 15) with 5 kΩ resistors to V_{TT} = −2.0 V. Note: all input pins, including $\overline{CS}$, have internal 50 kΩ pull-down resistors to V_{EE}.

3. Select the word to be programmed by applying the appropriate voltage levels, as shown in the *Programming Specifications* table, to the Address pins (2, 3, 4, 5, 6, 7, 9 and 10).
4. After the address levels are set raise V_{CP} = Pin 1 from 0 V to +10.5 V ± 0.3 V.
5. After V_{CP} has reached its HIGH level, select the bit to be programmed by applying a HIGH level of +3.0 V ± 0.1 V to the output associated with it, *i.e.*, pins 11, 12, 14 or 15. Only one bit (output) at a time may be selected for programming. Uncommitted outputs are terminated as outlined in 2.
6. After the HIGH level (+3.0 V) has been established at the selected output pin, source a current of −40 mA ± 4 mA out of the Chip Select input (pin 13) to program the selected bit; this applied current pulse which is 100 μs wide and has an approximate rise time of 1 μs is to be furnished by a current sink which clamps at V_{CLAMP} = −5.9 V.
7. To verify a LOW in the bit just programmed follow this sequence:
   (a) Remove current pulse from $\overline{CS}$ pin.
   (b) Remove applied voltage from selected output pin.
   (c) Lower V_{CP} from HIGH level to GND.
   (d) Keep same address but change its levels to normal ECL levels as outlined in the *Programming Specifications* table.
   (e) Enable the chip by applying a LOW level (V_{IL}) to $\overline{CS}$ (pin 13), or leave it open.
   (f) Sense the level at the selected output pin; a LOW level indicates successful programming whereas a HIGH level is a fail indication; in the latter case reprogramming of the bit can be attempted up to a maximum of eight times.
8. To program other bits in the memory repeat steps 3 through 7.

Programming Timing Sequence



*Input pins A_1 and A_7 cannot be lower than $V_{IL(min)}$.

Programming Specifications

Symbol	Characteristic	Min	Recommended Value	Max	Unit	Comment
V_{CC}	Power Supply		0		V	
V_{EE}		-5.46	-5.2	-4.94	V	
V_{TT}	Termination Voltage		-2.0		V	Applied to all outputs
V_{IH}	Chip Select (V_{CLAMP})	-0.1	0	+0.1	V	Max Current is 40 mA during programming
V_{IL}		-5.9	-5.2		V	
V_{IHP}	Address Input Threshold	-0.1	0	+0.1	V	Programming levels
V_{ILP}		-3.1	-3.0	-2.9	V	
V_{IHV}	Address Input Threshold	-0.88	-0.87	-0.86	V	Verify levels
V_{ILV}		-1.76	-1.75	-1.74	V	
V_{CP}	Program Setup Pulse	10.2	10.5	10.8	V	
V_{OP}	Programming Pulse	2.9	3.0	3.1	V	Applied to output to be programmed
I_{CS}	Chip Select Programming Current	36	40	44	mA	At V_{CLAMP} = -5.9 V Min on the Chip Select pin
t_{pcs}	Chip Select Programming Pulse	50	100	180	μs	
t_{rcs}	Chip Select Programming Pulse Rise Time	0.5	1.0	2.0	μs	
t_{pvcp}	V_{CP} Programming Pulse	90	140	220	μs	
t_{rvcp}	V_{CP} Programming Rise Time	0.5	1.0	2.0	μs	
t_{setup}	Setup Time	20			ns	Start time of V_{CP} pulse after address is selected

Guaranteed Operating Ranges

Part Number	Supply Voltage (V_{EE})			Ambient Temperature T_A
	Min	Typ	Max	
F10416XC	−5.46 V	−5.2 V	−4.94 V	−30°C to +85°C

X = Package Type

DC Characteristics: V_{EE} = −5.2 V, V_{CC} = GND, T_A = −30°C to +85°C unless otherwise specified[1]

Symbol	Characteristic	Min	Typ	Max	Unit	T_A	Condition	
V_{OH}	Output HIGH Voltage	−1060 −960 −890		−890 −810 −700	mV	−30°C +25°C +85°C	$V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$	Loading is 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1890 −1850 −1825		−1675 −1650 −1615	mV	−30°C +25°C +85°C		
V_{OHC}	Output HIGH Voltage	−1080 −980 −910			mv	−30°C +25°C +85°C	$V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage			−1655 −1630 −1595	mV	−30°C +25°C +85°C		
V_{IH}	Input HIGH Voltage	−1205 −1105 −1035		890 810 700	mV	−30°C +25°C +85°C	Guaranteed HIGH signal for All Inputs	
V_{IL}	Input LOW Voltage	−1890 −1850 −1825		−1500 −1475 −1440	mV	−30°C +25°C +85°C	Guaranteed LOW signal for All Inputs	
I_{IH}	Input HIGH Current			200	μA	−30°C to +85°C	$V_{IN} = V_{IH(max)}$	
I_{IL}	Input LOW Current, $\overline{CS}$	0.5		150	μA	+25°C	$V_{IN} = V_{IL(min)}$	
I_{EE}	Power Supply Current	−140	−110		mA	+25°C	All Inputs and Outputs Open	

AC Characteristics: V_{EE} = −5.2 V ± 5%, V_{CC} = GND, Output Load 50 Ω to −2.0 V, T_A = −30°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_{AA}	Address Access Time[2]		11	20	ns	Measured at 50% Points of both Input and Output
t_{ACS}	Chip Select Access Time		4.0	8.0	ns	Measured at 50% Points of both Input and Output

1. See 10K Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.