Product Preview

Video Measurement Graphic Monitor On-Screen Display - 24 (VMOSD-24)

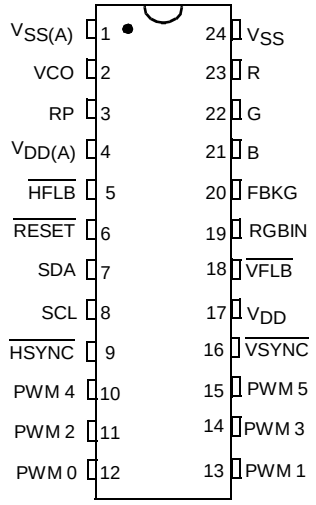
CMOS

MC141580P2

P SUFFIX
PLASTIC PACKAGE
CASE 724-03

ORDERING INFORMATION
MC141580P2 Plastic Dip

PIN ASSIGNMENT



This is a high performance HCMOS device designed to interface with a micro controller unit to allow colored symbols or characters to be displayed onto CRT monitor. Because of the large number of fonts, 512 fonts including 496 standard fonts and 16 multi-color fonts, VMOSD-24 is suitable to be adopted for the multi-language monitor application especially. Its on-chip PLL allows both multiscan operation and self generation of system timing. It also minimizes the MCU's burden through its built-in RAM. By storing a full screen of data and control information, this device has a capability to carry out 'screen-refresh' without any MCU supervision.There is a high speed timing measurement module that designed to measure the timing relationship among HSYNC, VSYNC, HFLB, and RGBIN. The resolution of video measurement will relate to the resolution setting of internal OSD PLL clock. Three resolutions: 768,896 or 1024 dot per line mode are avaliable for video measurement. MCU can get the measurement data through M-Bus write/read operation as well. Programmable hatch pattern generator is added for production burn-in test.

Since there is no clearance between characters, special graphics oriented characters can be generated by combining two or more character blocks. The full OSD menu is formed of 15 rows x 30 columns which can by freely positioned on anywhere of the monitor screen by changing vertical or horizontal delay.

There are 6 PWM DAC channels for external digital to analog control. Each PWM DAC channel is composed of an 8 bit register which contains a 5 bit PWM in MSB portion and a 3 bit binary rate multiplier (BRM) in LSB portion.

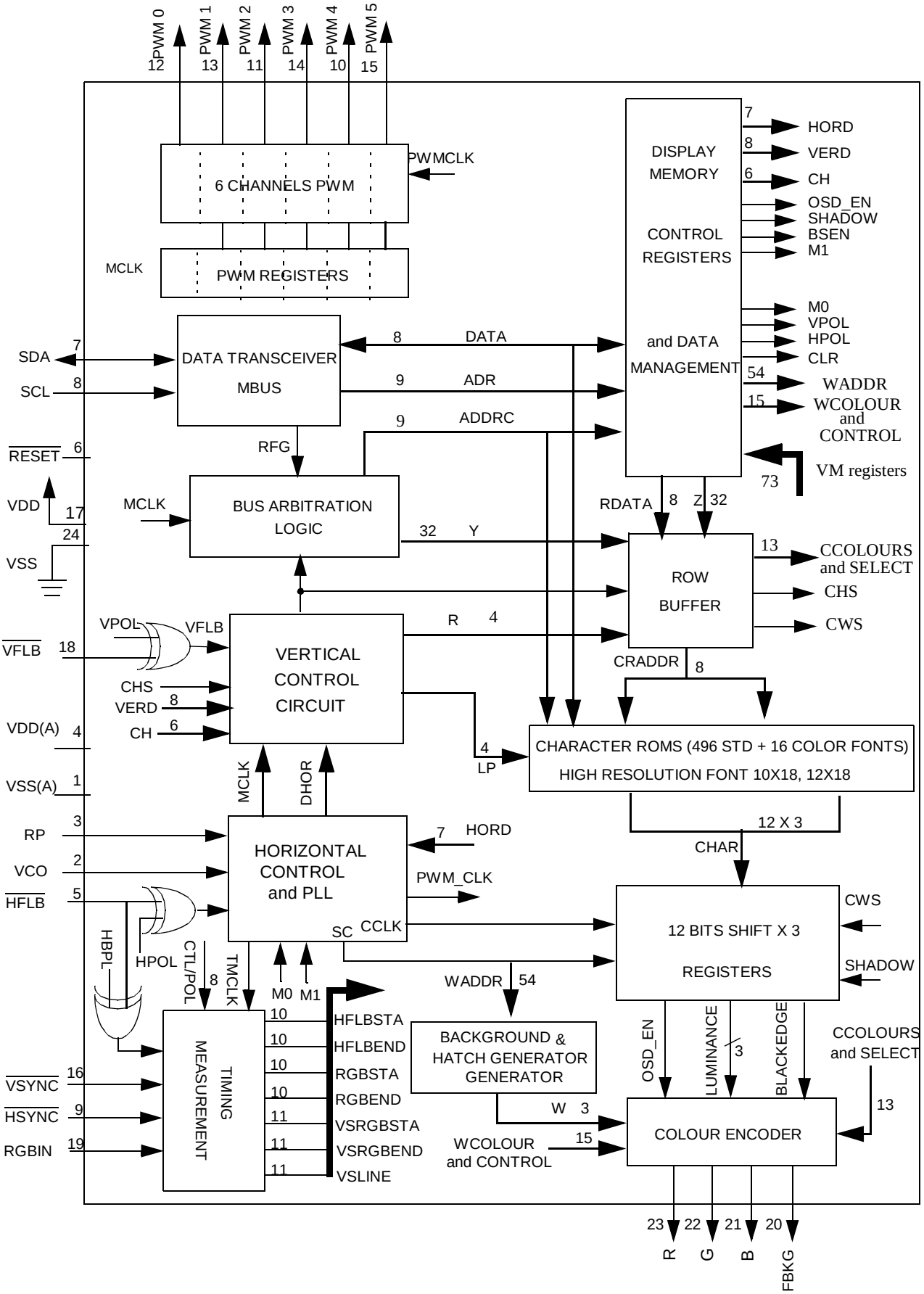
Special functions such as character background color, blinking, four-level windows with programmable shadowing, row double height and double width, programmable vertical height of character and row-to-row spacing, and full-screen erasing and Fade-In/Fade-Out are also incorporated. There are 8 color selections for any individual character display.Totally 512 Fonts Including 496 Standard Fonts and 16 Multi-Color Fonts.

- Timing measurement among HSYNC, VSYNC, HFLB, and RGBIN.
- 10x18 or 12x18 Font Matrix Selection
- Three resolutions for video measurement: 768, 896 and 1024 Dots/Line
- 768 dot per line for OSD menu display
- Wide Operating Frequency: max. 135KHz for Monitor
- Internal PLL generates a Wide-Ranged System Clock(Max 110MHz)
- 6 Channels Synchronous PWMs with 8-bit Resolution
- Fully Programmable Character Array of 15 Rows by 30 Columns
- 8-Color Selection for Characters/Windows
- 7-Color Selection for Characters background
- Fancy Fade-In/Fade-Out Effects
- Programmable Height of Character to Meet Multi-Sync Requirement
- Auto Height Scaling Function
- Row To Row Spacing Control to Avoid Expansion Distortion
- Four Programmable Windows with Overlapping Capability
- Character/Symbol Blinking Function
- Programmable Vertical and Horizontal Positioning for Display Centre
- M_BUS (IIC) Interface with Write Address $7A, Read Address $7B

- This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS Voltage Referenced to V_{SS}

Symbol	Characteristic	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to + 7.0	V
V_{in}	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
Id	Current Drain per Pin Excluding V_{DD} and V_{SS}	10	mA
Ta	Operating Temperature Range	0 to 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristic	Min	Typ	Max	Unit
VDD	Supply Voltage at Pin 17, Voltage Referenced to Pin24 VSS.	+4.75	—	+5.25	V
VDD(A)	Supply Voltage at Pin 4, Voltage Referenced to Pin24 VSS.	+4.75	—	+5.25	V
T_a	Ambient Temperature Range for Operation	0	—	+80	°C

AC ELECTRICAL CHARACTERISTICS(UNDER RECOMMENDED OPERATING CONDITIONS)

Symbol	Characteristic	Min	Typ	Max	Unit
	Output Signal (R, G, B, FBKG and INT) C_{load} = 10 pF				
t_r	Rise Time (Refer to Figure 1)	—	—	4.5	ns
t_f	Fall Time (Refer to Figure 1)	—	—	4.5	ns
$f_{\overline{HFLB}}$	$\overline{HFLB}$ Input Frequency at pin5	—	—	135	KHz
f_{PLL}	Internal PLL Clock(VMOSD display dot clock)	—	—	110	MHz
t_{setup}	Setup time between $\overline{HFLB}$ and $\overline{HSYNC}$ (for video measurement)	600	—	—	ns

***NOTE:1. Internal PLL Clock frequency is given by the following formula : $f_{PLL} = f_{\overline{HFLB}}$ x VMOSD resolution. Please also refer to Row 15, Coln15 register for reference to the resolution setting.**

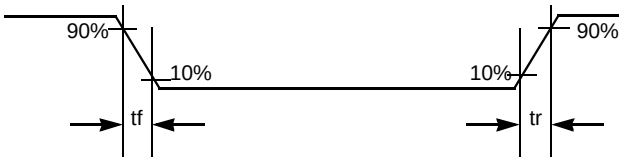


Figure 1. Switching Characteristics

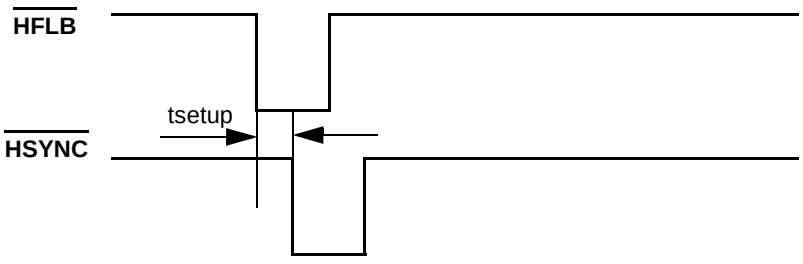


Figure 2. Setup time between $\overline{HFLB}$ and $\overline{HSYNC}$ for video measurement

DC CHARACTERISTICS(UNDER RECOMMENDED OPERATING CONDITIONS)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage I_{out} = – 5 mA	V_{DD} – 0.8	—	—	V
V_{OL}	Low Level Output Voltage I_{out} = 5 mA	—	—	V_{SS} + 0.4	V
 V_{IL} V_{IH}	Digital Input Voltage (Not Including SDA and SCL) Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in M_BUS Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
I_{II}	High-Z Leakage Current (R, G, B and FBKG)	– 10	—	+ 10	µA
I_{II}	Input Current (Not Including RP, VCO, R, G, B and FBKG)	– 10	—	+ 10	µA
I_{DD}	Supply Current (No Load on Any Output) at V_{DD}=5.0V	—	—	+ 35	mA
LVR	Low Voltage Reset	3.0	—	3.6	V

M_BUS AC TIMING (UNDER RECOMMENDED OPERATING CONDITIONS)

Symbol	Characteristics	Min	Typ	Max	Unit
f_{SCL}	SCL Clock Frequency for write operation(HFLB frequency >= 29KHz) SCL Clock Frequency for read operation(HFLB frequency >= 29KHz)	— —	— —	400 100	kHz kHz
t_{BUF}	BUS free time between a STOP and START condition	500	—	—	ns
t_{HDSTA}	START condition hold time	500	—	—	ns
t_{LOW}	SCK low period	400	—	—	ns
t_{HIGH}	SCK high period	400	—	—	ns
t_{SUSTA}	START condition set-up time(for repeated START condition only)	100	—	—	ns
t_{HDDAT}	Data hold-time	250	—	—	ns
t_{SUDAT}	Data set-up time	100	—	—	ns
t_{SUSTO}	Set-up time for STOP condition	500	—	—	ns

NOTES: For the M_BUS can run at full speed and meet above specifiction, the $\overline{\text{HFLB}}$ signal should be applied to pin5 not less than 60ms in advance of M_BUS communication. This 60ms timing is for the stablizing of VMOSD internal PLL CLK.

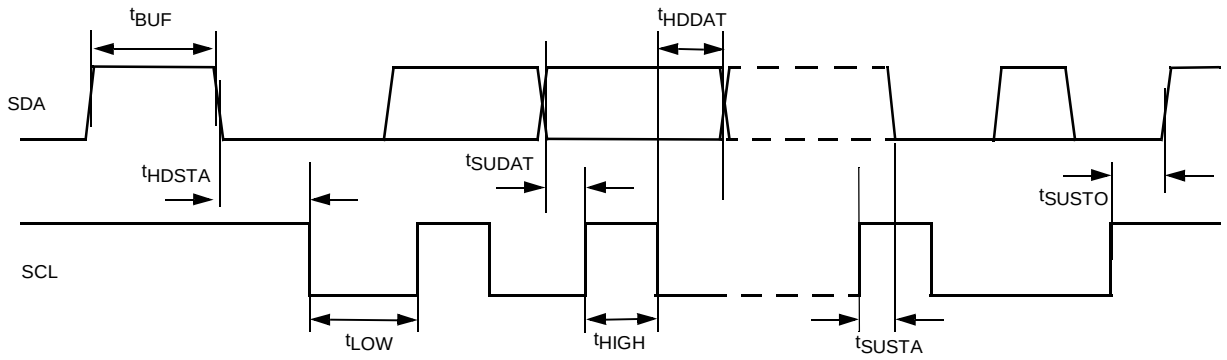


Figure 3. Timing Definition for M_BUS

PIN DESCRIPTION

VSS(A) (Pin 1)

This pin provides the signal ground to the PLL circuitry. Analog ground for PLL is separated from digital ground for optimal performance.

VCO (Pin 2)

A dc control voltage input to regulate an internal oscillator frequency. See the Application Diagram for the application values used.

RP (Pin 3)

An external RC network is used to bias an internal VCO to resonate at the specific dot frequency. The maximum voltage at Pin 3 should not exceed 3.5 V at any condition. See the Application Diagram for the application values used.

$V_{DD(A)}$ (Pin 4)

A positive 5 V dc supply for PLL circuitry. Analog power for PLL is separated from digital power for optimal performance.

$\overline{\text{HFLB}}$ (Pin 5)

This pin inputs a negative polarity horizontal synchronize signal pulse to phase lock into an internal system clock generated by the on-chip VCO circuit. The HFLB signal input to this pin must be present during the BUS communication. Please also refer to "BUS operation" section.

$\overline{\text{RESET}}$ (Pin 6)

An active low signal will reset ROW15 and ROW16 control registers. Refer to Control Registers section for default settings. A proper RC network have to be tighted to this pin to ensure the device initialize properly during power up. Refer to the application diagram.

SDA (Pin 7)

Data and control message are being transmitted to this chip from a host MCU via M_bus systems. This wire is configurated as a uni-directional data line. (Detailed description of protocols will be discussed in the M_BUS section).

SCL (Pin 8)

A separate synchronizing clock input from the transmitter is required for M_Bus protocol. Data is read at the rising edge of each clock signal.

$\overline{\text{HSYNC}}$ (Pin 9)

This HSYNC input pin is used as signal reference for horizontal timing measurement.

PWM 4 (Pin 10)

Channel 4 of the PWM.

PWM 2 (Pin 11)

Channel 2 of the PWM.

PWM 0 (Pin 12)

Channel 0 of the PWM.

PWM 1 (Pin 13)

Channel 1 of the PWM.

PWM 3 (Pin 14)

Channel 3 of the PWM.

PWM 5 (Pin 15)

Channel 5 of the PWM.

$\overline{\text{VSYNC}}$ (Pin 16)

This VSYNC input pin is used as signal reference for vertical timing measurement.

V_{DD} (Pin 17)

This is the power pin for the digital logic of the chip.

$\overline{\text{VFLB}}$ (Pin 18)

Similar to Pin 5, this pin inputs a negative polarity of vertical synchronize signal to synchronize the vertical control circuit.

RGBIN (Pin 19)

This CMOS level signal input should be the OR signal of R, G. B video.

FBKG (Pin 20)

This pin will output a logic high while displaying characters or windows. It is defaulted to high impedance state after power on, or when there is no output. An external 10 kΩ resistor pulled low is recommended to avoid level toggling caused by hand effect when there is no output.

B,G,R (Pin 21, 22, 23)

VMOSD-24 color outputs in CMOS level to the host monitor. They are active high push-pull outputs. These pins could be configured to either high impedance state or logic low voltage when OSD display is being disabled. Please refer to "TRIC" bit description in "REGISTER" section for more detailed. These pin are in high impedance state after power on.

V_{SS} (Pin 24)

This is the ground pin for the digital logic of the chip.

SYSTEM DESCRIPTION

MC141580P2 is a full screen memory architecture. Refresh is done by the built-in circuitry after a screenful of display data has been loaded in through the serial bus. Only changes to the display data need to be input afterward.

Serial data, which includes screen mapping address, display information, and control messages, are being transmitted via M_BUS. Data is first received and saved in the MEMORY MANAGEMENT CIRCUIT in the Block Diagram. Meanwhile, the VMOSD-24 is continuously retrieving the data and putting it into a ROW BUFFER for display and refreshing, row after row. During this storing and retrieving cycle, a BUS ARBITRATION LOGIC will patrol the internal traffic, to make sure that no crashes occur between the slower serial bus receiver and fast 'screen-refresh' circuitry. After the full screen display data is received through the serial communication interface, the link can be terminated if change on display is not required.

The bottom half of the Block Diagram constitutes the heart of this entire system. It performs all the VMOSD-24 functions such as programmable vertical length (from 16 lines to 63 lines), display clock generation (which is phase locked to the

incoming horizontal sync signal at Pin 5 $\overline{\text{HFLB}}$), and multiple windowing.

The video measurement module is composed of two types of timing measurement, horizontal and vertical. In horizontal measurement, the $\overline{\text{HSYNC}}$ is the reference signal. As PLL clock is the certain multiple of $\overline{\text{HSYNC}}$ frequency, i.e. 768, 896 and 1024, the measurements for $\overline{\text{HFLB}}$ and RGBIN are all based on the PLL clock and store the desired parameters, like Dhbsta, Dhbend, Drgbsta, and Drgbend, into the corresponding read only registers. In vertical measurement, the $\overline{\text{VSYNC}}$ pulse is the reference signal and the $\overline{\text{HSYNC}}$ is the counting clock. The module will count the line number from the specified edge of $\overline{\text{VSYNC}}$ to the first RGBIN active line and the last RGBIN active line and store these two parameters, Dvrgbsta and Dvrgbend, into read only registers. All these measurements commence at the following $\overline{\text{VSYNC}}$ pulse after the VMEN bit is set, complete the measurement after one vertical frame, and set the DONE flag in the STATUS read only register. The horizontal measurement for RGBIN will store the minimum start location and the maximum ending location in one vertical frame into registers. All of the input signals for timing measurement are polarity programmable, so the different phase measurement can be obtained.

The RSTF flag in STATUS register is used for MCU to be aware of any incidental reset to the VMOSD chip and then to re-initialize all the settings of this chip. It is cleared after first time read.

COMMUNICATION PROTOCOLS

BUS Operation

The operating clock for M_Bus derives from system dot clock. Internal PLL is using to generate the dot clock base on the $\overline{\text{HFLB}}$ input frequency where the dot clock is equal to 768/896/1024x$f_{\overline{\text{HFLB}}}$ in 768/896/1024 modes respectively. To achieve stable operation of M_Bus and meet below specifications, $\overline{\text{HFLB}}$ must be presented and the PLL locks to $\overline{\text{HFLB}}$ properly. Refer to Application Diagram for PLL bias circuit.

M_BUS Serial Communication

This is a two-wire serial communication link that is fully compatible with the IIC bus system. It consists of SDA bidirectional data line and SCL clock input line. Data is sent from a transmitter (master), to a receiver (slave) via the SDA line, and is synchronized with a transmitter clock on the SCL line at the receiving end. The maximum data rate is limited to 400 kbps for write operation and 100kbps for read operation. The default chip address is $7A for write operation and $7B for read operation. Please refer to the M_Bus specification for detail timing requirement.

Operating Procedure

Figure 3 shows the M_BUS transmission format. The master initiates a transmission routine by generating a START condition, followed by a slave address byte. Once the address is properly identified, the slave will respond with an ACKNOWLEDGE signal by pulling the SDA line LOW during the ninth SCL clock. Each data byte which then follows must be eight bits long, plus the ACKNOWLEDGE bit, to make up nine bits together. Appropriate row and column address information and display data can be downloaded sequentially in one of the three transmission formats described in DATA TRANSMISSION FORMATS SECTION. In the cases of no ACKNOWLEDGE or completion of data transfer, the master will generate a STOP condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent in order to activate the VMOSD-24 circuitry of MC141580P2, so that the received information can then be displayed.

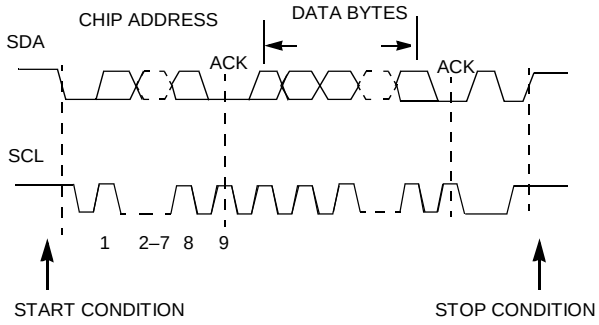


Figure 4. M_BUS Format

DATA TRANSMISSION FORMATS

After the proper identification by the receiving device, data train of arbitrary length is transmitted from the Master. As mentioned above, two register blocks, display registers, attribute/control registers, need to be programmed before the proper operation. Basically, these three areas use the similar transmission protocol. Only two bits of the row/segment byte are used to distinguish the programming blocks.

There are three transmission formats, from (a) to (c) as stated below. The data train in each sequence consists of row/seg address (R), column/line address (C), and data informations (I). In format (a), each display information data have to be preceded with the corresponding row/seg address and column/line address. This format is particular suitable for updating small amount of data between different row. However, if the current information byte has the same row/seg address as the one before, format (b) is recommended. For a full screen pattern change which requires massive information update or during power up situation, most of the row/seg and column/line address on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. It sends the RAM starting row/seg and column/line addresses once only, and then treat all subsequent data as data information. The row/seg and column/line addresses will be automatically incremented internally for each information data from the starting location.

Based on the different programming areas, the detail transmission protocol is described below respectively.

(I) Display Register Programming

The data transmission formats are:

(a) R - > C- > I -> R - > C - > I - > . . . . . .

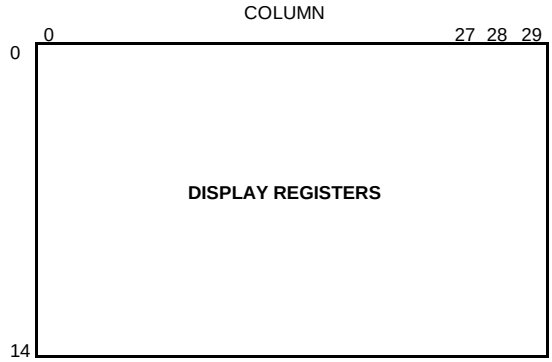
(b) R - > C - > I - > C - > I - > C - > I. . . . . .

(c) R - > C - > I - > I - > I - > . . - > I_{dummy} - > I_{dummy} - > I - > I. .

NOTE: - R means row byte.
- C means column byte.
- I means data byte.
- In format (c), two dummy data bytes (col 30, col 31) have to be inserted after the last data byte (col 29) at the end of each row, before the first data byte of the next row.

To differentiate the display row address from attribute area when transferring data, the most significant three bits are set to '100' to represent display row address, while '00X' for column address used in format (a) or (b) and '01X' for column address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

Figure 5. Data Packet for Display Data



ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	0	0	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 6. Address Bit Patterns for Display Data

(II) Attribute/Control Register Programming

The data transmission formats are similar with that in display data programming:

(a) R - > C- > I -> R - > C - > I - > . . . . . .

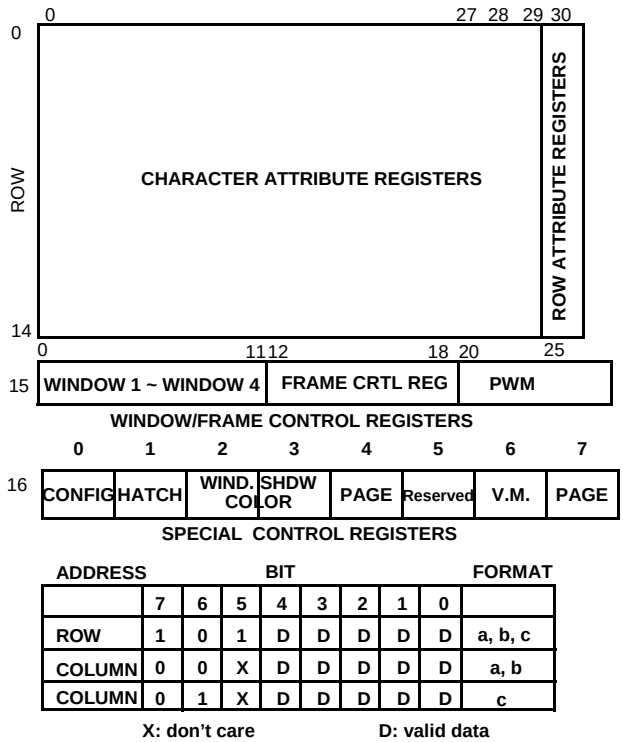
(b) R - > C - > I - > C - > I - > C - > I. . . . . .

(c) R - > C - > I - > I - > I - > . . - > $I_{row\ attr.}$ - > I_{dummy} - > I - > I. .

NOTE: - R means row byte.
- C means column byte.
- I means data byte.
- In format (c), one dummy data byte(col 31) has to be inserted after the row attribute data byte (col 30) at end of each row, before the first character attribute data byte of the next row.

To differentiate the row address for attribute/control registers from display area when transferring data, the most significant three bits are set to '101' to represent the row address of the attribute/control registers, while '00X' for column address used in format (a) or (b) and '01X' for column address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

Figure 7. Data Packet for Attribute/Control Data



ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	0	1	D	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 8. Address Bit Patterns for Attribute/Control Data

MEMORY MANAGEMENT

All the internal programmable area can be divided into two parts including (1) Display Registers (2) Attribute/Control Registers. Please refer to the following two figures for the corresponding memory map.

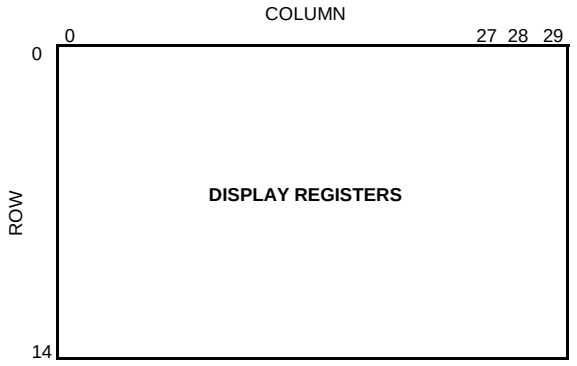


Figure 9. Memory Map of Display Registers

Internal display RAM are addressed with row and column (coln) number in sequence. As the display area is 15 rows by 30 columns, the related display registers are also 15 by 30. The space between row 0 and coln 0 to row 14 and coln 29 are called Display registers, with each contains a character/symbol address corresponding to display location on monitor screen. And each register is 8-bit wide to identify the selected character/symbol out of 256 ROM fonts.

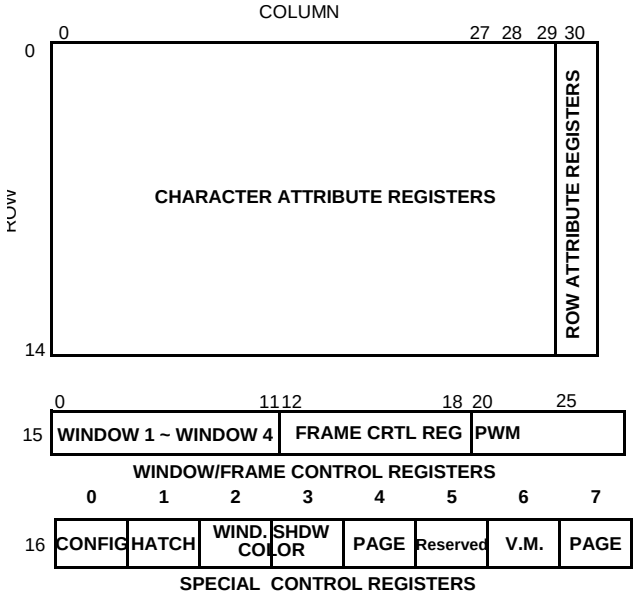


Figure 10. Memory Map of Attribute/Control Registers

Besides the font selection, there is 3-bit attribute associated with each symbol to identify its color and 3-bit to define its background. Because of 3-bit attribute, each character can select any color out of 8 independently on the same row. as well as background. Every data row associate with one attribute register, which locate at coln 30 of their respective rows, to control the characters display format of that row such as the character blinking, color intensity, character double height and character double width function. In addition, other control registers are located at row 15 such as window control, frame function control registers. Four window control registers for each of four windows together with four frame control registers occupy the first 19 columns of row 15 space. These control registers will be described on the "REGISTERS" section. ROW 16, COL 0 - 7 contain special function registers for pattern generation, windows color shadow, video measurement and page ROM selection.

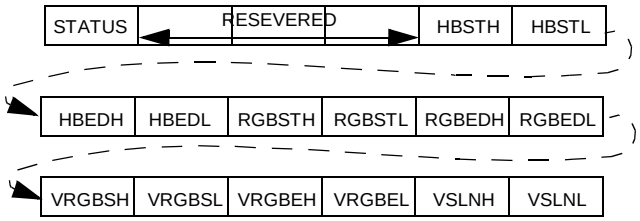
User should handle the internal display RAM address location with care especially for those rows with double length alphanumeric symbols. For example, if row n is destined to be double height on the memory map, the data displayed on screen row n and n+1 will be represented by the data contained in the memory address of row n only. The data of next row n+1 on the memory map will appear on the screen of n+2 and n+3 row space and so on. Hence, it is not necessary to throw in a row of blank data to compensate for the double row action. User needs to take care of excessive row of data in memory in order to avoid over running the limited number of row space on the screen.

There is difference for rows with double width alphanumeric symbols. Only the data contained in the even numbered columns of memory map will be shown, the odd numbered columns will be ignored and not disclosed.

DATA READ FORMATS

After the read operation calling address $7B is recognized by the slave VMOSD-24, all the read only registers of VMOSD-24 are transmitted out to the SDA line in the sequence as shown below.

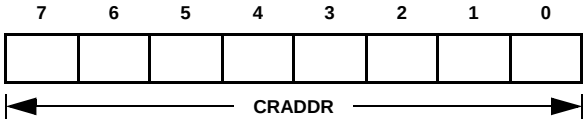
Figure 11. IIC Registers Read Sequence



REGISTERS

(I) Display Register

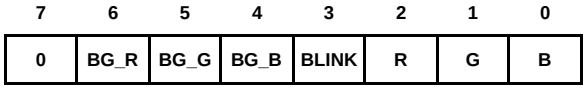
Display Register (Row 0~14, Coln 0~29)



Bit 7-0 CRADDR - This eight bits address one of the 256 logical address characters or symbols resided in the character ROM . This 256 character ROM is compose of Base Bank($00-3F), Bank A, Bank B and Bank C. Base Bank is fixed($00-$3F), Bank A is the first page 64-ROM(address $3F-$7F), Bank B is the second page 64-ROM(address $80-$BF) and Bank C is the third page 64-ROM(address $C0-$FF). Total addressable ROM is 256 out of 512 physical ROM. Pages(Page 0 to Page6) in Bank A, Bank B and Bank C can be selected by Page Selection Register at ROW16 COL 4 and ROW16 COL7.

(II) Attribute Registers

Character Attribute Register (Row 0~14, Coln 0~29)



Bit 7 Reserved. Set "0" for operation.

Bit 6-4 These three bits define the color of the background for the correspondent characters. If all three bits are clear, no background will be shown(transparent). Therefore, total seven background colors can be selected.

Bit 3 BLINK - The blinking effect will be active on the corresponding character if this bit is set to 1. The blinking frequency is approximately one time per second (1Hz) with fifty-fifty duty cycle at 80Hz vertical scan frequency.

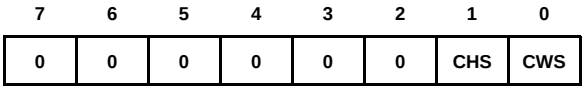
Bit 2-0 These three bits are the color attribute to define the color of the associated character/symbol.

Table 1. The Character/Window/Shadow Color Selection

	R	G	B
Black	**0**	**0**	**0**
Blue	**0**	**0**	**1**
Green	**0**	**1**	**0**
Cyan	**0**	**1**	**1**
Red	**1**	**0**	**0**
Magenta	**1**	**0**	**1**
Yellow	**1**	**1**	**0**
White	**1**	**1**	**1**

Note:The above color selection can also be applied for character background except that when RBG=000, the background will be transparent instead of black.

Row Attribute Register (Row 0~14, Coln 30)



Bit 7-2 Reserved. Set "0" for operation.

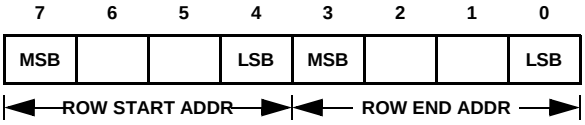
Bit 1 CHS - It determines the height of a display symbol. When this bit is set, the symbol is displayed in double height.

Bit 0 CWS - Similar to bit 1, character is displayed in double width, if this bit is set.

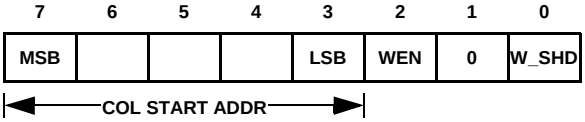
(III) Window/Control/Frame Register

Window 1 Registers

Row 15 Coln 0



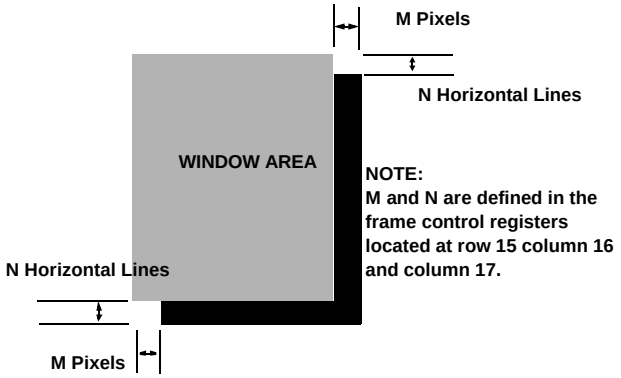
Row 15 Coln 1



Bit 2 WEN - It enables the window 1 generation if this bit is set.

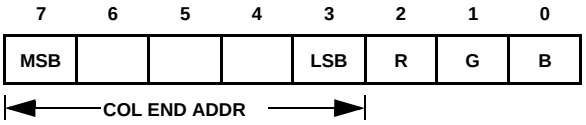
Bit 1 Reserved. Set this bit to "0" for normal operation.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 1 shadowing. When the window is active, the right M pixels and lower N horizontal scan lines will output black shadowing. The width/height of window shadow, number of M/N, is defined in the frame control registers located at row 15 column 16 and 17. See the following figure and the related frame control register for detail.



Window Shadowing

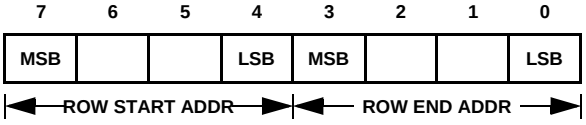
Row 15 Coln 2



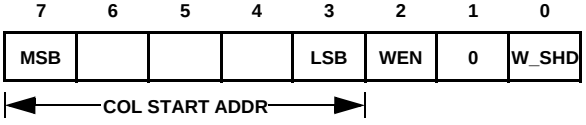
Bit 2-0 R, G and B - Controls the color of window 1. Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 2 Registers

Row 15 Coln 3



Row 15 Coln 4

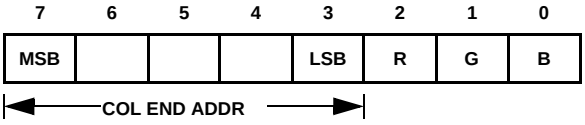


Bit 2 WEN - It enables the window 2 generation if this bit is set.

Bit 1 Reserved. Set this bit to "0" for normal operation.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 2 shadowing.

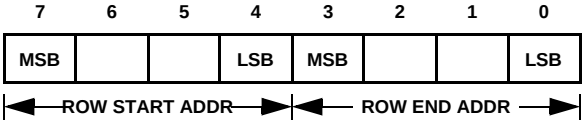
Row 15 Coln 5



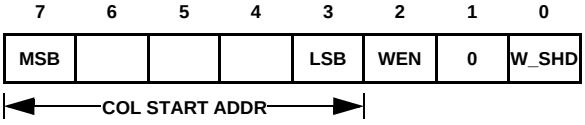
Bit 2-0 R, G and B - Controls the color of window 2.Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 3 Registers

Row 15 Coln 6



Row 15 Coln 7

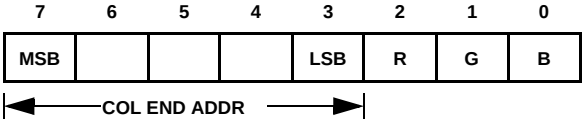


Bit 2 WEN - It enables the window 3 generation if this bit is set.

Bit 1 Reserved. Set this bit to "0" for normal operation.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 3 shadowing.

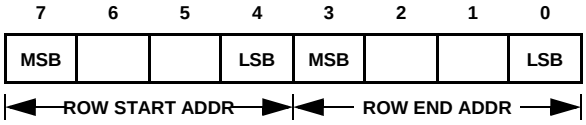
Row 15 Coln 8



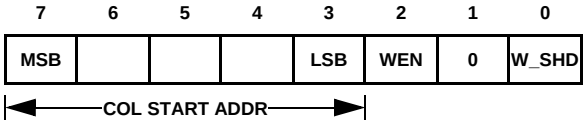
Bit 2-0 R, G and B - Controls the color of window 3.Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 4 Registers

Row 15 Coln 9



Row 15 Coln 10

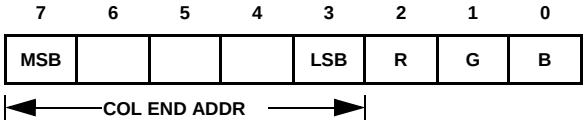


Bit 2 WEN - It enables the window 4 generation if this bit is set.

Bit 1 Reserved. Set this bit to "0" for normal operation.

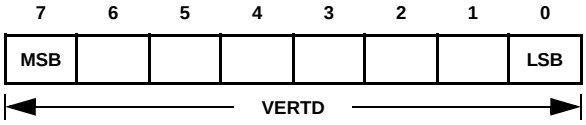
Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 4 shadowing.

Row 15 Coln 11



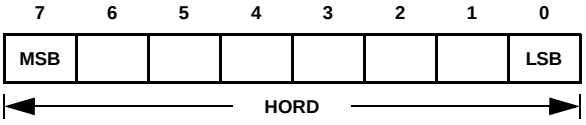
Bit 2-0 R, G and B - Controls the color of window 4.Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Vertical Delay Control Register Row 15 Coln 12



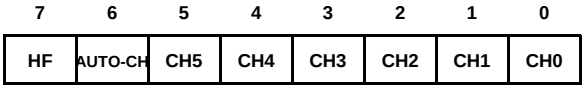
Bit 7-0 VERTD - These 8 bits define the vertical starting position. Total 256 steps, with an increment of eight horizontal lines per step for each field. Its value can't be zero anytime. The default value of it is 4.

Horizontal Delay Control Register Row 15 Coln 13



Bit 7-0 HORD - Horizontal starting position for character display. 8 bits give a total of 256 steps and each increment represents 5 or 6 dots(10x18 or 12x18 font) movement shift to the right on the monitor screen. The movement of each step is base on half character size. The default value is 15.

Character Height Control Register Row 15 Coln 14



Bit 7 HF - High Frequency Bit. Set this bit to 1 for better performance if the incoming HFLB signal is higher than 75 KHz and this bit 0 when HFLB frequency is lower than 75KHz. This bit controls gain of internal VCO so that PLL can work for whole range up to 135KHz.

Bit 6 AUTO_CH - Auto Character Height Adjustment. If this bit is set, the character height will be controlled internally to keep the fixed ratio in the vertical direction and independent of the display modes. In the meantime, CH5-CH0 are ignored.

Bit 5-0 CH5-CH0 - This six bits will determine the displayed character height. VMOSD-24 adopts 12 by 18 font matrix and the middle 16 lines, line 2 to line 17, are expanded by BRM algorithm. The top line and bottom line will be duplicated dependent on the value of CH. No any line is duplicated for top and bottom if CH is less than 32. One extra duplicated line will be inserted for top and bottom if CH is larger or equal to 32 and less than 48. Two extra duplicated lines will be inserted for top and bottom if CH is larger or equal to 48. Setting a value below 16 will not have a predictable result.

Formula of character height is:

H = N x 18 + (CH3 : CH0)

N = 1 if CH5:CH4=0,0 or 0,1

N = 2 if CH5:CH4=1,0

N = 3 if CH5:CH4=1,1

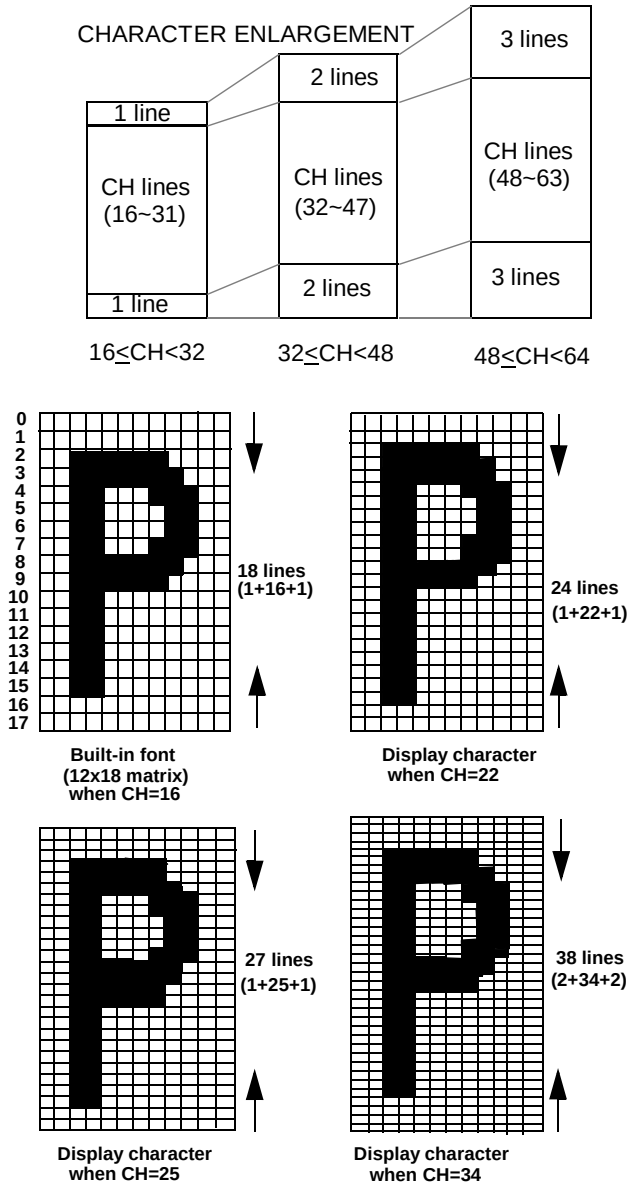


Figure 12. Variable Character Height

Figure 12 illustrates the enlargement algorithm for top and bottom lines and how this chip expand the built-in character font to the desired height.

In this approach, the actual character height in unit of the scan line can be calculated from the following simple equation:

H = CH + N

Where H is the expanded character height in unit of lines
CH is the number defined by CH5 ~ CH0
N is a variable dependent on the value of CH
N = 2 when 16≤CH<32
N = 4 when 32≤CH<48
N = 6 when 48≤CH<64

Frame Control Register Row 15 Coln 15

7	6	5	4	3	2	1	0
OSD_EN	0	0	M1	M0	0	FAD	0

Bit 7 OSD_EN - OSD circuit is activated when this bit is set.

Bit 6 Reserved. Set "0" for normal operation.

Bit 5 Reserved. Set "0" for normal operation.Impor

Bit 4-3 M1-M0 - It determines the number of dots per horizontal line. Three resolutions: 768,896 or 1024 dot per line mode are avaliable for video measurement function.

Note: After 896 or 1024 dot per line mode has been set for video measurement, i.e. (M1:M0)=(1,0) or(1,1) , it is recommended to refresh all the OSD display registers content(Row 0 to 14) and character attribute registers content(Row 0 to 14) before displaying the OSD menu again.

OSD menu display resolution is stricted to 768 dot per line. User can change these bits for higher resolution for video measurement and then resume 768 dot per line mode for OSD menu display. Please refer to the Table 2 for details.

Table 2. Resolution Setting

(M1, M0)	0,0	0,1	1,0	1,1
Dots / Line	Reserved	768	896	1024

Note : The internal VMOSD PLL clock (dot clock) frequency is related to this resolution setting and the HFLB input in Pin5. The VMOSD dot clock is given by following formula:

$f_{PLL} = f_{\overline{HFLB}} \times$ Resolution

eg. 768 dot/line mode at $\overline{HFLB}$ of 107KHz will give f_{PLL} of 82.2MHz.

Together with the max. 135KHz $\overline{HFLB}$ and max. 110MHz f_{PLL} spec, the maximum Pin5 HFLB frequency that can be applied for each resolution are summaried in the table below:

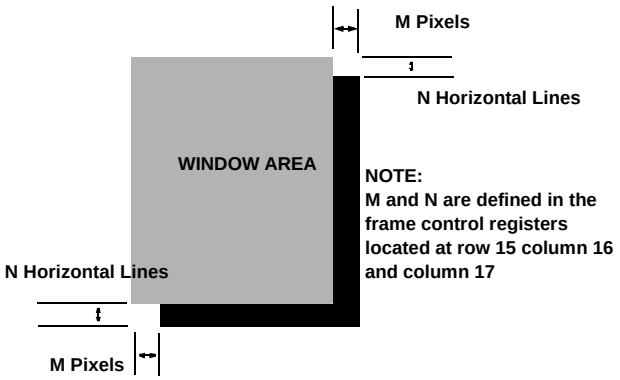
Table 3. Resolution vs $\overline{HFLB}$

Resolution (Dots/Line)	Max. $\overline{HFLB}$ frequency (KHz)*
768	135
896	122
1024	107

Bit 2 Reserved. Set "0" for normal operation.

Bit 1 FAD - It enables the fade-in/fade-out functions when OSD is turned on from off state or vice versa. If this bit is set, it roughly takes about one second to fully display the whole menu. It also takes 1 second to disappear completely.

Bit 0 Reserved for chip testing. Set to "0" for normal operation.



Window Shadowing

Frame Control Register Row 15 Coln 16

7	6	5	4	3	2	1	0
WW41	WW40	WW31	WW30	WW21	WW20	WW11	WW10

Bit 7-6 WW41, WW40 - It determines the shadow width of the window 4 when the window shadowing function is activated. Please refer to the following table for more details where M is the actual pixel number of the shadowing.

Table 4. Shadow Width Setting

(WW41, WW40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Width M (unit in Pixel)	2	4	6	8

Bit 5-4 WW31, WW30 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 3 when the window shadowing function is activated.

Bit 3-2 WW21, WW20 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 2 when the window shadowing function is activated.

Bit 1-0 WW11, WW10 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 1 when the window shadowing function is activated

Frame Control Register Row 15 Coln 17

7	6	5	4	3	2	1	0
WH41	WH40	WH31	WH30	WH21	WH20	WH11	WH10

Bit 7-6 WH41, WH40 - It determines the shadow height of the window 4 when the window shadowing function is activated. Please refer to the following table for more details where N is the actual line number of the shadowing.

Table 5. Shadow Width Setting

(WH41, WH40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Height N (unit in Line)	2	4	6	8

Bit 5-4 WH31, WH30 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 3 when the window shadowing function is activated.

Bit 3-2 WH21, WH20 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 2 when the window shadowing function is activated.

Bit 1-0 WH11, WH10 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 1 when the window shadowing function is activated.

Frame Control Register Row 15 Coln 18

7	6	5	4	3	2	1	0
MSB				LSB	TRIC	HPOL	VPOL
← RSPACE →							

Bit 7-3 RSPACE - These 5 bits define the row to row spacing in unit of horizontal scan line. It means extra N lines, defined by this 5-bit value, will be appended for each display row. Because of the nonuniform expansion of BRM used by character height control, this register is usually used to maintain the constant OSD menu height for different display modes instead of adjusting the character height. The default value of it is 0. It means there is no any extra line inserted between row and row after power on. It can be used for Portrait monitor too when icon design is rotated 90 degree.

Bit 2 TRIC - Tri-state Control. This bit is used to control the driving state of output pins, R, G, B and FBKG when the OSD is disabled. After power on, this bit is reset and R, G, B and FBKG are in high impedance state while OSD being disabled. If it is set by MCU, these four output pins will drive low while OSD being in disabled state. Basically, the setting is dependent on the requirement of the external application circuit.

Bit 1 HPOL - This bit selects the polarity of the incoming horizontal sync signal (HFLB). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive H sync signal. After power on, this bit is cleared.

Bit 0 VPOL - This bit selects the polarity of the incoming vertical sync signal (VFLB). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive V sync signal. After power on, this bit is cleared.

NOTE: The registers located at column 19 of row 15 are reserved for the chip testing. In normal operation, they should not be programmed anytime.

PWM Control Registers Row 15 Col 20 to Col 25

	7	6	5	4	3	2	1	0
ROW 15 COLN 20-25	MSB			PWM_n				LSB

Bit 7-0 PWM_n - This eight-bit value decides the output duty cycle and waveforms of PWM. There are 6 channels of PWM. And the corresponding registers are located from column 20 to column 25 respectively on row 15. The higher five bits (MSB) are used for the conventional PWM and the lower 3 bits (LSB) for the BRM. Please refer to Figures 13 &14 for more information about BRM algorithm and PWM output waveform. The default values for these registers after power on are "0".

Please also refer to the setting of the PWM Output Control Register(Row15;Col28) for higher performance of the PWM channels.

Reserved Registers:Row15,Coln26 to Coln 27

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bit 7-0 Reserved. Do not program these registers after power on.

PWM Output State Registers:Row15,Coln 28

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PWMOUT

Bit 7-1 Reserved. Do not program these registers after power on.

Bit 0 PWM Output State Control - Set this bit to "1" will make the PWM output to high impedance state for the half horizontal period. This period includes the PLL phase detection region where the original internal CLK pulses for PWM are less even. The remaining half period will keep at push-pull. This is to get a higher linearity for the PWM output. A more linear DC voltage can be obtained after the RC low pass filter attached to the PWM pin. **It is recommended to set this bit to "1" for better performance of PWM output**. Figure 15 shows the full period push-pull PWM CLK when this bit is reset. Figure 16 shows the PWM output when this bit is set.

Power on default for this bit is "0" where the PWM output is always push-pull.

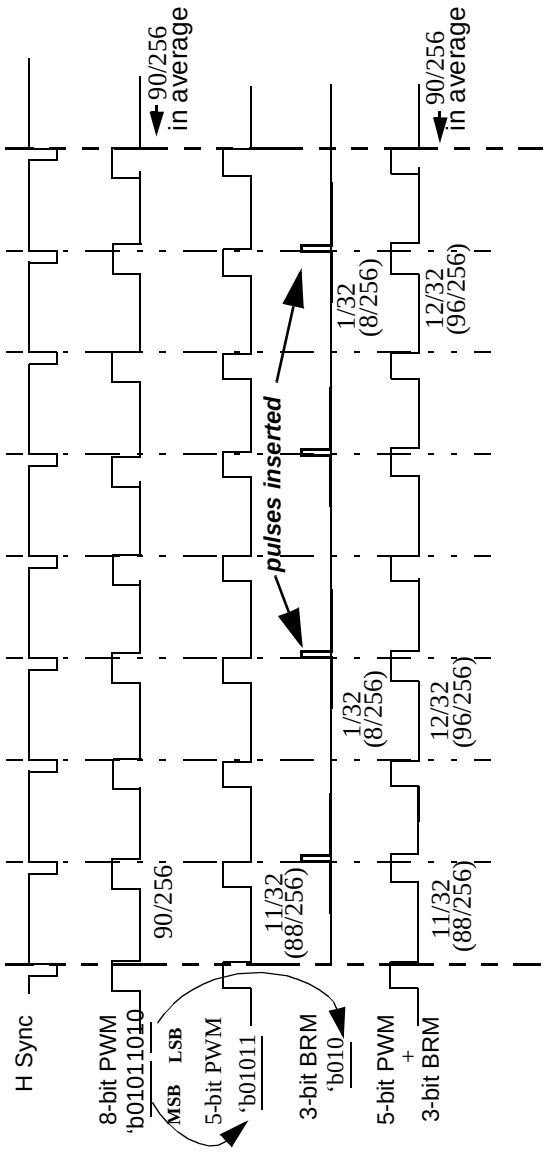


Figure 13. Pure 8-bit PWM v.s. 5-bit PWM + 3-bit BRM

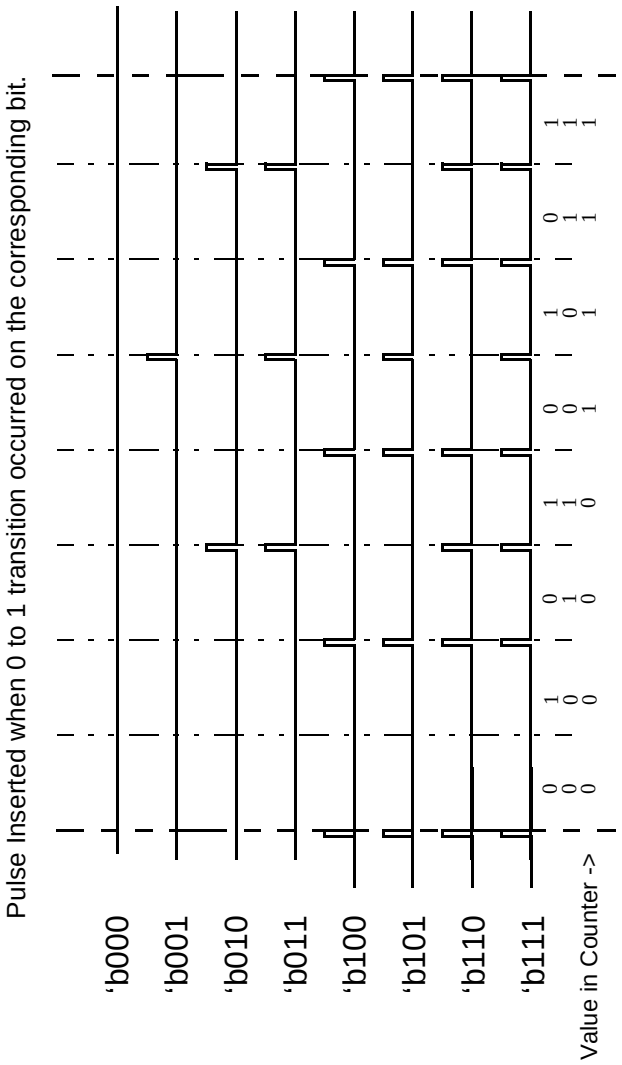


Figure 14. BRM Pulse Insertion Algorithm

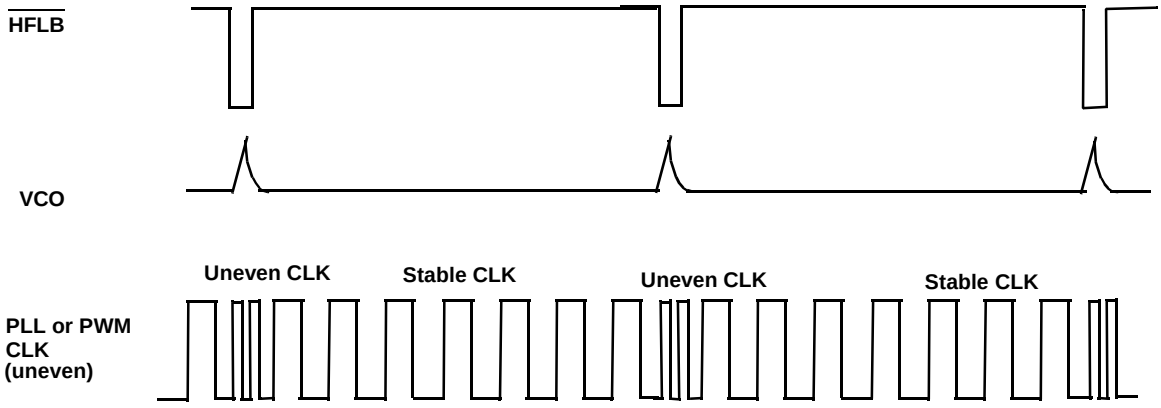
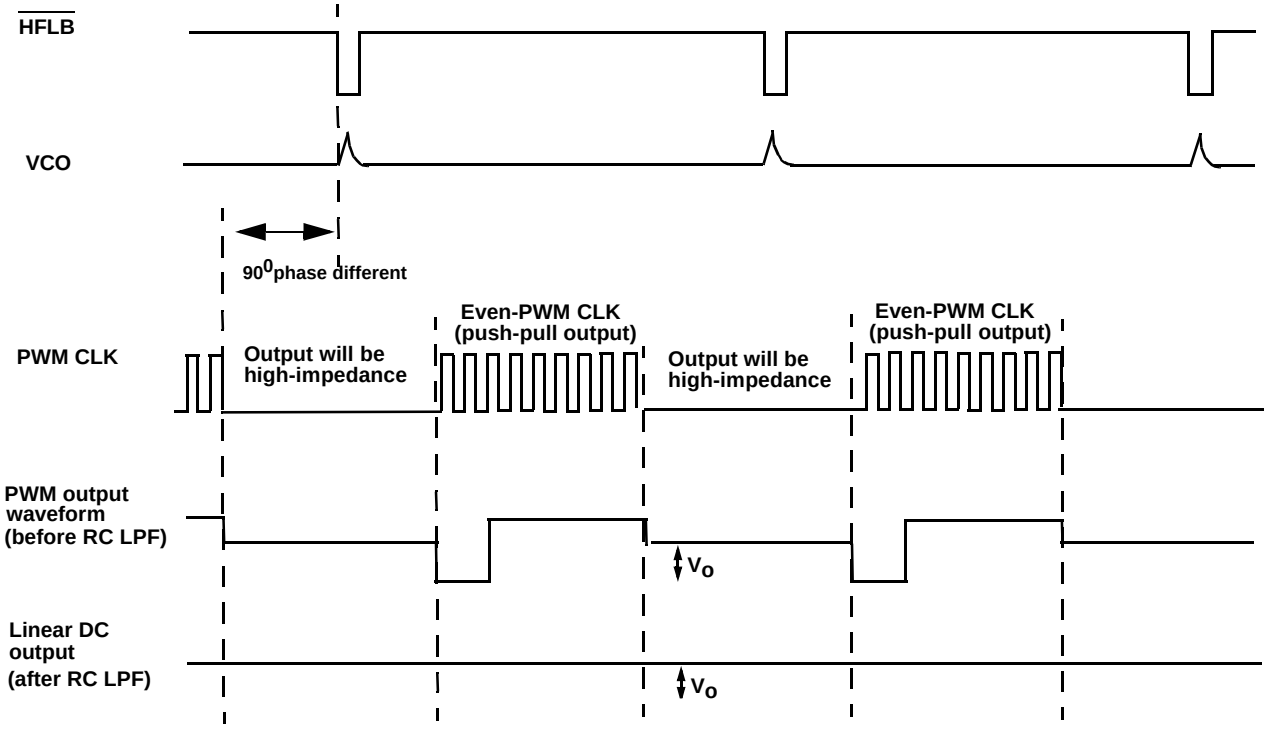


Figure 15. : PWM CLK for Full Period Push-Pull Output



Vo:PWM DC output after the RC Low-Pass-Filter

Figure 16. PWM "Half Period Push-Pull, Half Period High-Impedance" output concept

(IV) Special Control Registers

Chip Configuration Register (Row16, Coln0)

7	6	5	4	3	2	1	0
CLR	FSS	INV	FSW	VE	HE	0	0

Bit 7 CLR - By writing “1” to this bit, all display memory from Row 0 to Row 14 are all cleared but not affecting Control registers.

Bit 6 FSS - Font Size Selection

1: 10x18 font size selected

0: 12x18 font size selected

Bit 5 INV - Inverse the test pattern outputs from white to black and black to white vice versa.

Bit 4 FSW - Full Screen White Enable, by setting “1” to this bit, all R,G,B and FBKG output will be pull high continuously. The vertical and horizontal hatch lines pattern enabled by Bit 3 & Bit 4 in this register will be overridden. Full Screen White can be inversed by setting INV bit to “1” where R,G, B will be pull low and FBKG pull high continuously.

Bit 3 VE - Vertical Line Enable, while writing “1” to this bit, the vertical hatch lines will be shown by the settings of V3, V2, V1, V0 in Hatch Line Space Register.

Bit 2 HE - Horizontal Line Enable, while writing “1” to this bit, the horizontal hatch lines will be shown by the settings of H3, H2, H1, H0 in Hatch Line Space Register.

Note: Compares with OSD outputs, FSW and the Hatch lines pattern above are at the lowest priority. In addition, when these test pattern generator is activated, the video signal from PC will be disable as FBKG output signal will always high.

Bit 1-0 Reserved. Set "0" for normal operation.

Hatch Line Space Register(Row16, Coln1)

7	6	5	4	3	2	1	0
H_3	H_2	H_1	H_0	V_3	V_2	V_1	V_0

Bit 7-4 H3, H2, H1, H0 - define line space of horizontal hatch lines.

Zero is not allowed. Default value is 1.

Bit 3-0 V3, V2, V1, V0 - define line space of vertical hatch lines.

Zero is not allowed. Default value is 1.

The space is defined by the formulas below:

Space of Horizontal Hatch lines = (H3, H2, H1, H0) X 3 + 3

Space of Vertical Hatch Lines = (V3, V2, V1, V0) X 4 + 4

The hatch lines are white when the INV bit is not set. The whole hatch pattern will be inversed by setting INV bit to “1”.

Windows Shadow Color Register 1(Row16,Coln2)

7	6	5	4	3	2	1	0
0	R_2	G_2	B_2	0	R_1	G_1	B_1

This register defines the shadow colors of window 1 and window 2.

Bit 7 Reserved. Set "0" for operation.

Bit 6-4 R2, G2, B2 - define the shadow color for window 2.

Bit 3 Reserved. Set "0" for operation.

Bit 2-0 R1, G1, B1 - define the shadow color for window 1.

Windows Shadow Color Register 2(Row16, Coln3)

7	6	5	4	3	2	1	0
0	R_4	G_4	B_4	0	R_3	G_3	B_3

This register defines the shadow colors of window 3 and window 4.

Bit 7 Reserved. Set "0" for operation.

Bit 6-4 R4, G4, B4 - define the shadow color for window 4.

Bit 3 Reserved. Set "0" for operation.

Bit 2-0 R3, G3, B3 - define the shadow color for window 3.

Page Selection Register(Row16,Coln4)

7	6	5	4	3	2	1	0
0	C_2	C_1	C_0	0	B_2	B_1	B_0

Base Bank is fix 64-ROM(address 00-3F). The register define the address pointers of Bank B(address 80-BF) and Bank C(address C0-FF). Please also refer to table 6 and Figure 20 for Page ROM illustration.

Note:The definition of Bank A(40-7F) address pointer is located in Row16, Coln 7 register.

Bit 7 Reserved. Set "0" for normal operation.

Bit 6-4 C2, C1, C0 - define the page selected to Bank C.

Bit 3 Reserved. Set "0" for normal operation.

Bit 2-0 B2, B1, B0 - define the page selected to Bank B.

The default page in bank B and C are page 1.

Reserved Register(Row16,Coln5)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bit 7-0 Reserved. Set all bits to "0" for normal operation.

Video Measurement Control Register(Row16,Coln6)

	7	6	5	4	3	2	1	0
ROW 16 COLN 6	VMEN	0	0	0	VSPL	RGBPL	HBPL	HSPL

This register is the control register of video measurement function.

Bit 7 VMEN is set to enable the video measurement starting from next vertical frame. This bit is clear after reset.

Note:

1. It is suggested to disable the OSD menu display during video measurement function to aviod any possible unstable OSD menu display during video measurement.

2. If 896 or 1024 dot per line mode(refer to page 12)has been set during video measurement, it is recommended to refresh all the display registers contents(Row0-14) and character attribute registers content(Row0-14) before displaying OSD menu again.

Bit 6-4 Reserved. Set "0" for normal operation.

Bit 3 VSPL defines the signal edge of $\overline{\text{VSYNC}}$ input to be referred for vertical timing measurement. When it is "0", the falling edge of VSYNC is the reference edge. When it is "1", the rising edge of VSYNC is the reference edge. It is "0" after reset.

Bit 2 RGBPL defines the active level of RGBIN input. When it is "0", the active level is high. When it is "1", the active level is low. It is "0" after reset.

Bit 1-0 HBPL defines the polarity of $\overline{\text{HFLB}}$ pulse input for the reference of the video measurement function. Set it to "0" if the polarity is negative. Set to "1" when it the polarity is positive. It is "0" after reset.

Bit 0 HSPL defines the signal edge of $\overline{\text{HSYNC}}$ input to be referred for horizontal timing measurement. Set it to "0" means the falling edge of HSYNC is the reference edge. When set to "1", the rising edge of $\overline{\text{HSYNC}}$ is the reference edge. It is "0" after reset.

Page Selection Register(Row16,Coln7)

7	6	5	4	3	2	1	0
0	0	0	0	0	A_2	A_1	A_0

The register define the address pointer of Bank A(address $40-$7F). Please also refer to table 6 and Figure 20 for Page ROM illustration.

Note:The definition of Bank B and Bank C address pointer is located in Row16, Coln 4 register.

Bit 7-3 Reserved. All bits are set to 0 during normal operation.

Bit 2-0 A2, A1, A0 define the page selected to Bank A.

The default page in bank A is Page 0.

The definition of page number is listed in Table 6.

Table 6. Page ROM selection

	BANK A			BANK B			BANK C		
	A2	A1	A0	B2	B1	B0	C2	C1	C0
Page 0	1	1	0	1	1	0	1	1	0
Page 1	0	0	0	0	0	0	0	0	0
Page 2	0	0	1	0	0	1	0	0	1
Page 3	0	1	0	0	1	0	0	1	0
Page 4	0	1	1	0	1	1	0	1	1
Page 5	1	0	0	1	0	0	1	0	0
Page 6	1	0	1	1	0	1	1	0	1
Reserve	1	1	1	1	1	1	1	1	1

READ-ONLY REGISTERS DEFINITION

There are 18 read-only registers in this chip which can be accessed by MCU through M-Bus in the sequence as shown in **Figure 17**. Their definition is shown in table 7 and diagram.

Table 7. Read Only Register Description

Register	Descriptions
STATUS	b7: RSTF =1: The chip has been reset. =0: The STATUS register has been read. b6: DONE =1: One complete timing measurement cycle has been done and VMEN bit is cleared. =0: When the VMEN bit is set by MCU. b5 ~ b0: reserved
RESERVED	b7 ~ b0: Not used
RESERVED	b7 ~ b0: Not used
RESERVED	b7 ~ b0: Not used
HBSTH	b7 ~ b2: Not used b1 ~ b0: The most significant 2 bits of **Dhbsta** which represents the distance between the leading edge of $\overline{\text{HFLB}}$ and reference $\overline{\text{HSYNC}}$ edge. See FIGURE 17.

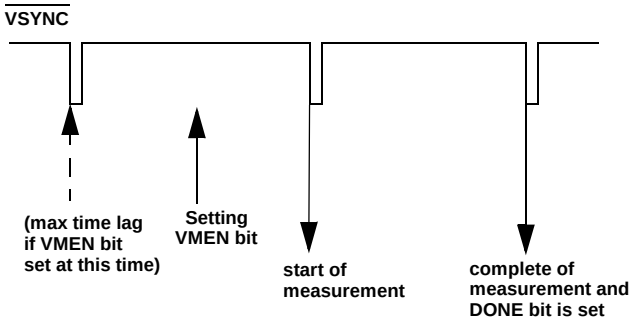
Table 7. Read Only Register Description

HBSTL	b7 ~ b0: The least significant 8 bits of **Dhbsta** which represents the distance between the leading edge of HFLB and reference HSYNC edge. See FIGURE 17.
HBEDH	b7 ~ b2: Not used b1 ~ b0: The most significant 2 bits of **Dhbend** which represents the distance between the trailing edge of HFLB and reference HSYNC edge. See FIGURE 17.
HBEDL	b7 ~ b0: The least significant 8 bits of **Dhbend** which represents the distance between the trailing edge of HFLB and reference HSYNC edge. See FIGURE 17.
RGBSTH	b7 ~ b2: Not used b1 ~ b0: The most significant 2 bits of **Drgbsta** which represents the distance between the first active edge of RGBIN input and reference HSYNC edge. See FIGURE 17
RGBSTL	b7 ~ b0: The least significant 8 bits of **Drgbsta** which represents the distance between the first active edge of RGBIN input and reference HSYNC edge. See FIGURE 17.
RGBEDH	b7 ~ b2: Not used b1 ~ b0: The most significant 2 bits of **Drgbend** which represents the distance between the last active edge of RGBIN input and reference HSYNC edge. See FIGURE 17.
RGBEDL	b7 ~ b0: The least significant 8 bits of **Drgbend** which represents the distance between the last active edge of RGBIN input and reference HSYNC edge. See FIGURE 17.
VRGBSH	b7 ~ b3: Not used b2 ~ b0: The most significant 3 bits of **Dvrgbsta** which represents the H line distance between the first active line of RGBIN input and reference VSYNC edge. See FIGURE 17.
VRGBSL	b7 ~ b0: The least significant 8 bits of **Dvrgbsta** which represents the H line distance between the first active line of RGBIN input and reference VSYNC edge. See FIGURE 17.
VRGBEH	b7 ~ b3: Not used b2 ~ b0: The most significant 3 bits of **Dvrgbend** which represents the H line distance between the last active line of RGBIN input and reference VSYNC edge. See FIGURE 17.

Table 7. Read Only Register Description

VRGBEL	b7 ~ b0: The least significant 8 bits of **Dvrgbend** which represents the H line distance between the last active line of RGBIN input and reference VSYNC edge. See FIGURE 17.
VSLNH	b7 ~ b4: Not used b3: LNOVER =1: The line number counter is overflow. =0: Not overflow. b2 ~ b0: The most significant 3 bits of **Dvsline** which represents the total H line count between two consecutive VSYNC pulses. See FIGURE 17.
VSLNL	b7 ~ b0: The least significant 8 bits of **Dvsline** which represents the total H line count between two consecutive VSYNC pulses. See FIGURE 17.

After VMEN bit has been set, the chip will start the measurement in the coming vertical reference edge and will complete the measurement at the end of that vertical period. Therefore, when taking the maximum possible time lag between VMEN bit enabling and the reference edge into account, customer can reserve two vertical frame periods for the whole video measurement process. Please refer to below diagram:



Note: VSYNC falling edge is set as reference edge in above diagram

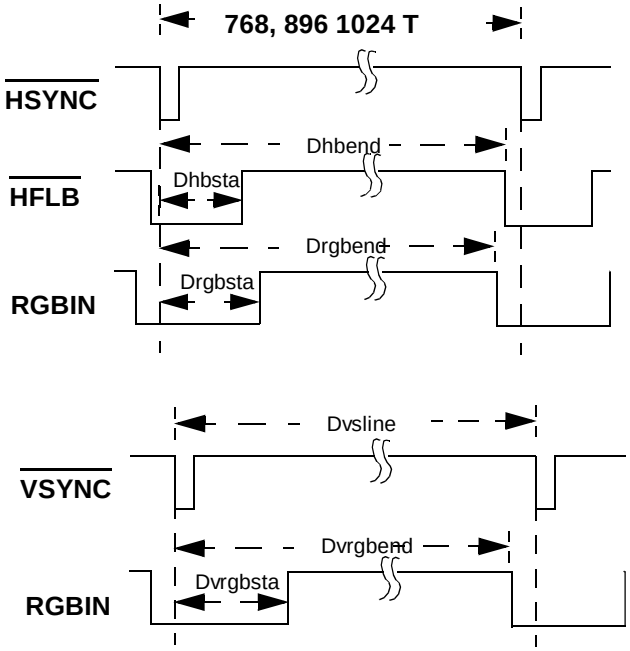


Figure 17. Timing Diagram of Video Measurement

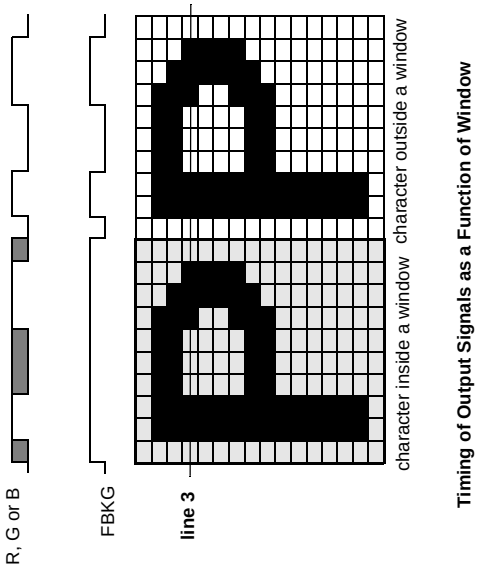


Figure 18. Display Frame Format

Figure 18 illustrates the timing of all output signals as a function of window and fast blanking features. Line 3 of all three characters is used to illustrate the timing signals. The shaded area depicts the window area.

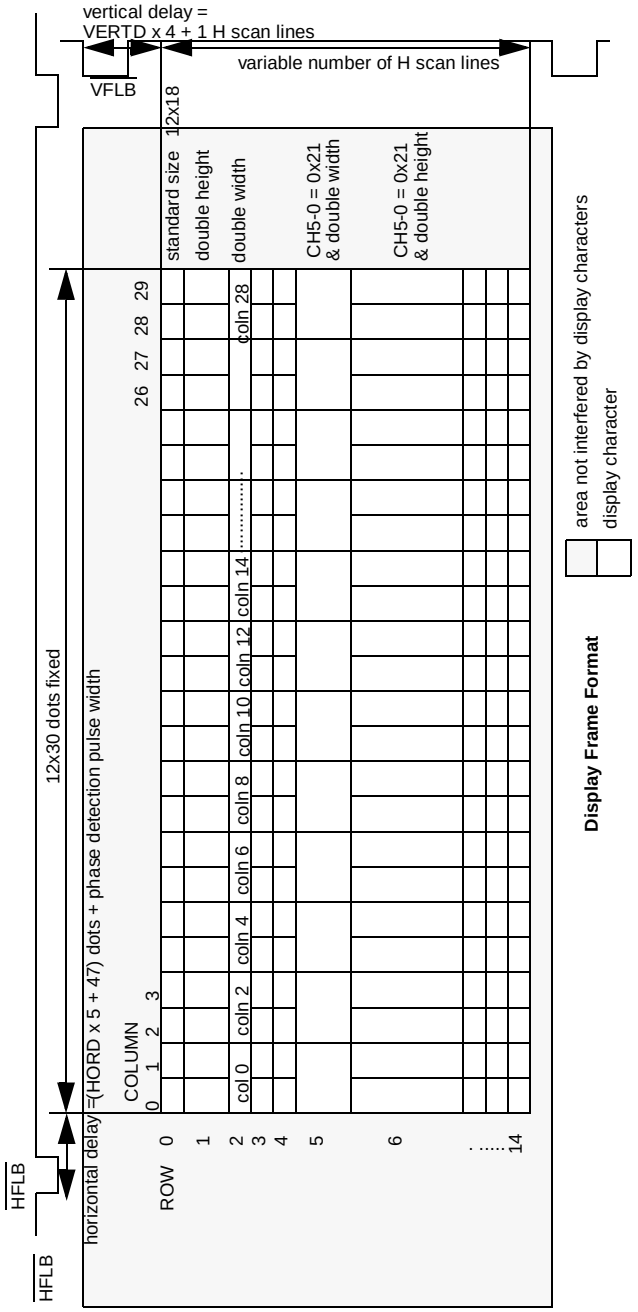


Figure 19. Display Frame Format

Figure 19 illustrates the positions of all display characters on the screen relative to the leading edge of horizontal and vertical flyback signals. The shaded area indicates the area not interfered by the display characters. Notice that there are two components in the equations stated in Figure 19 for horizontal and vertical delays: fixed delays from the leading edge of HFLB and VFLB signals, regardless of the values of HORD and VERTD: (47 dots + phase detection pulse width) and one H scan line for horizontal and vertical delays, respectively; variable delays determined by the values of HORD and VERTD. Refer to Frame Control Registers COLN

9 and 10 for the definitions of VERTD and HORD. Dot frequency is determined by the equation: H Freq. x Dot/line which can be selection by resolution setting.

When double character width is selected for a row, only the even-numbered characters will be displayed, as shown in row 2. Notice that the total number of horizontal scan lines in the display frame is variable, depending on the chosen character height of each row. Care should be taken while configuring each row character height so that the last horizontal scan line in the display frame always comes out before the leading edge of VFLB of next frame to avoid wrapping display characters of the last few rows in the current frame into the next frame.

A software called MC141580P2 FONT EDITOR in IBM PC environment was written for MC141580P2 editing purposes. It generates a set of S-Record or Binary record for the desired display patterns to be masked onto the character ROM of the MC141580P2. 16 Color fonts are located in addresses $01-10. The character $00 is pre-defined for blank character, the character $7F is pre-defined for full-filled character.

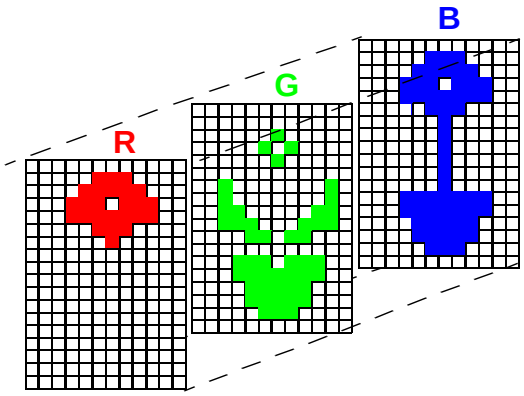
In order to have better character display within windows, we suggest you to place your designed character font in the centre of the 10x18 or 12x18 matrix, and let its spaces be equally located in the four sides of the matrix.

Multi-Color Font

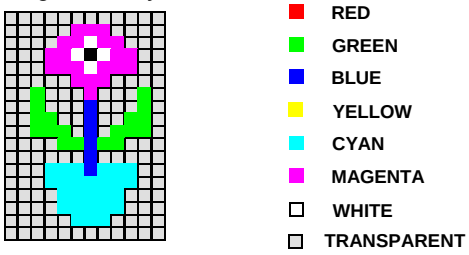
The color font comprises three different R, G and B fonts. When the code of color font is accessed, the separate R/G/B dot pattern conbime to a multi-color font. When editing color fonts, there are 9 items for selection. They are eight colors and transparent option for selections in font editor. Please refer to following diagram.

.

Color Font Dot Matrix



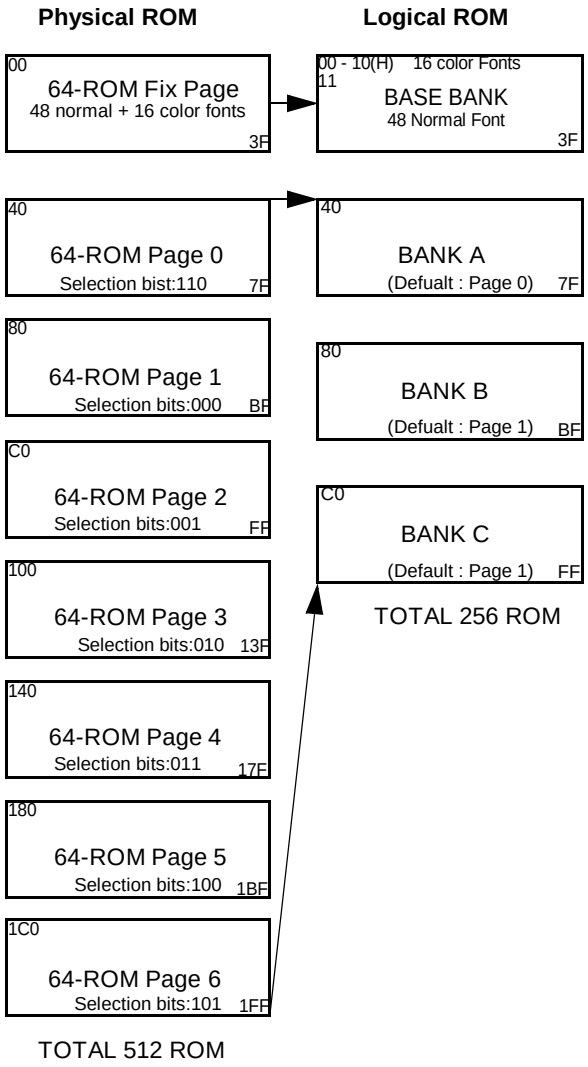
Displayed Color Font



ROM

MC141580P2 contains 512 character ROM. Physical ROM includes one 64-ROM fix ROM and seven 64-ROM Pages(0-6). User can define these character ROM in mask ROM layer. Addressable/logical ROM includes Base Bank, Bank A, Bank B and Bank C. Base Bank address range is $00-3F where 16 color fonts locate in $01-$10, blank in $00 (and fill is at $7F in Page0). It is direct mapping of Base Bank. Bank A address range is $40-$7F. Bank B address range is $80-BF and Bank C address range is $C0-FF. Contents of Bank A, Bank B and Bank C are selected by Page Selection Registers which determine the Page mapping, Page 0 to Page 6.

It is suggested that users arrange the most frequent used fonts into the first 64-ROM fix page when designing their custom fontset. This can make those symbols can be called to display no matter how the page selection registers are configured. Moreover, the color fonts is locating from 01h to 10h.



0	C_2	C_1	C_0	0	B_2	B_1	B_0

Selections for BANK B & C
Register in ROW 16, Coln 4

0	0	0	0	0	A_2	A_1	A_0

Selection for BANK A:
Register in ROW 16, Coln 7

Figure 20. Character ROM Mapping

10x18 and 12x18 Font

There is no physical difference between 10x18 and 12x18 fonts inside MC141580P2 character ROM. All the 512 characters are masked in 12x18 format.

But once the FSS bit in Special Register (ROW16:Coln0) is set to 1, the RGB output will change to 10x18 display format. That is, only the first 10 dots in every line of the original character will be displayed, the last two dots will be omitted.Then all characters in OSD menu will be in 10x18 display format . So do not use the two dots at right most in the 12x18 dot matrix when designing 10x18 fonts for custom mask ROM:

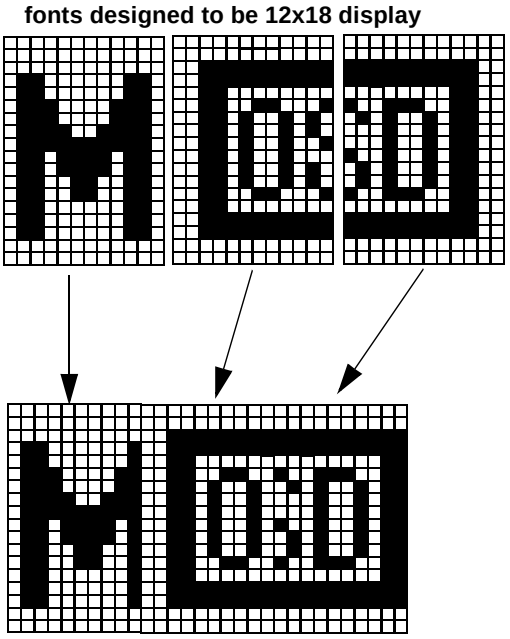


Figure 21. 12x18 & 10x18 fonts

Icon Combination

User can create On-Screen menu based on those characters and icons. Please refer to Table 8 for Icon combination. Address $00(space) & $7F(full-filled) are pre-defined characters for testing, address $01-10(H) are location of multi-color fonts.

ROM CONTENT

Figures 22 – 29 show the ROM content of MC141580P2. Mask ROM is optional for custom parts.

Table 8. Contents for the Page ROMS

Fix PAGE (00-3F)
Multi-color fonts($01-$10)
Numeric
PAGE 0 (40-7F)
Geometry
PAGE 1 (80-BF)
English & European(large capitcal)
PAGE 2 (C0-FF)
English & European(small capitcal)
PAGE 3 (100-13F)
Japanese
PAGE 4 (140-17F)
Japanese
PAGE 5 (180-1BF)
Korean
PAGE 6 (1CF-1FF)
Additional symbols

NOTE: The address ranges shown in above table refer to the physical address inside Mask ROM. These addresses will only be useful in designing the custom fontset using the VMOSD-24 font editor. The logical addressable space for display characters will only be 00-FF after desired ROM pages for BANK A, B & C are selected.

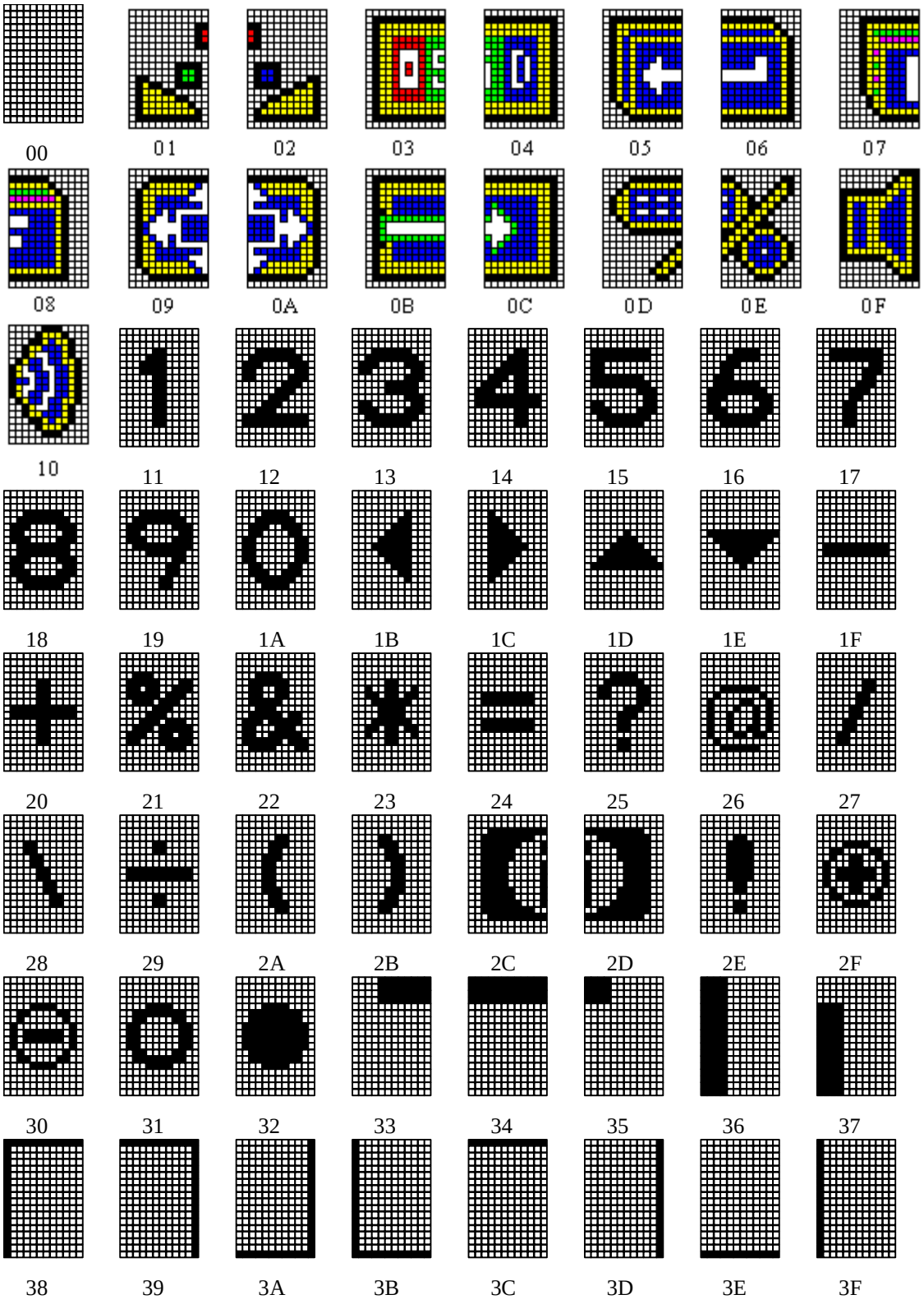


Figure 22. ROM contents for Fix PAGE ($00-$3F)

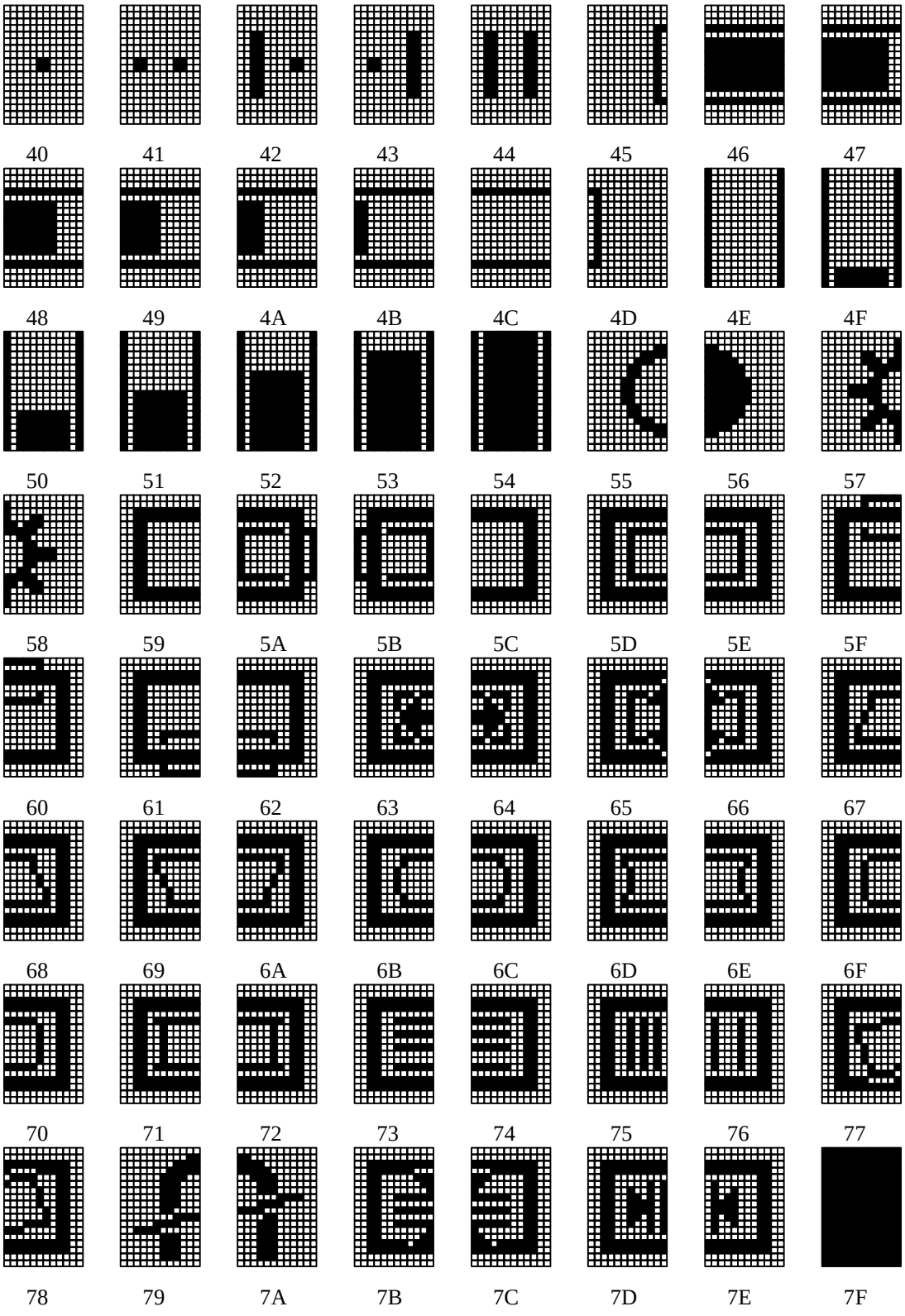


Figure 23. ROM contents for PAGE 0 ($40-$7F)

NOTE: The logical addresses shown above assume PAGE 0 is selected for BANK A. If it is selected for BANK B, each address needs to be increased by 40(H). If it is selected for BANK C, each address needs to be increased by 80(H).

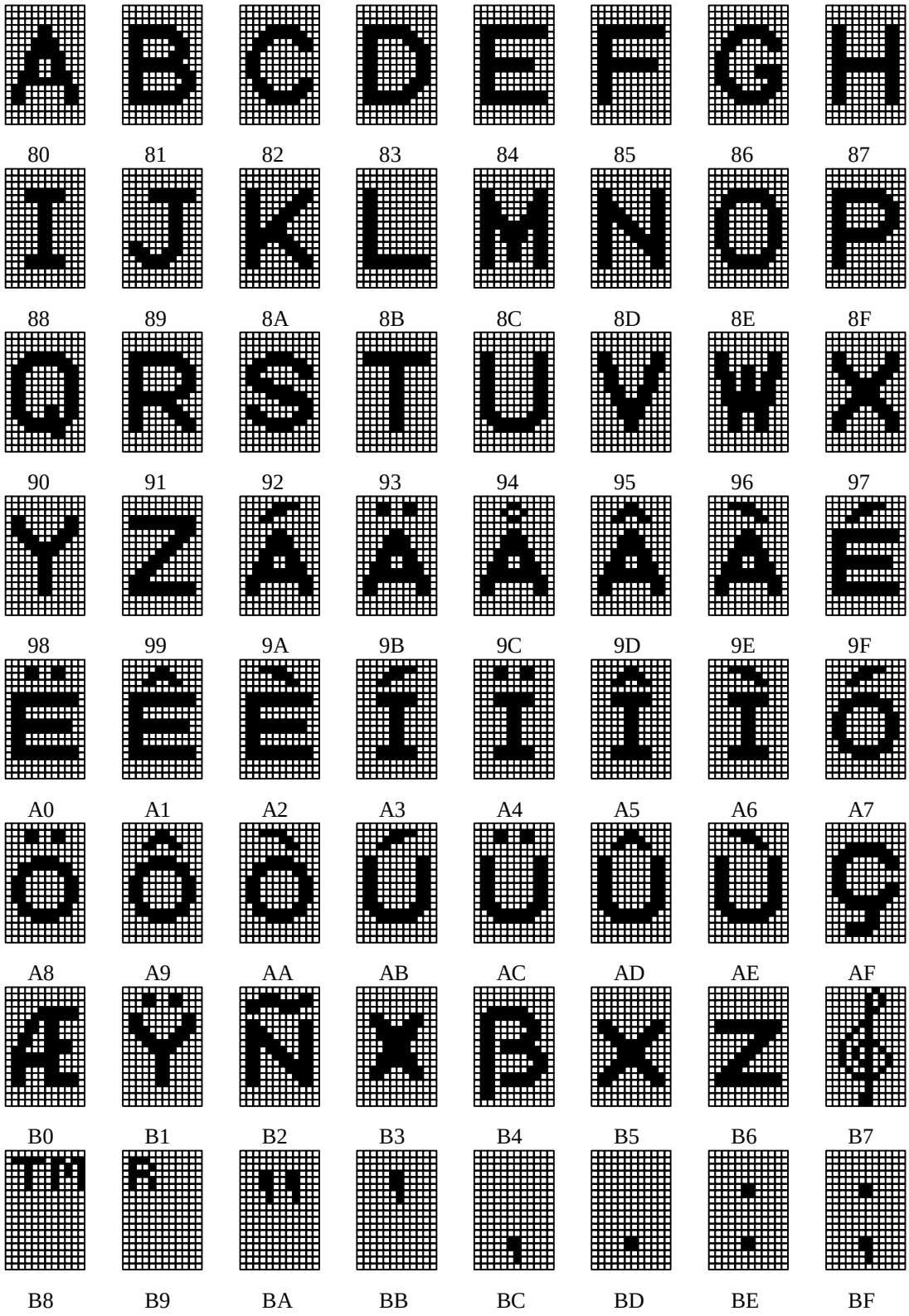


Figure 24. ROM contents for PAGE 1

NOTE: The logical addresses shown above assume PAGE 1 is selected for BANK B. If it is selected for BANK C, each address needs to be increased by 40(H). If it is selected for BANK A, each address needs to be decreased by 40(H).

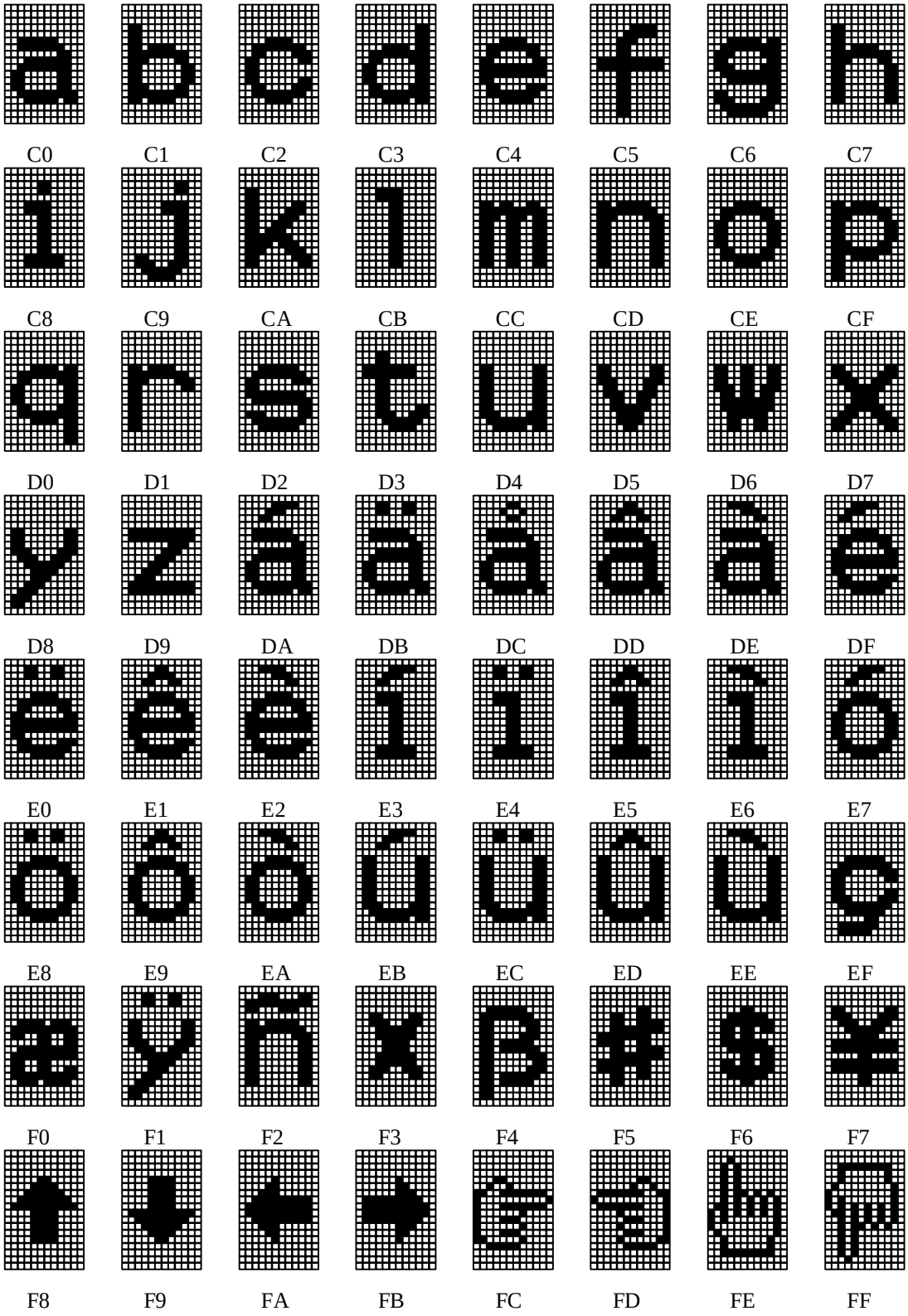


Figure 25. ROM contents for PAGE 2

NOTE: The logical addresses shown above assume PAGE 2 is selected for BANK C. If it is selected for BANK B, each address needs to be increased by 40(H). If it is selected for BANK A, each address needs to be decreased by 80(H).

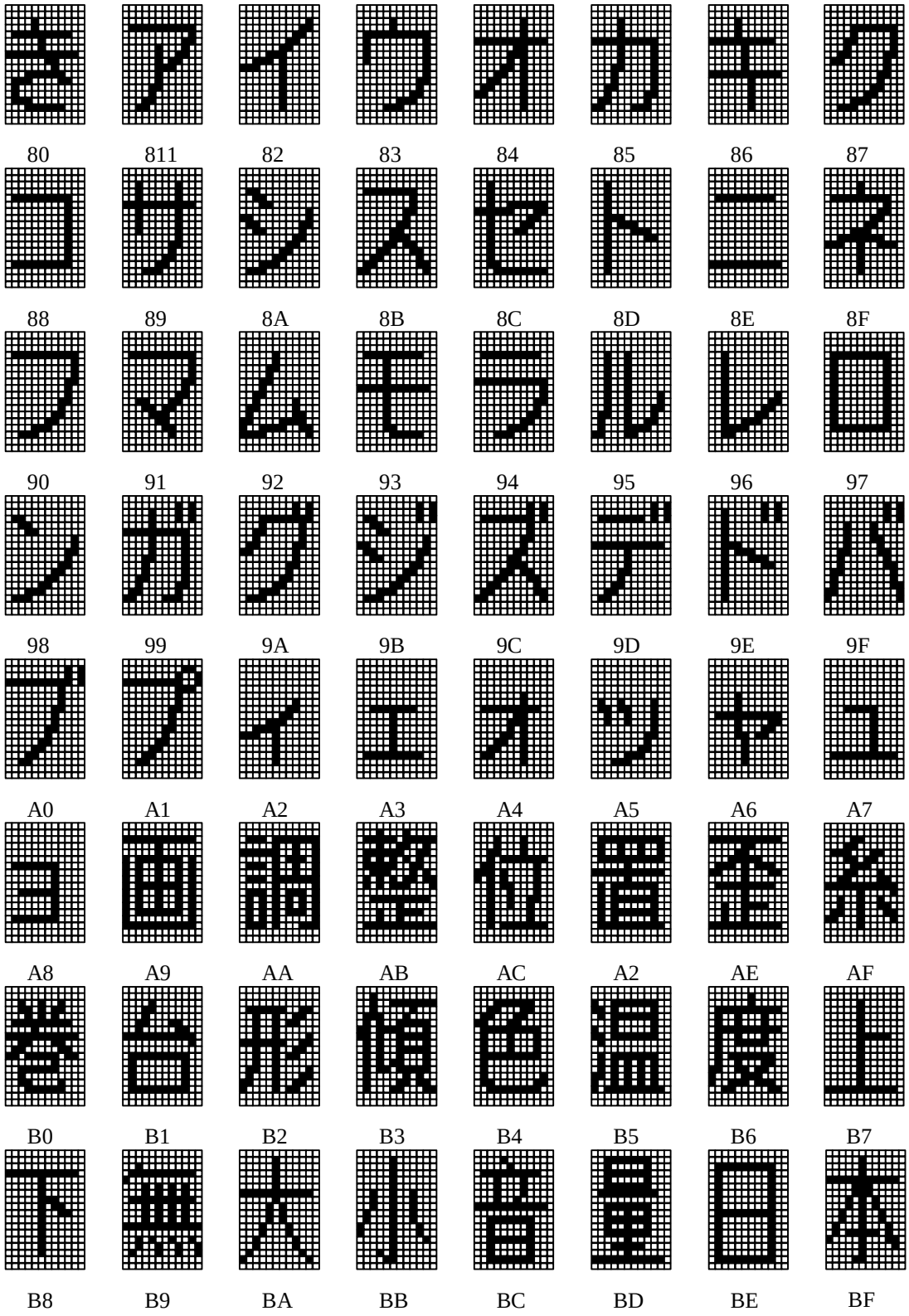


Figure 26. ROM contents for PAGE 3

NOTE: The logical addresses shown above assumes PAGE 3 is selected for BANK B. If it is selected for BANK C, each address needs to be increased by 40(H). If it is selected for BANK A, each address needs to be decreased by 40(H).

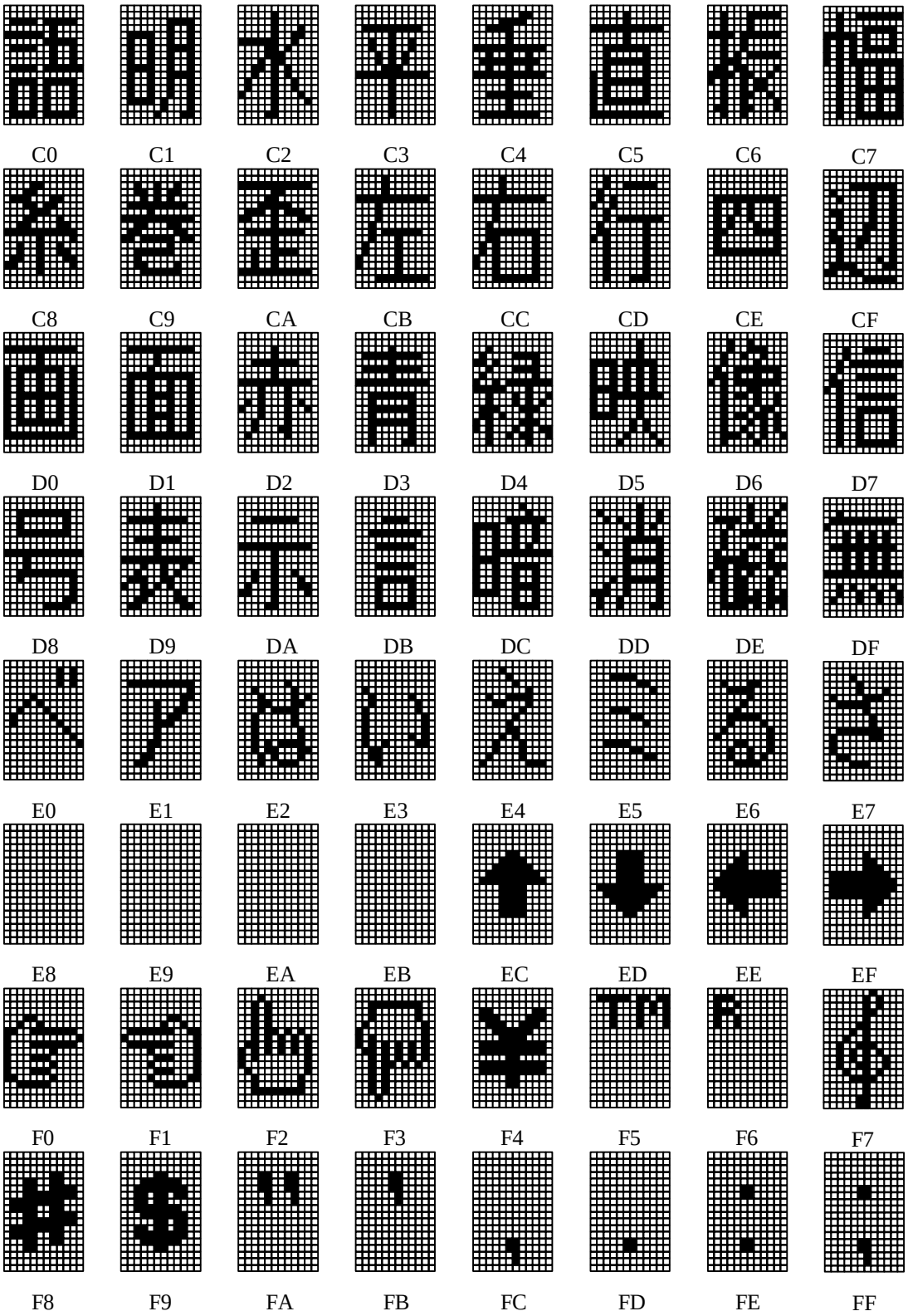


Figure 27. ROM contents for PAGE 4

NOTE: The logical addresses shown above assumes PAGE 4 is selected for BANK C. If it is selected for BANK B, each address needs to be decreased by 40(H). If it is selected for BANK A, each address needs to be decreased by 80(H).

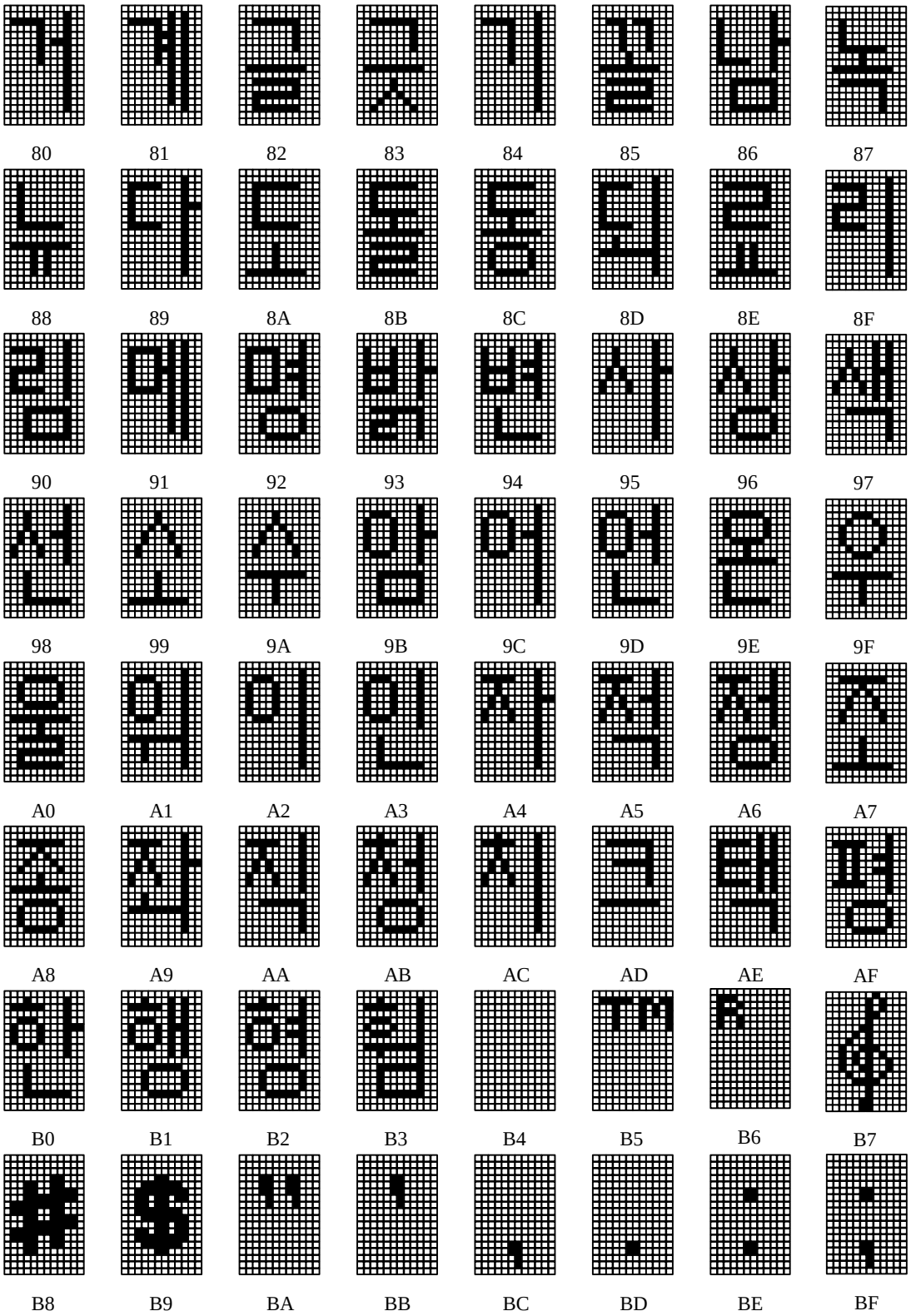


Figure 28. ROM contents for PAGE 5

NOTE: The logical addresses shown above assumes PAGE 5 is selected for BANK B. If it is selected for BANK C, each address needs to be increased by 40(H). If it is selected for BANK A, each address needs to be decreased by 40(H).

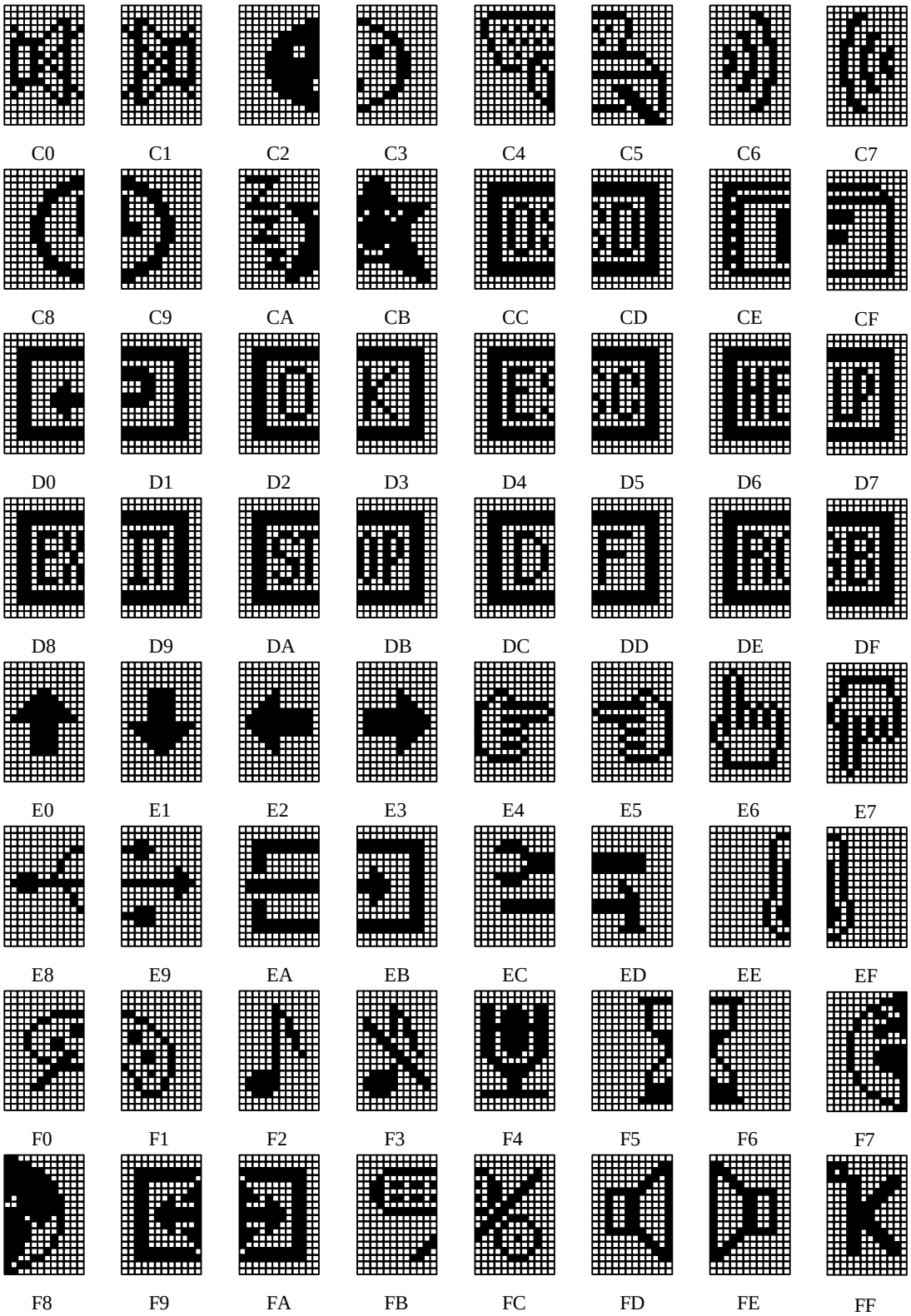


Figure 29. ROM contents for PAGE 6

NOTE: The logical addresses shown above assumes PAGE 6 is selected for BANK C. If it is selected for BANK B, each address needs to be decreased by 40(H). If it is selected for BANK A, each address needs to be decreased by 80(H).

DESIGN CONSIDERATIONS

Distortion

Motorola's MC141580P2 VMOSD-24 has a built-in PLL for multisystems application. Pin 2 voltage is a dc basing for the internal VCO in the PLL. When the input frequency ($\overline{HFLB}$) in Pin 5 becomes higher, the VCO voltage will increase accordingly. The built-in PLL then has a higher locked frequency output. The frequency should be equal to 768/896/1024 x $f_{\overline{HFLB}}$ (depends on resolution). It is the dot-clock in each horizontal line.

Display distortion is caused by noise in Pin 2. Positive noise makes VCO run faster than normal. The corresponding scan line will be shorter accordingly. In contrast, negative noise causes the scan line to be longer. The net result will be distortion on the display, especially on the right hand side with window turn on.

In order to have distortion-free display, the following recommendations should be considered.

- Only analog part grounds (Pin 2 to Pin 4) can be connected to Pin 1($V_{SS(A)}$). V_{SS} and other grounds should connect to PCB common ground. Then the $V_{SS(A)}$ and V_{SS} grounds can be connected by a bead core. Please refer to the application diagram(NOTE: Vss(A) and Vss are connected internally.)
- DC supply path for Pin 4 ($V_{DD(A)}$) should be separated from other switching devices.
- LC filter should be connected between Pin 17 and Pin 4. Refer to the values used in the Application Diagram.
- Biasing and filter networks should be connected to Pin 2 and Pin 3. Refer to the recommended networks in the Application Diagram.
- Two small capacitors can be added between Pin1-Pin2 and Pin3-Pin4 to filter VCO noise if necessarry. Values should be small enough to avoid picture unlocking caused by temperature variation.

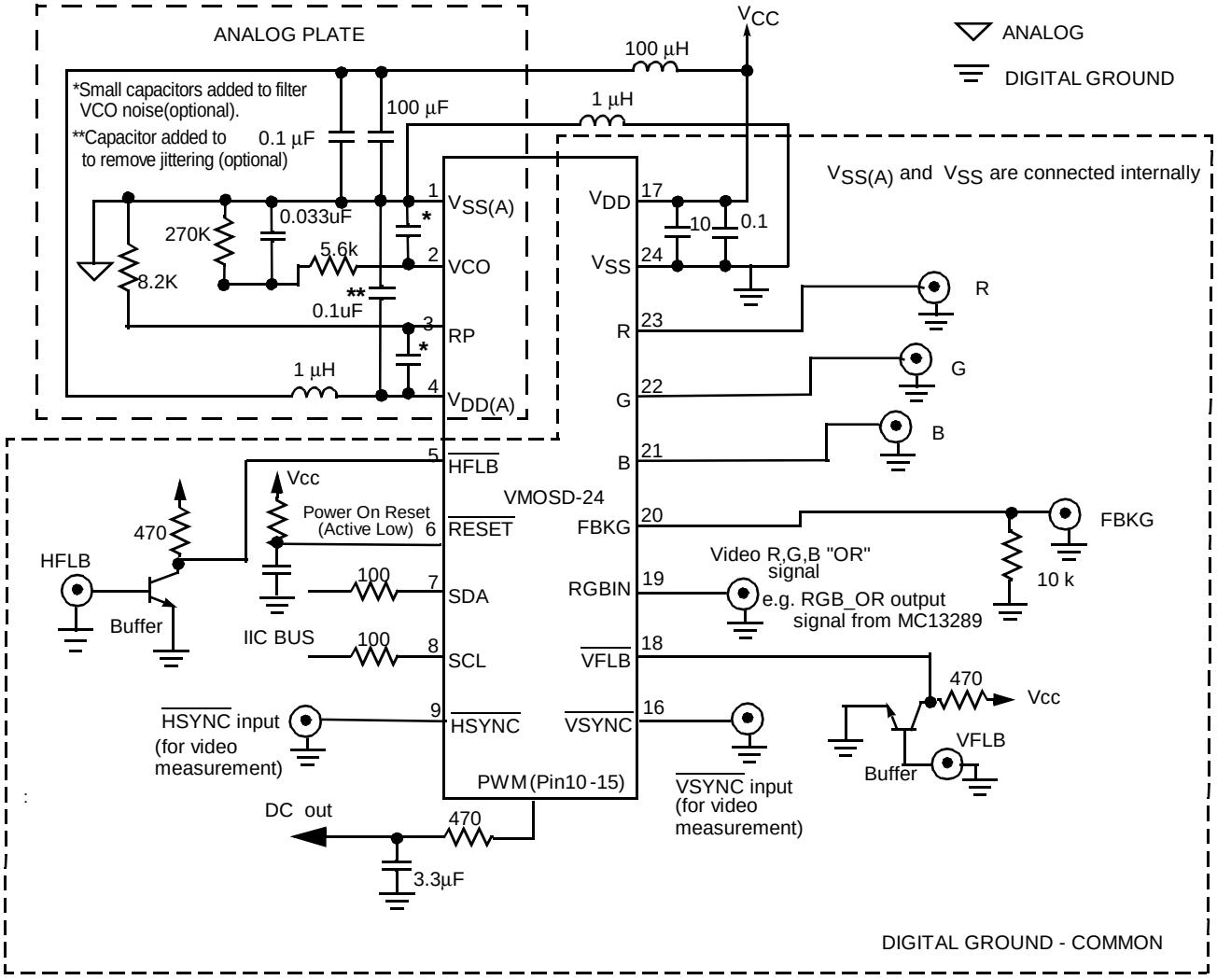
Jittering and Unlocking

Most display jittering and unlocking is caused by $\overline{HFLB}$ in Pin 5. Care must be taken if the $\overline{HFLB}$ signal comes from the flyback transformer. A short path and shielded cable are recommended for a clean signal. Buffer is needed for both $\overline{HFLB}$ and $\overline{VFLB}$ inputs. Refer to the value used in the Application Diagram.

Display Dancing

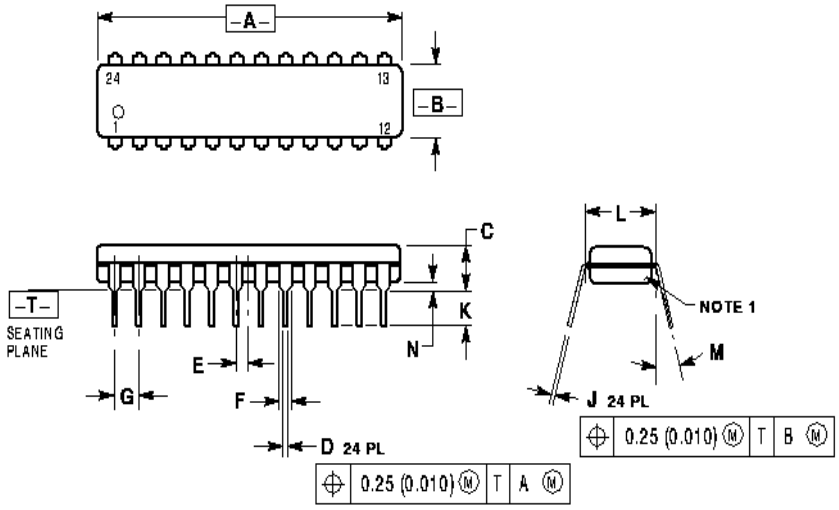
Most display dancing is caused by interference of the serial bus. It can be avoided by adding resistors in the bus in series.

APPLICATION DIAGRAM



PACKAGE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE(DUAL IN-LINE PACKAGE)
CASE 724-03



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

CASE 724–03
ISSUE D

DATE 07/15/87