TC74HC365AP/AF
TC74HC366AP/AF

HEX Bus Buffer
TC74HC365 Non-Inverted
TC74HC366 Inverted

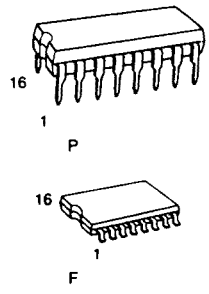
The TC74HC365A and TC74HC366A are high speed CMOS 3-STATE BUFFERs fabricated with silicon gate C^2MOS technology.

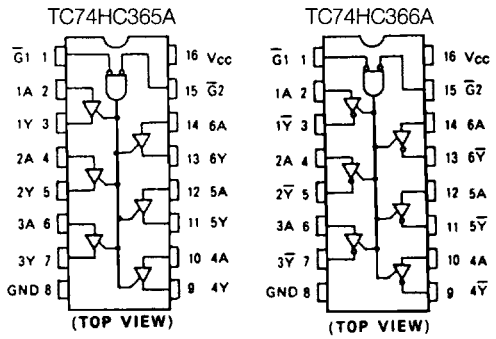
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC365A is an inverting type, while the TC74HC366A is non-inverting.

All six buffers are controlled by the combination of two enable inputs ($\overline{G}1$ and $\overline{G}2$); the outputs of these buffers are enabled only when both $\overline{G}1$ and $\overline{G}2$ inputs held low, and at the other combinations, these outputs are disabled to the high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.





Pin Assignment

Features

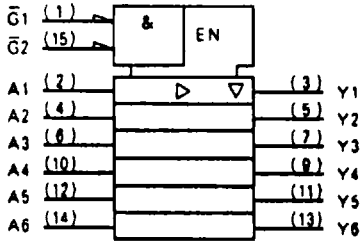
- High Speed: t_{pd} = 9ns(Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}(Min.)
- Output Drive Capability: 15 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 6mA(Min.)
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: V_{CC}(opr) = 2V~6V
- Open Drain Structure
- Pin and Function Compatible with 74LS365/366

Truth Table

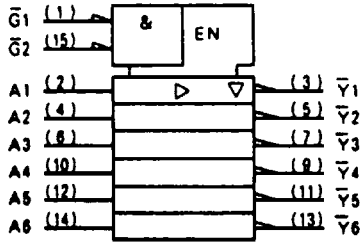
Inputs			Outputs	
$\overline{G}1$	$\overline{G}2$	An	Yn(365A)	$\overline{Y}n$(366A)
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

X: Don't Care
Z: High Impedance

TC74HC365A



TC74HC366A



IEC Logic Symbol

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC} = 2.0V) 0 ~ 500(V_{CC} = 4.5V) 0 ~ 400(V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		V_{CC}	Ta = 25°C Min.	Ta = 25°C Typ.	Ta = 25°C Max.	Ta = -40 ~ 85°C Min.	Ta = -40 ~ 85°C Max.	Unit
High-Level Input Voltage	V_{IH}	–		2.0 4.5 6.0	1.5 3.15 4.2	– – –	– – –	1.5 3.15 4.2	– – –	V
Low-Level Input Voltage	V_{IL}	–		2.0 4.5 6.0	– – –	– – –	0.5 1.35 1.8	– – –	0.5 1.35 1.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	V
			I_{OH} = -6 mA I_{OH} = -7.8mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	– –	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
			I_{OL} = 6 mA I_{OL} = 7.8mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	–	–	±0.5	–	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	–	–	4.0	–	40.0	

AC Electrical Characteristics (Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition			Ta = 25°C			Ta = -40 ~ 85°C		Unit
			CL	V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	–	50	2.0 4.5 6.0	– – –	20 6 5	60 12 10	– – –	75 15 13	ns
Propagation Delay Time	t_{pLH}	–	50	2.0 4.5 6.0	– – –	38 12 10	90 18 15	– – –	115 23 20	
	t_{pHL}		150	2.0 4.5 6.0	– – –	51 17 14	130 26 22	– – –	165 33 28	
Output Enable Time	t_{pZH}	–	50	2.0 4.5 6.0	– – –	56 17 14	130 26 22	– – –	165 33 28	
	t_{pZH}		150	2.0 4.5 6.0	– – –	69 22 17	170 34 29	– – –	215 44 37	
Output Disable Time	t_{pLZ} t_{pHZ}	–	50	2.0 4.5 6.0	– – –	42 18 15	130 26 22	– – –	165 33 28	MHz
Input Capacitance	C_{IN}	–			–	5	10	–	10	pF
Output Capacitance	C_{OUT}	–			–	10	–	–	–	
Power Dissipation Capacitance	C_{PD}(1)	–			–	25	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/6$(per Gate)