

STRUCTURE	Silicon Monolithic Integrated Circuits
PRODUCT SERIES	3 in 1 Motor Driver for Digital Video Camera
TYPE	BD6637KV BD6637KS
FUNCTIONS	3-phase motor driver for capstan , 3-phase sensor-less motor driver for cylinder, - Reversible motor driver for loading

○ABSOLUTE MAXIMAM RATINGS (Ta=25°C)

Parameter	Symbol	Limit	Unit
Supply voltage	VCC	7	V
	UNREG	15	V
	C_VM	10	V
	D_VM	10	V
	L_VM	7	V
Power dissipation	Pd	1250 *	mW
Operate temperature	Topr	-25~+75	°C
Storage temperature	Tstg	-40~+150	°C
Output max current	IOMAX	1000 * *	mA
Junction temperature	Tjmax	150	°C

* 70mm×70mm×1.6mm glass epoxy board.Derating in done at 10mW/°C for operating above Ta=25°C

* * However, do not exceed Pd, ASO and Tj=150°C(Common to 3 drivers)

○OPERATING CONDITIONS

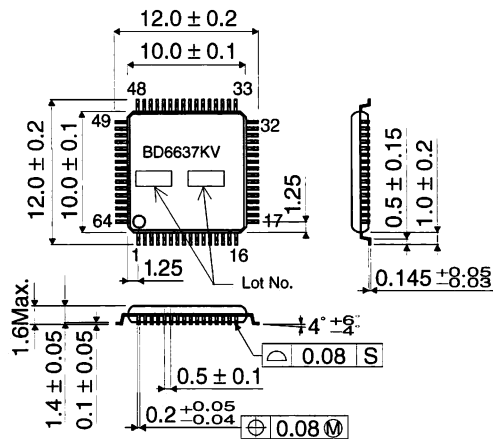
Parameter	Symbol	Limit	Unit
Supply voltage	VCC	2.7~4.5	V
	UNREG	5~12 *	V
	C_VM	0~8 *	V
	D_VM	0~8 *	V
	L_VM	4.5~5.5	V

* UNREG≥C_VM,UNREG≥D_VM, L_VM≥VCC

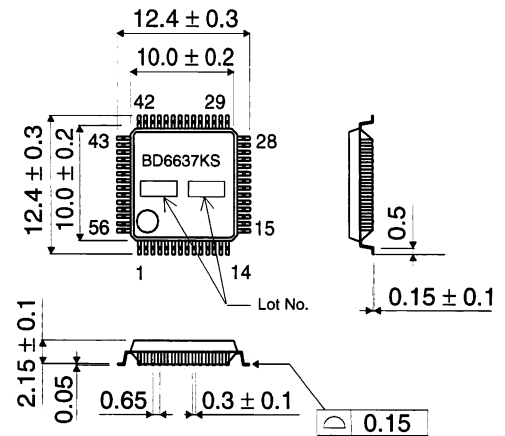
○ELECTRICAL CHARACTERISTICS (Unless otherwise specified Ta=25°C, VCC=3V, C_VM=D_VM=L_VM=5V, UNREG=7.2V)

Parameter		Symbol	Limit			Unit	Conditions
			Min.	Typ.	Max.		
TOTAL	VCC Circuit current 1	ICC1	6	13	20	mA	Power save OFF
	VCC Circuit current 2	ICC2	—	—	5	μA	Power save ON
	UNREG Stand by current	IUNREG	—	—	5	μA	Power save ON
	PS input switching level	PS	0.6	1.4	2	V	
	VG voltage	VG	9.5	11	12.5	V	
CAPSTAN OUTPUT	Output H voltage	C_VOH	—	0.35	0.55	V	IOUT=−400mA
	Output L voltage	C_VOL	—	0.4	0.65	V	IOUT=400mA
CAPSTAN HALL AMP	In-phase input voltage range	C_VCM	1.2	—	VCC-1.1	V	
	Hall input offset voltage	C_VHOFS	-15	—	15	mV	
CAPSTAN TORQUE CONTROL	EC input bias current	C_IEC	—	3.0	7.5	μA	C_EC=VCC
	Torque control input/output gain	C_GIO	0.35	0.50	0.65	A/V	C_RNF=0.33Ω,C_RCC=3.3kΩ
	Torque control start voltage	C_VECOFS	1.05	1.2	1.35	V	
	Current limit voltage	C_CLIMIT	0.20	0.24	0.28	V	C_RNF=0.33Ω,C_RCC=3.3kΩ
	Ripple Cancel Ratio	C_VRCC	8	20	32	%	IOUT=200mA,C_RCC=3.3k, C_RNF=0.33Ω
CAPSTAN VS	Voltage gain	C_GVS	7	8	9	TIMES	
	Output H voltage	C_VVSOH	—	0.5	0.8	V	IOVS=−1mA, between VCC and output voltage
	Output L voltage	C_VVSOL	—	0.13	0.2	V	IOVS=50μA
	VS offset voltage	C_VVSOFS	0.12	0.25	0.38	V	DC/DC×3 in use
CAPSTAN FGAMP	Input offset voltage	C_VFGOFS	-12	—	12	mV	
	DC bias voltage	C_VFG+	1/2VCC-0.2	1/2VCC	1/2VCC+0.2	V	
	Voltage gain 1	C_AV1	50	59	—	dB	f=3kHz
	Voltage gain 2	C_AV2	30	36	—	dB	f=50kHz
	In-phase input voltage range	C_VFGCM	0.35	—	VCC-1.1	V	
	Output H voltage	C_VFGAOH	—	0.3	0.5	V	IOH=−0.2mA, between VCC and output voltage
	Output L voltage	C_VFGAOL	—	0.1	0.3	V	IOL=1mA
	C_FG hysteresis width	C_VFGHYS	±30	±46	±62	mV	
CAPSTAN FGHYS	DC bias voltage	C_VFG+	1/2VCC-0.2	1/2VCC	1/2VCC+0.2	V	
	Output L voltage	C_VFGSOL	—	0.1	0.3	V	IOL=1mA
DRUM OUTPUT	Output H voltage	D_VOH	—	0.3	0.5	V	IOUT=−400mA
	Output L voltage	D_VOL	—	0.4	0.65	V	IOUT=400mA
DRUM TORQUE CONTROL	EC input bias current	D_IEC	—	2.0	5.0	μA	D_EC=VCC
	Torque control input/output gain	D_GIO	0.45	0.66	0.87	A/V	D_RNF=0.33Ω
	Torque control start voltage	D_VECOFS	1.05	1.2	1.35	V	
	Current limit voltage	D_CLIMIT	0.217	0.274	0.332	V	D_RNF=0.33Ω
DRUM STARTING/DETECTION/ SLOPE	DETECT terminal charge current	D_IDETO	2	5	10	μA	
	DETECT terminal discharge current	D_IDETI	2	5	10	μA	
	DETECT terminal H voltage	D_VDETH	1.1	1.3	1.5	V	
	DETECT terminal L voltage	D_VDETL	0.5	0.65	0.8	V	
	ISET voltage	D_VISET	0.32	0.4	0.48	V	RD_ISET=18kΩ
	SL1,2 charge current	D_ISLO	16	22	28	μA	RD_ISET=18kΩ
	SL1,2 discharge current	D_ISLI	17	24	31	μA	RD_ISET=18kΩ
	SL1,2 H voltage	D_VSLH	2.5	2.8	—	V	
	SL1,2 L voltage	D_VSLL	0.85	1.0	1.15	V	
	SL switching EC level	D_VECSL	1.6	2.0	2.4	V	
	Output H voltage	D_VVSOH	—	0.5	0.8	V	IOVS=−1mA, between VCC and output voltage
DRUM VS	Output L voltage	D_VVSOL	—	0.13	0.2	V	IOVS=50μA
	VS offset voltage	D_VVSOFS	0.12	0.25	0.38	V	DC/DC×3 in use
	Input offset voltage	D_VFGOFS	-12	—	12	mV	
	DC bias voltage	D_VFG+	1/2VCC-0.2	1/2VCC	1/2VCC+0.2	V	
DRUM FGAMP	Voltage gain 1	D_FAV1	50	59	—	dB	f= 3kHz
	Voltage gain 2	D_FAV2	30	36	—	dB	f= 50kHz
	In-phase input voltage range	D_VFGCM	0.35	—	VCC-1.1	V	
	Output H voltage	D_VFGAOH	—	0.3	0.5	V	IOH=−0.2mA, between VCC and output voltage
	Output L voltage	D_VFGAOL	—	0.15	0.35	V	IOL=1mA
	D_FG hysteresis width	D_VFGHYS	±84	±110	±136	mV	
	DC bias voltage	D_VFG+	1/2VCC-0.2	1/2VCC	1/2VCC+0.2	V	
	Output L voltage	D_VFGSOL	—	0.1	0.3	V	IOL=1mA
DRUM PGAMP	Input offset voltage	D_VPGOFS	-12	—	17	mV	
	DC bias voltage	D_VPG+	1/2VCC-0.2	1/2VCC	1/2VCC+0.2	V	
	Voltage gain 1	D_PAV1	50	59	—	dB	f= 3kHz
	Voltage gain 2	D_PAV2	30	36	—	dB	f= 50kHz
	In-phase input voltage range	D_VPGCM	0.35	—	VCC-1.1	V	
	Output H voltage	D_VPGAOL	—	0.3	0.5	V	IOH=−0.2mA, between VCC and output voltage
	Output L voltage	D_VPGAOL	—	0.15	0.35	V	IOL=1mA
	D_PG hysteresis width	D_VPGHYS	±118	±144	±170	mV	
DRUM PGHYS	DC bias voltage	D_VPG+	1/2VCC-0.2	1/2VCC	1/2VCC+0.2	V	
	Output L voltage	D_VPGSOL	—	0.1	0.3	V	IOL=1mA
LOADING	Output saturation voltage	L_VSAT	—	0.1	0.3	V	IOUT=200mA, L_REF=L_VM, Total saturation voltage of low and high side output transistor
	L_REF pin input current	L_IREF	—	0.3	2	μA	
	Vout-L_REF offset	L_VOFS	0	100	200	mV	

○Package outline(Plastic Mold)

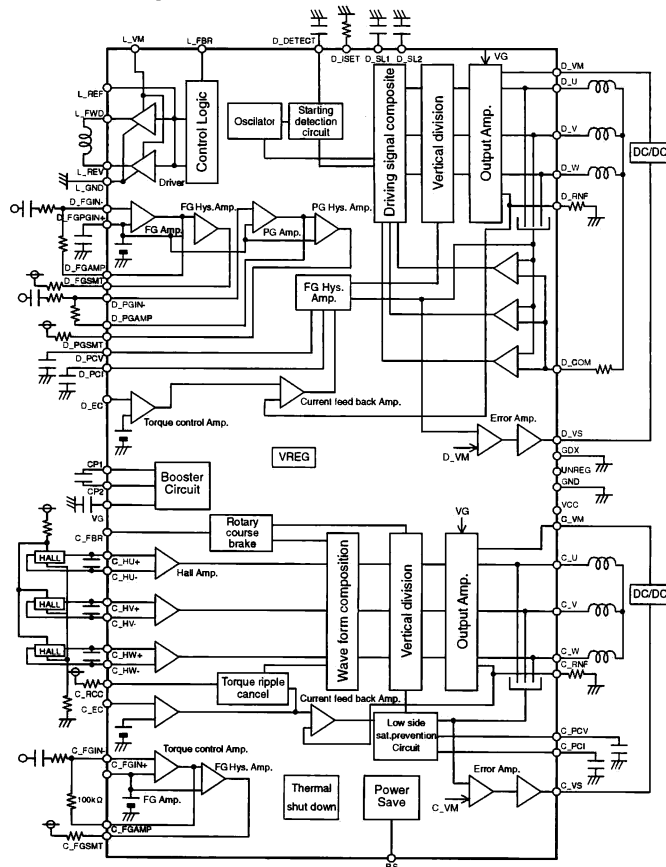


BD6637KV[VQFP64(Unit:mm)]



BD6637KS[SQFP56(Unit:mm)]

○Block Diagram



○Terminal function table

PIN NO.	PIN Name (KV)	PIN Name (KS)	PIN NO.	PIN Name (KV)	PIN Name (KS)
1	N.C.	C_U	33	D_COM	D_W
2	C_U	C_V	34	D_U	L_FBR
3	C_V	C_RNF	35	D_V	L_REF
4	C_RNF	C_W	36	D_RNF	L_FWD
5	C_W	C_HU+	37	D_W	L_GND
6	N.C.	C_HU-	38	N.C.	L_REV
7	N.C.	C_HV+	39	L_FBR	L_VM
8	C_HU+	C_HV-	40	L_REF	C_FGIN+
9	C_HU-	C_HW+	41	L_FWD	C_FGIN-
10	C_HV+	C_HW-	42	N_C	C_FGAMP
11	C_HV-	D_PGSM T	43	L_GND	C_FGSM T
12	C_HW+	D_PGAMP	44	L_REV	VG
13	C_HW-	D_PGIN-	45	L_VM	CP1
14	D_PGSM T	D_FGPGIN+	46	C_FGIN+	CP2
15	D_PGAMP	D_FGIN-	47	C_FGIN-	GND
16	D_PGIN-	D_FGAMP	48	C_FGAMP	GDX
17	D_FGPGIN+	D_FGSM T	49	C_FGSM T	PS
18	D_FGIN-	VCC	50	N.C.	C_RCC
19	D_FGAMP	D_DETECT	51	VG	C_FBR
20	D_FGSM T	D_ISET	52	CP1	C_VM
21	VCC	D_SL1	53	CP2	C_VS
22	D_DETECT	D_SL2	54	N.C.	C_EC
23	D_ISET	UNREG	55	GND	C_PCI
24	D_SL1	D_VM	56	GDX	C_PCV
25	D_SL2	D_VS	57	PS	
26	UNREG	D_EC	58	C_RCC	
27	N.C.	D_PCI	59	C_FBR	
28	D_VM	D_PCV	60	C_VM	
29	D_VS	D_COM	61	C_VS	
30	D_EC	D_U	62	C_EC	
31	D_PCI	D_V	63	C_PCI	
32	D_PCV	D_RNF	64	C_PCV	

○ NOTES FOR USE

1) Absolute maximum ratings

When the absolute maximum rating of applied voltage, operation temperature range, etc is exceeded, destruction is possible. In case of destruction, short-circuit mode or open mode cannot be identified; therefore when special mode is envisioned where absolute maximum rating may be exceeded, please take a physical safety measure such as use of fuse.

2) Power supply line

Return of regenerated current is caused by back electromotive force of motor, therefore take a measure such as placing a capacitor between power supply and GND for routing regenerated current, and fully ensure that various characteristics of electric field capacitor have no problem such as pull-out capacity at a low temperature before determining a capacity value.

3) GND potential

Ensure that the potential of GND terminal is the minimum potential in any operating condition. Also ensure that all terminals except GND terminal do not fall below GND voltage including transient phenomenon. However, it is possible that the motor output terminal may deflect below GND because of influence by back electromotive force of motor. Trouble such as malfunction may possibly occur depending on use condition, environment, and property of individual motor. Fully make sure that no problem is found on operation of IC etc.

4) Thermal design

Consider the permissible loss (Pd) under actual use condition and apply thermal design with sufficient margin.

5) Operation in strong electromagnetic field

Use in strong electromagnetic field may cause malfunction. Be careful.

6) ASO

In using this IC, perform setting so that the output Tr does not exceed the absolute maximum rating and ASO.

7) Thermal shut down circuit

This IC is built in the protection of IC and power supply circuit and so on, and Thermal shut down circuit for safety. Operation temperature is to 175°C(Typ) and hysteresis width is 25°C(Typ). The condition of Output terminal is OPEN when chip temperature of IC rise and TSD circuit operate. Please be careful as this is effective against being due to output current like exceeding power dissipation and short of output, but is not effective in case of flowing large current into IC generating heat by internal destruction of IC and short during terminal.

8) GND wiring pattern

When there are small signal GND and large current GND, separate the large current GND pattern from small signal GND pattern. It is recommended to apply one-point grounding at the reference point of the set in order that resistance of wiring pattern and large current do not cause change of voltage of small signal GND. Please be cautious not to fluctuate the wiring pattern of GND of external mounted parts.

9) Capacitor between output and GND

When a large capacitor is connected between output and GND, if Vcc is shorted with 0V or GND for some cause, it is possible that the current charged in the capacitor may flow into the output resulting in destruction. Keep the capacitor between output and GND below 100uF.

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