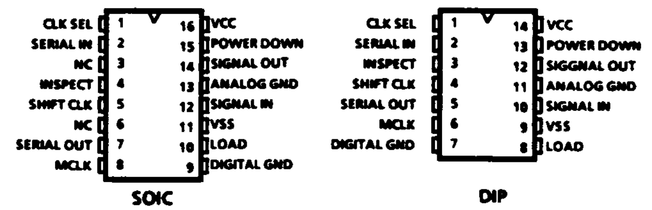
TEL 5500 PROGRAMMABLE TELEPHONE LINE EQUALIZER



PIN CONFIGURATIONS

PRELIMINARY INFORMATION

Features

- Provides Telco type Equalization
- Serially Programmable Transfer Function (Slope, Bandwidth and Height)
- Very Low Noise Level
- 60 Hz Rejection Filter
- By-Pass Mode
- Low Supply Current
- Low-Power Standby Mode
- Selectable Clock Frequency
- Diagnostic Inspection Capability
- Compatible with TEL 5100 Gain/Attenuator
- Low-Power CMOS
- DIP or SOIC

General Description

The TEL 5500 Programmable Telephone Line Equalizer is a monolithic CMOS integrated circuit which performs Telco type equalization on a telephone signal.

The Equalizer is composed of an arrangement of programmable switched capacitor filters for equalization, a high pass filter to remove 60 Hz interference, and an output smoothing filter.

Programming of the Equalizer's transfer function is accomplished by serially loading an internal register with a binary coded value which selects the slope, bandwidth and height of the switched capacitor filters.

Functional Description

The TEL 5500 contains a lead-lag filter and a second order bandpass filter. The break points of the lead-lag filter as well as the bandwidth and height of the bandpass filter are programmable. This configuration allows the user to program the transfer function of the Equalizer by selecting its slope, bandwidth and height.

Controlling the Transfer Function

A serially loadable register holds a binary coded value which selects the bandwidth and height of the bandpass filter, providing ready selection of filter characteristics in the telephone passband.

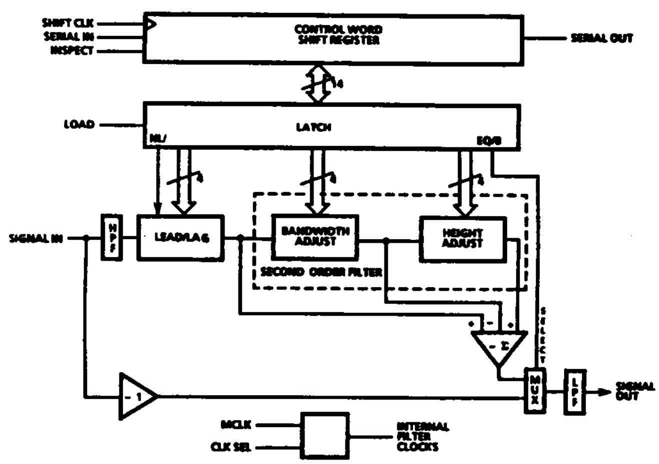
The upper and lower break points of the lead-lag filter are similarly selected by programming a binary coded value into a separate bit field in the register. This adjusts the base amplitude of the equalized signal.

The in band transfer response of the Equalizer is given below:

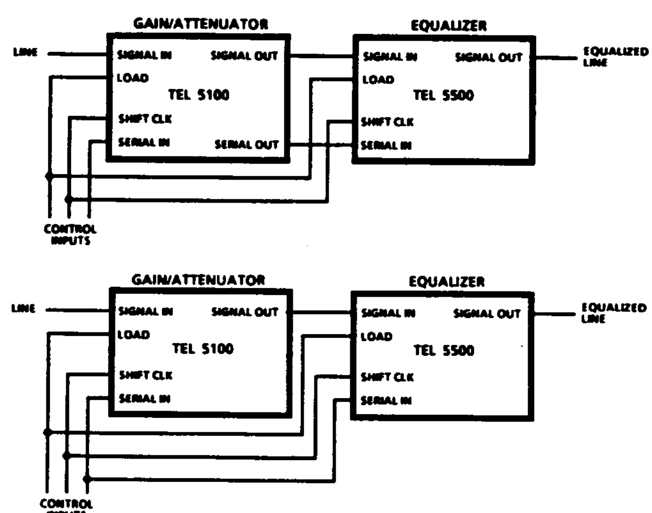
$$H(s) = \left(\frac{-s}{s+a}\right)\left(\frac{c(s+b)}{b(s+c)}\right)\left(\frac{[s^2 + h(\omega_0/Q)s + \omega_0^2]}{[s^2 + (\omega_0/Q)s + \omega_0^2]}\right)$$

Where $a = 848.23$ and $\omega_0 = 20463.77$

EQUALIZER INTERNAL BLOCK DIAGRAM
FIGURE 1



TYPICAL TELEPHONE LINE INTERCONNECTIONS
FIGURE 2



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CONTROL REGISTER FUNCTION

BIT	NAME	FUNCTION
BIT 13 MSB	No Load/Load	This bit adjusts the upper and lower break points (b and c, respectively) of the lead-lag filter equally. If this bit is a '1', non-loaded cable compensation is selected. A '0' selects loaded cable compensation.
BITS 12-9	Slope 8, 4, 2, 1	The slope bits determine the lower break point (b) of the lead-lag filter and hence the gain between 300 Hz and 2.5 KHz. (See Table 1.)
BITS 8-5	Bandwidth 8, 4, 2, 1	The bandwidth bits affect the spread of the equalized signal around 3250 Hz by changing the Q of the second order filter. (See Table 2.)
BITS 4-1	Height 8, 4, 2, 1	These bits control the amplitude of the equalized signal at 3250 Hz by adjusting the Q of the numerator of the second order filter relative to the Q of the denominator. (See Table 3.)
BIT 0	EQualize/ BYpass	This bit determines whether SIGNAL OUT is equalized or passed through without equalization.

Table 1. Effect of Slope Bit Programming on Gain

SLOPE BIT 8421	TYP GAIN (dB)	TOLERANCE (dB)
0000	0	± 0.1
0001	1.4	± 0.2
0010	2.6	± 0.2
0100	4.7	± 0.2
1000	7.8	± 0.2
1111	11.4	± 0.25

1 kHz sinusoidal input; EQ/BY = 1, NL/L = 0, B8-B1 = 0000, H8-H1 = 0000

SLOPE BIT 8421	TYP GAIN (dB)	TOLERANCE (dB)
0000	0	± 0.1
0001	0.4	± 0.2
0010	0.9	± 0.2
0100	1.8	± 0.2
1000	3.7	± 0.2
1111	6.6	± 0.25

1 kHz sinusoidal input; EQ/BY = 1, NL/L = 1, B8-B1 = 0000, H8-H1 = 0000

Table 2. Effect of Bandwidth Bit Programming on Q

SLOPE BIT 8421	TYP Q (dB)	TOLERANCE (dB)
0000	16.1	± 2
0001	14.2	± 1.5
0010	12.6	± 1.5
0100	9.1	± 1.0
1000	3.6	± 0.5
1111	1.2	± 0.35

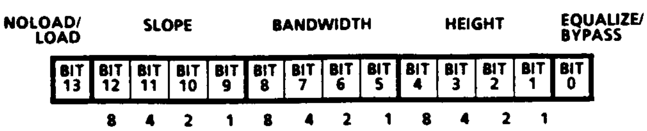
1 kHz sinusoidal input; EQ/BY = 1, NL/L = 0, S8-S1 = 0000, H8-H1 = 1111

Table 3. Effect of Height Bit Programming on Gain

SLOPE BIT 8421	TYP GAIN (dB)	TOLERANCE (dB)
0000	0.1	± 0.2
0001	0.7	± 0.2
0010	1.3	± 0.2
0100	2.5	± 0.2
1000	5.9	± 0.3
1111	11.4	± 0.3

1 kHz sinusoidal input; EQ/BY = 1, NL/L = 0, S8-S1 = 0000, B8-B1 = 0000

CONTROL REGISTER BIT ASSIGNMENT



Programming the Transfer Function

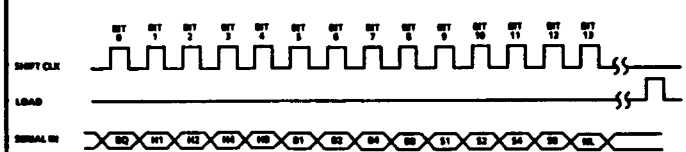
A fourteen bit control word is serially shifted into the TEL 5500's internal shift register, BIT 0 first, via the SERIAL IN input, clocked by the rising edge of SHIFT CLK. (See Figure 3.)

The control word is then transferred from the shift register into an internal latch by bringing the LOAD pin high while SHIFT CLK is low.

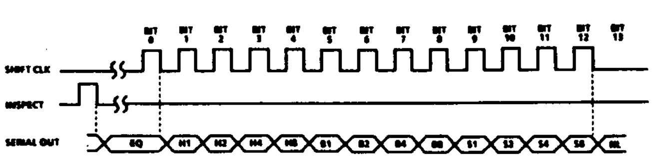
A new control word may be serially loaded into the shift register without affecting the contents of the latch.

The control word in the latch may be loaded back into the shift register for inspection. This is done by bringing the INSPECT pin high while SHIFT CLK is held low. The control word can then be shifted out, BIT 0 first, on the SERIAL OUT pin at the falling edge of SHIFT CLK. (See Figure 4.) The contents of the latch are not affected by this inspection procedure.

CONTROL REGISTER LOAD TIMING
FIGURE 3



CONTROL REGISTER INSPECT TIMING
FIGURE 4



PIN NAME	DESCRIPTION
CLK SEL	When low, this input causes the TEL 5500 to suppress every 193rd clock pulse internally, converting a 1.544 MHz input clock at the MCLK pin to a 1.536 MHz internal filter clock for accurate frequency response. If a 1.536 MHz clock is input directly to the MCLK pin, CLK SEL should be forced high or left unconnected, disabling clock suppression. This input has an internal pullup.
SERIAL IN	Serial data input for loading the slope of the lead-lag filter and the bandwidth and height of the second order band pass filter into the TEL 5500's shift register (Bit 0 first).
INSPECT	A high logic level on this input loads the shift register with the previously programmed slope, bandwidth and height values stored in the latch. This allows these values to be shifted out for inspection.
SHIFT CLK	The rising edge of this input clocks data serially into the internal shift register (Bit 0 first) for loading the slope of the lead-lag filter and the bandwidth and height of the second order band pass filter. The falling edge of this input clocks data out of the shift register (Bit 0 first) onto the SERIAL OUT pin for inspection.
SERIAL OUT	The previously programmed values for the slope of the lead-lag filter and the bandwidth and height of the second order filter may be shifted out (Bit 0 first) for inspection at this pin.
MCLK	1.536 MHz or 1.544 MHz master clock input. The CLK SEL input is used to indicate whether the clock frequency connected to the MCLK pin is 1.536 MHz or 1.544 MHz.
DIGITAL GND	Digital Ground.
LOAD	A high logic level on this input transfers the slope, bandwidth and height values previously shifted into the internal shift register via the SERIAL IN pin into the internal latch where they determine the transfer function of the internal filters.
VSS	Negative Power Supply Terminal.
SIGNAL IN	Telephone signal requiring equalization.
ANALOG GND	Analog Ground.
SIGNAL OUT	Equalized telephone signal.
POWER DOWN	This active high input puts the TEL 5500 into Low-Power Standby mode. In this mode the SIGNAL OUT pin is forced to a high impedance. The digital communication section of the TEL 5500 remains operable in this mode.
VCC	Positive Power Supply Terminal.

Input Filtering: A high pass filter on the input rejects 60 Hz interference.

Clock Suppression: Forcing the CLK SEL input low causes the TEL 5500 to internally suppress every 193rd clock pulse, converting a 1.544 MHz input clock at the MCLK pin to a 1.536 MHz internal filter clock for accurate frequency response. If a 1.536 MHz clock is input directly to the MCLK pin, clock suppression should be disabled by forcing CLK SEL high or leaving it unconnected.

By-Pass Mode: Programming the least significant bit of the control register to a logic low level causes the TEL 5500 to pass the input signal as presented to the SIGNAL IN pin through to the SIGNAL OUT pin without performing equalization, bypassing the switched capacitor filters.

Low-Power Standby Mode: Holding the POWER DOWN input high puts the TEL 5500 into its Low-Power Standby mode. In this mode the analog circuitry is switched to a low powermode, and the SIGNAL OUT pin is put into a high impedance state. The digital circuitry, including the transfer function control register and associated circuitry, is operable when the TEL 5500 is in Low-Power Standby mode. It is not necessary to provide a clock signal to the MCLK input when in Low-Power Standby mode.

Output Smoothing Filter: A low pass smoothing filter reconstructs the signal at the output of the second order switched capacitor filter.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those limits which, if exceeded, may cause damage to the device. Proper operation is not implied at these limits.

Supply Voltage	
V_{cc}	+6.5V
V_{ss}	−6.5V
Voltage difference between ANALOG GND and DIGITAL GND	±0.5V
Positive Voltage at any pin, with respect to GND	
Analog inputs and outputs	V_{cc} + 0.3V
Digital inputs and outputs	V_{cc} + 0.3V
Negative Voltage at any pin, with respect to GND	
Analog inputs and outputs	V_{ss} − 0.3V
Digital inputs and outputs	DIGITAL GND −0.3V
Input Current on any pin	±10 mA
Power Dissipation	500 mW
Storage Temperature	−65 °C to +150 °C
Lead Temperature (Soldering, 10 sec.)	245 °C

OPERATING CONDITIONS

Operating Temperature	0 °C to +70 °C
Supply Voltage	
V_{cc}	+4V to +6V
V_{ss}	−4V to −6V

ELECTRICAL CHARACTERISTICS

Unless other noted, $T_{ambient}$ = 0 °C to 70 °C,
V_{cc} = +5V ± 10%,
V_{ss} = −5V ±10%,
MCLK frequency = 1.544 MHz ±300 Hz,
SIGNAL OUT R_{load} = 10 kOhms, SIGNAL OUT C_{load} = 75 pF.

ANALOG

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Center Frequency	3230	3250	3270	Hz	EQ/BY, H8-H1 = 1; All other Control Register Bits = 0.
Frequency Response (EQualization Mode)			±0.2	dB	From 1 kHz to 4 kHz; EQ/BY = 1; All other bits in Control Register = 0; 4 dBm input signal.
Frequency Response (BYpass Mode)			±0.1	dB	From 100 Hz to 4 kHz; All Control Register bits set to 0; 4 dBm input signal;
Gain Variation @1 kHz (EQualization Mode vs. BYpass Mode)			±0.1	dB	All Control Register bits except EQ/BY = 0.
Idle Channel Output Noise			10	dBrnC	NL/L = 1; All other Control Register bits = 0; Note 1.
Single Frequency Distortion (DC to 4 kHz output)			−46	dB	4.0 dBm input @1 kHz; EQ/BY = 1; All other bits in Control Register = 0.
Overload Compression Loss (Input to Output)					1004 Hz input; A8-A1, B8-B1, S8-S1 = 0.
EQualizationMode					EQ/BY = 1
			0.2	dB	SIGNAL IN = 1.23 Vrms
			0.2	dB	SIGNAL IN = 1.75 Vrms
			0.6	dB	SIGNAL IN = 2.48 Vrms
			1.8	dB	SIGNAL IN = 3.50 Vrms
BYpass Mode					EQ/BY = 0
			0.1	dB	SIGNAL IN = 1.23 Vrms
			0.1	dB	SIGNAL IN = 1.75 Vrms
			0.5	dB	SIGNAL IN = 2.48 Vrms
			1.7	dB	SIGNAL IN = 3.50 Vrms
60 Hz Rejection Filter Frequency Cutoff (3 dB)		135		Hz	
Power Supply Rejection Ratio (PSRR)					100 mV p-p 1 kHz sinusoid; SIGNAL IN = 0V. All control register bits = 0.
V_{cc}	25			dB	
V_{ss}	25			dB	
Offset Voltage			±100	mV	SIGNAL IN = 0V.
SIGNAL IN Input Impedance	100			kOhm	
SIGNAL OUT Load Impedance			10	kOhm	
SIGNAL OUT Load Capacitance			75	pF	

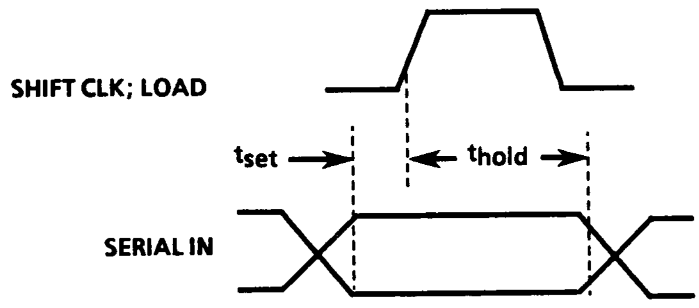
NOTE 1: The idle channel output noise specified in dBrnC corresponds to a measurement made driving a 600 Ohm output load. This translates to a 77.5µVrms C-message weighted output noise signal with the output driving the maximum specified output load of 10 KOhm and 75 pF.

DC CHARACTERISTICS

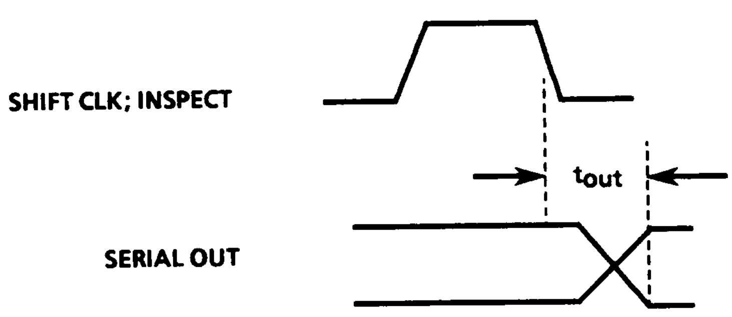
PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Positive Supply Current (I_{cc})			8	mA	No output load; V_{IL} = DIGITAL GND, $V_{IH} = V_{cc}$, SIGNAL IN = 0V.
Negative Supply Current (I_{ss})			−8	mA	No output load; V_{IL} = DIGITAL GND, $V_{IH} = V_{cc}$, SIGNAL IN = 0V.
Positive Power Supply Standby Current ($I_{cc_{standby}}$)			0.5	mA	No output load; V_{IL} = DIGITAL GND, $V_{IH} = V_{cc}$, SIGNAL IN = 0V.
Negative Power Supply Standby Current ($I_{ss_{standby}}$)			−0.5	mA	No output load; V_{IL} = DIGITAL GND, $V_{IH} = V_{cc}$, SIGNAL IN = 0V.
Output Voltage, Digital Outputs					
V_{OH}	2.4			V	$I_{OH} = -1.0$ mA
V_{OL}			0.4	V	$I_{OL} = 2.0$ mA
Input Voltage, digital Inputs					
V_{IH}	2.0			V	
V_{IL}			0.8	V	
Input Current (I_L), CLK SEL	−5		−100	uA	$V_{IN} = 0V$
Input Leakage Current (I_{LL}), Digital Inputs, except CLK SEL			± 1	uA	

AC CHARACTERISTICS

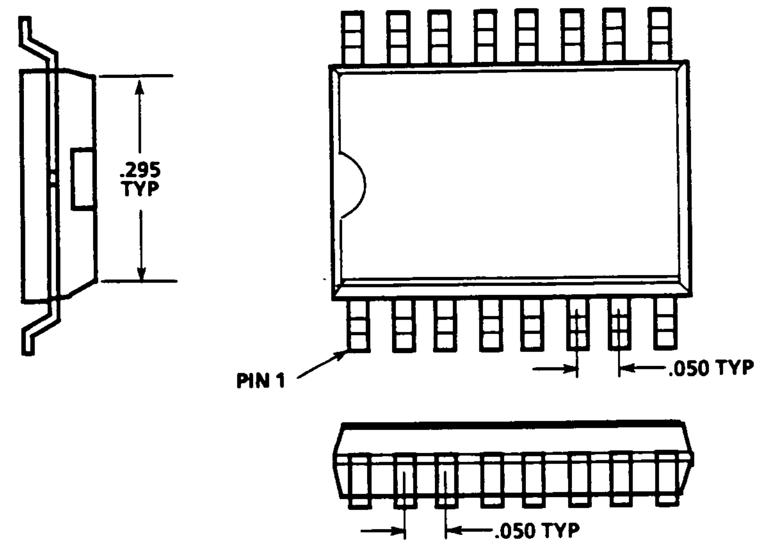
PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
MCLK Frequency		1.544		MHz	CLK SEL low
		1.536		MHz	CLK SEL high
MCLK Duty Cycle	45	50	55	%	
Pulse Width (t_{pw})					
SHIFT CLK	290			ns	
LOAD	290			ns	
INSPECT	290			ns	
SERIAL IN Set Up Time, with respect to rising edge of SHIFT CLK, LOAD, INSPECT (t_{set})	200			ns	
SERIAL IN Hold Time, with respect to rising edge of SHIFT CLK, LOAD, INSPECT (t_{hold})	315			ns	
SERIAL OUT Propagation Delay (t_{out})			125	ns	C = 35 pF
Delay Between SHIFT CLK and LOAD, INSPECT	310			ns	



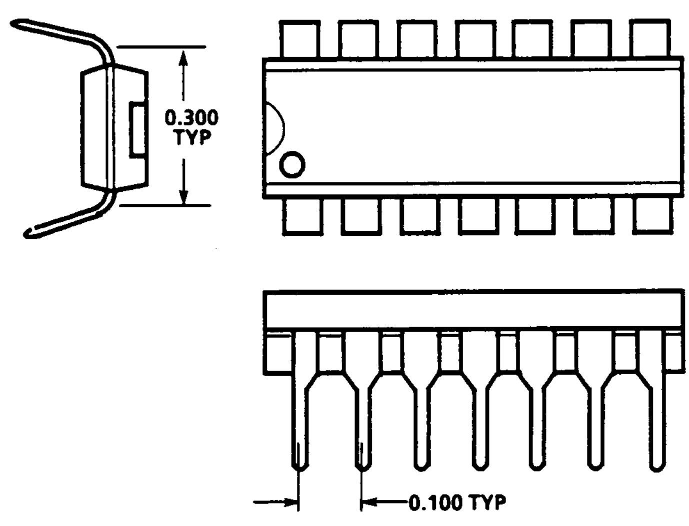
SERIAL INPUT TIMING



SERIAL OUTPUT TIMING



SOIC



DIP

TEL 5500 PACKAGE CONFIGURATIONS

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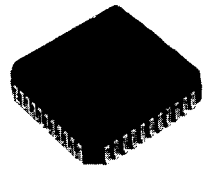
PACKAGES



DUAL IN-LINE PACKAGES (DIP)

PLASTIC DIP	8 through 24 (300 mil); 24 through 48 (600 mil); 64 (900 mil)
CERAMIC DIP, SIDE BRAZED	8 through 24 (300 mil); 24 through 48 (600 mil); 64 (900 mil)
CERDIP	8 through 24 (300 mil); 24 through 48 (600 mil)

SURFACE MOUNT PACKAGES

SOIC	8 through 16 (150 mil); 16 through 28 (300 mil)
PLCC	20 through 84
QUAD FLAT PACK	44 through 208
BUMPERED QFP	100 and up
CHIP CARRIER (LCC)	18 through 68
CERAMIC QFP	44 through 160 (EIJ); 132 through 164 (JEDEC)
CERFLAT	14 through 28
CERQUAD	20 through 68

PIN GRID ARRAYS

PLASTIC PGA	28 through 244
PGA	28 through 244

This is a partial list; consult factory for availability of other packages.
NOTE: Devices are available in anti-static tubes or trays, on tape & reel, or in die form.