VITESSE

VSC7139
Data Sheet

Quad Transceiver for Gigabit Ethernet and Fibre Channel

FEATURES

- Four Complete Transmitter/ Receiver Functions in a Single Integrated Circuit
- Full Fibre Channel (T11) and Gigabit Ethernet (IEEE 802.3z) Compliance
- 1.05 Gbps to 1.36 Gbps Operation per Channel
- Common or Per-Channel Transmit Byte Clocks
- TTL or PECL Reference Clock Input
- 1/10th or 1/20th Baud Rate Recovered Clocks
- Common and Per-Channel, Serial and Parallel Loopback Controls
- Common Comma Detect Enable Inputs
- Per-Channel Comma Detect Outputs
- Cable Equalization in Receivers
- Automatic Lock-to-Reference
- 3.3 V Power Supply, 2.67 W Max Power Dissipation
- 208-Pin, 23 mm TBGA Packaging

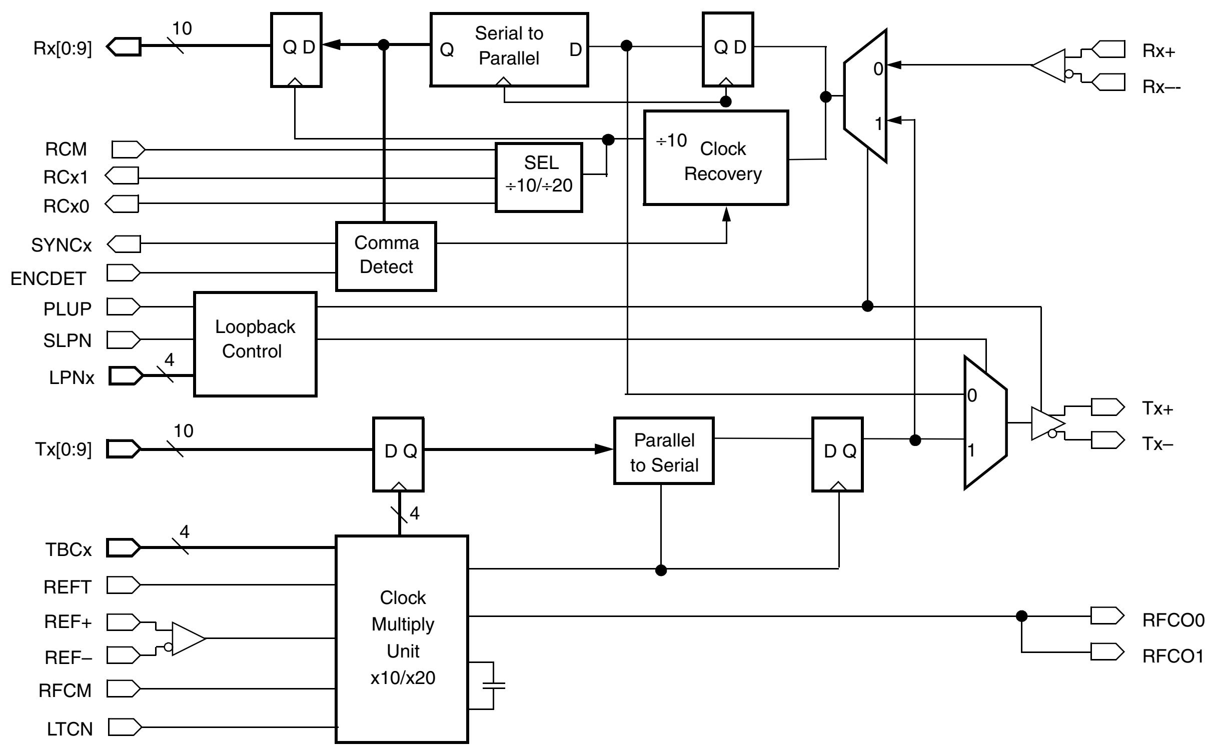
APPLICATIONS

- Fibre Channel
- Gigabit Ethernet Serial Backplanes
- Hubs/Switches

GENERAL DESCRIPTION

The VSC7139 is a full-speed Quad Fibre Channel and Gigabit Ethernet Transceiver IC. Each of the four transmitters has a 10-bit wide bus, running up to 136 MHz that accepts 8B/10B encoded transmit characters and serializes the data onto high-speed differential outputs at speeds up to 1.36 Gbps. The transmit data can be synchronous to the reference clock, a common transmit byte clock or a per-channel transmit byte clock. Each receiver samples serial receive data, recovers the clock and data, deserializes it into 10-bit receive characters, outputs a recovered clock and detects “comma” characters. The VSC7139 contains on-chip (PLL) circuitry for synthesis of the baud-rate transmit clock and extraction of the clocks from the received serial streams.

VSC7139 Block Diagram



Functional Descriptions

Notation

In this document, each of the four channels are identified as Channel A, B, C or D. When discussing a signal on any specific channel, the signal will have the channel letter embedded in the name, e.g., TA[0:9]. When referring to the common behavior of a signal that is used on each of the four channels, a lower case “x” is used in the signal name, e.g., Tx[0:9]. Differential signals, e.g., RA+ and RA–, may be referred to as a single signal, e.g., RA, by dropping reference to the “+” and “–.” REF refers to either the TTL input REFT, or the PECL differential inputs REF+/REF–, whichever is used.

Clock Synthesizer

The VSC7139 clock synthesizer multiplies the reference frequency, provided on the REF input, by 10 or 20 to achieve a baud rate clock between 1.05 GHz and 1.36 GHz. The reference clock input can be either TTL or PECL. If the reference clock input is TTL, connect to REFT. Additionally, connect REF+ to V_{DD} using a 10k Ω resistor and leave REF– open. If the reference clock input is PECL, connect the PECL inputs to REF+ and REF– . Leave REFT open or tie it HIGH through a 10k Ω resistor. The internal clock presented to the clock synthesizer is a logical XNOR of REFT and REF+/–. The reference clock will be active HIGH if the unused input is HIGH. The reference clock is active LOW if the unused input is LOW. REFT has an internal pull-up resistor. Internal biasing resistors set the proper DC level on REF+/–, therefore AC-coupling may be used.

The TTL outputs, RFCO0 and RFCO1, provide a clock that is frequency-locked to the REF input. This clock is derived from the clock synthesizer and is always $1/10^{th}$ the baud rate, regardless of the state of the RFCM input.

The on-chip PLL uses a single external 0.1 µF capacitor, connected between CAP0 and CAP1 to control the loop filter. This capacitor should be a multilayer ceramic dielectric, or better, with at least a 5 V working voltage rating and a good temperature coefficient (NPO is preferred, but X7R is acceptable). These capacitors are used to minimize the impact of common-mode noise on the Clock Multiplier Unit (CMU), especially power supply noise. Higher value capacitors provide better robustness in systems. NPO is preferred because if an X7R capacitor is used, the power supply noise sensitivity will vary with temperature.

For best noise immunity, the designer may use a three-capacitor circuit; one differential capacitor between CAP0 and CAP1, C1, a capacitor from CAP0 to ground, C2, and a capacitor from CAP1 to ground, C3. Larger values are better, however, 0.1µF is adequate. If the designer cannot use a three-capacitor circuit, a single differential capacitor, C1, is adequate. These components should be isolated from noisy traces.

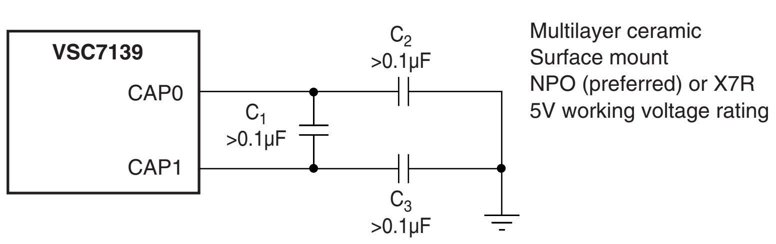


Figure 1. Loop Filter Capacitors (Best Circuit)

G52196-0, Rev 4.1
August 18, 2004

VITESSE

Serializer

The VSC7139 accepts TTL input data as a parallel 10-bit character on the Tx[0:9] bus, which is latched into the input register on the rising edge of either REF or TBCx. Three clocking modes are available and automatically detected by the VSC7139. If TBCC is static and RFCM is HIGH, all four Tx[0:9] busses are latched on the rising edges of REF. If TBCC is static and RFCM is LOW, then REF is multiplied by 20 and the input busses are latched on the rising edges of REF and at the midpoint between rising edges. If TBCC is toggling but TBCB is static, then all four Tx[0:9] busses are latched on the rising edges of TBCC. If TBCB and TBCC are both toggling, the rising edge of each TBCx latches the corresponding Tx[0:9] bus.

The active TBCC or TBCx inputs must be frequency-locked to REF. There is no specified phase relationship. Prior to normal data transmission, LTCN must be asserted LOW for 50 bit clocks so that the VSC7139 can lock to TBCx, which can result in corrupted data being transmitted. Once LTCN has been raised HIGH, the transmitters remain locked to REF and can tolerate +2 bit times of drift in TBCx relative to REF. If TBCC or TBCx drifts away from the reference clock by more than two bit clocks, corrupted data may also result and the LTCN pin should be asserted LOW again to perform another phase alignment. The latency from LTCN deassertion to TX serial output valid data is 50 bit clocks (bc). Figure 2 shows the LTCN to valid serial output data timing.

The 10-bit parallel transmission character will be serialized and transmitted on the Tx PECL differential outputs at the baud rate with bit Tx0 (bit a) transmitted first. User data should be encoded using 8B/10B or an equivalent code. The mapping to 10B encoded bit nomenclature and transmission order is shown in Table 1, along with the recognized comma pattern.

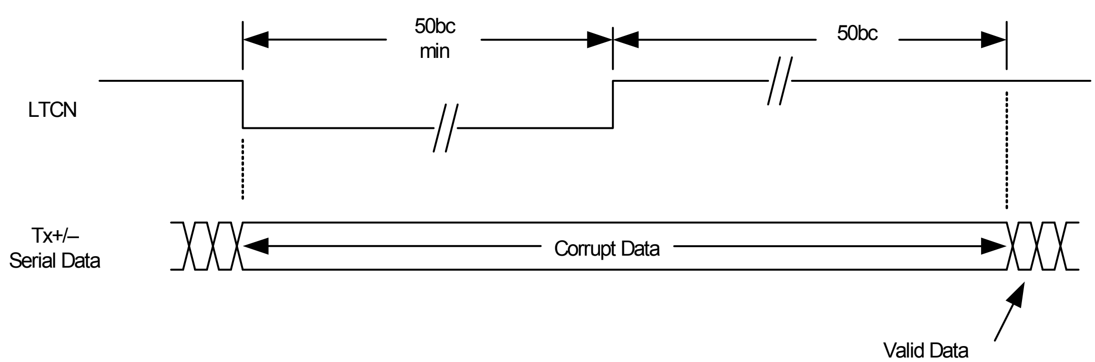


Figure 2. LTCN and Valid Serial Output Data Timing

Table 1. Transmission Order and Mapping of a 10B Character

Data Bit	Tx9	Tx8	Tx7	Tx6	Tx5	Tx4	Tx3	Tx2	Tx1	Tx0
10B Bit Position	j	h	g	f	i	e	d	c	b	a
Comma Character	x	x	x	1	1	1	1	1	0	0

Clock Recovery

The VSC7139 accepts differential high-speed serial inputs from the selected source (either the PECL Rx+/Rx– pins or the internal Tx+/– data), extracts the clock and retimes the data. Equalizers are included in the receiver to open the data eye and compensate for InterSymbol Interference (ISI) that may be present in the incoming data. The serial bit stream should be encoded so as to provide DC balance and limited run length by an 8B/10B encoding scheme. The digital Clock Recovery Unit (CRU) is completely monolithic and requires no external components. For proper operation, the baud rate of the data stream to be recovered should be within ±200 ppm of ten times the REF frequency. For example, Gigabit Ethernet systems would use 125MHz oscillators with a ±100 ppm accuracy resulting in ±200 ppm between VSC7139 pairs.

Deserializer

The recovered serial bit stream is converted into a 10-bit parallel output character. The VSC7139 provides complementary TTL recovered clocks, RCx0 and RCx1, which are at $1/20^{th}$ of the serial baud rate if RCM is LOW or $1/10^{th}$ if RCM = HIGH. The clocks are generated by dividing down the high-speed recovered clock, which is phase-locked to the serial data. The serial data is retimed, deserialized and output on Rx[0:9].

If serial input data is not present, or does not meet the required baud rate, the VSC7139 will continue to produce a recovered clock so that downstream logic may continue to function. The RCx0/RCx1 output frequency under these circumstances will differ from its expected frequency by no more than ±1%.

Word Alignment

The VSC7139 provides 7-bit comma character recognition and data word alignment. Word synchronization is enabled on all channels by asserting ENCDET HIGH. When synchronization is enabled, the receiver examines the recovered serial data for the presence of the comma pattern. This pattern is 0011111XXX, where the leading zero corresponds to the first bit received. The comma sequence is not contained in any normal 8B/10B coded data character or pair of adjacent characters. It occurs only within special characters, known as K28.1, K28.5 and K28.7, which are defined for synchronization purposes. Improper comma alignment is defined as any of the following conditions:

- The comma is not aligned within the 10-bit transmission character such that Rx[0:6] = 0011111.
- The comma straddles the boundary between two 10-bit transmission characters.
- The comma is properly aligned, but occurs in the received character presented during the rising edge of RCx0 rather than RCx1.

When ENCDET is HIGH and an improperly-aligned comma is encountered, the recovered clock is stretched, never slivered, so that the comma character and recovered clocks are aligned properly to Rx[0:9]. This results in proper character and word alignment. When the parallel data alignment changes in response to a improperly-aligned comma pattern, data which would have been presented on the parallel output port prior to the comma character, and possibly the comma character itself, may be lost. Possible loss of the comma character is data dependent, according to the relative change in alignment. Data subsequent to the comma character will always be output correctly and properly aligned. When ENCDET is LOW, the current alignment of the serial data is maintained indefinitely, regardless of data pattern.

On encountering a comma character, SYNCx is driven HIGH. The SYNCx pulse is presented simultaneously with the comma character and has a duration equal to the data. The SYNCx signal is timed such that it can be captured by the adjoining protocol logic on the rising edge of RCx1. Functional waveforms for synchronization are given in Figure 3. The first K28.5 shows the case where the comma is detected, but it is misaligned so a change in the output data alignment is required. Note that up to three characters prior to the comma character may be corrupted by the realignment process. The second K28.5 shows the case when a comma is detected and no phase adjustment is necessary. Figure 3 illustrates the position of the SYNCx pulse in relation to the comma character on Rx[0:9].

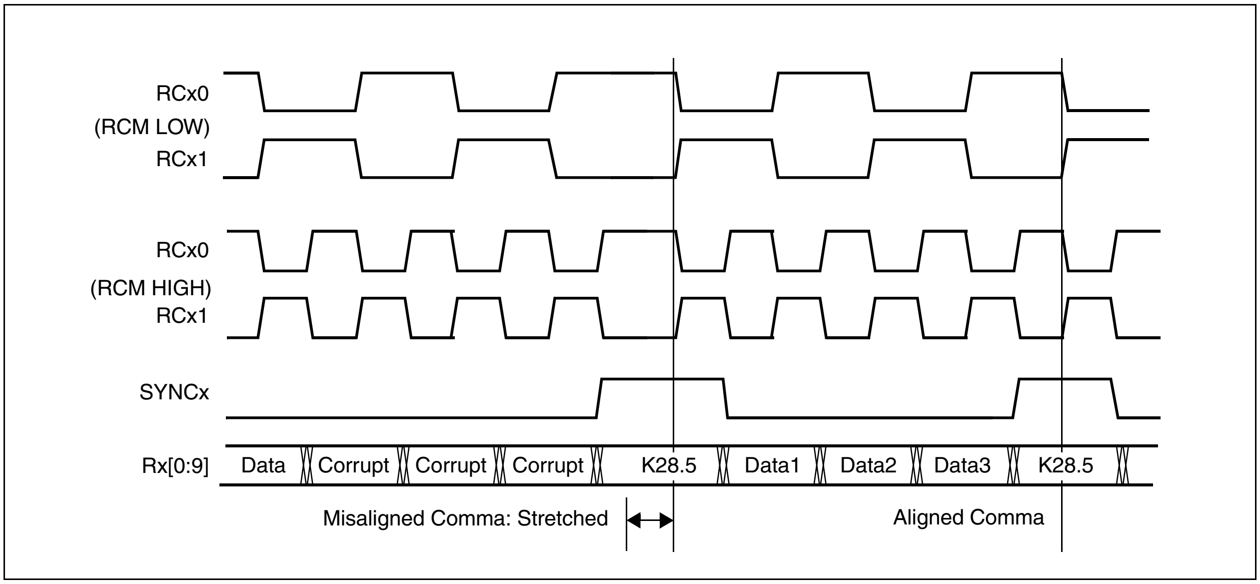


Figure 3. Misaligned and Aligned K28.5 Characters

Loopback Operation

There are four modes of Loopback operation that are controlled by the PLUP (Parallel Loopback), SLPN (Serial Loopback), and LPNx inputs (also see Table 2). The LPNx signals enable the selected loopback function (via PLUP and SLPN) on a per channel basis when LOW. If LPNx = 1, the state of PLUP and SLPN have no effect on that channel.

Normal SerDes Operation: Set PLUP = 0 and SLPN = 1 to configure the device for normal operation. The LPNx signals do not have an effect on this operation.

Parallel Loopback with Serial Outputs Disabled: Where Tx[0:9] parallel data in appears at the Rx[0:9] parallel data out. Set SLPN = 1 and PLUP = 1, and one or more of the LPNx signals to LOW. The Tx of the channel, where LPN = LOW, is internally looped to the Rx, and the transmitter output for that channel is Tx+ = HIGH and Tx– = LOW.

Parallel Loopback with Serial Outputs Enabled: Where Tx[0:9] parallel data in appears at the Rx[0:9] parallel data out, and Tx+/– serial out. Set SLPN = 0 and PLUP = 1, and one or more of the LPNx signals to LOW. The Tx[0:9] data for the selected channel(s) is serialized, looped to the receiver, deserialized and available at the Rx[0:9] parallel outputs. The serialized data is also looped back to from the receiver to the Tx+/– serial outputs.

Serial Loopback: Where Rx+/– serial data in appears at the Tx+/– serial data out. Set SLPN = 0 and PLUP = 0, and one or more of the LPNx signals to LOW. The Rx+/– serial data of the channel where LPN = LOW is internally looped to the Tx+/– serial outputs. Internal loopback occurs after the Clock Recovery Unit (CRU), and removes much of the jitter, however the signal at the TX+/– outputs may not meet the jitter specifications listed in the Table 4, “Transmitter AC Characteristics” on page 9 due to low-frequency jitter transfer.

Table 2. Loopback Selection

Loopback Mode	LPNx	PLUP	SLPN	Tranmitter Source	Receiver Source
Serial	LOW	LOW	LOW	Receiver	Receiver
Normal	LOW	LOW	HIGH	Transmitter	Receiver
Parallel with Outputs Enabled	LOW	HIGH	LOW	Transmitter	Transmitter
Parallel with Outputs Disabled	LOW	HIGH	HIGH	HIGH	Transmitter
Normal	HIGH	X	X	Transmitter	Receiver

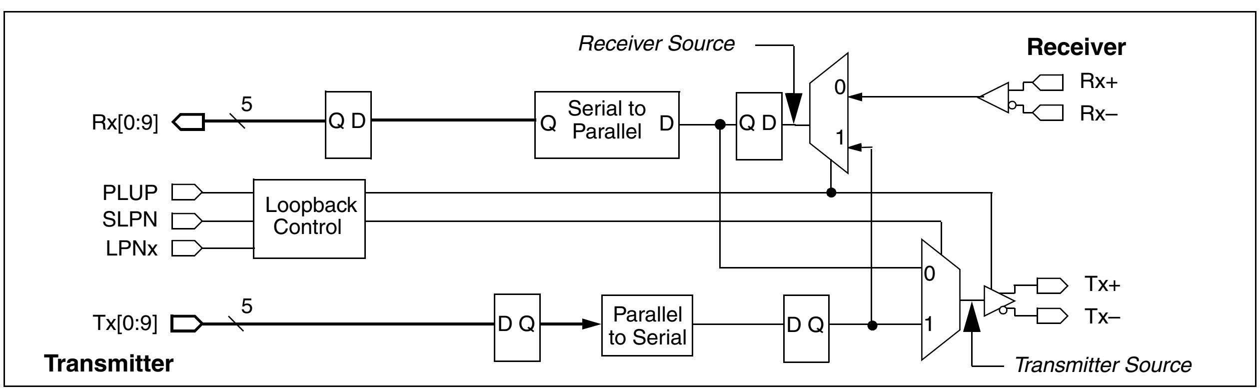


Figure 4. Loopback Diagram

JTAG Access Port

A JTAG Access Port is provided to assist in board-level testing. Through this port, most pins can be accessed or controlled and all TTL outputs can be tri-stated. Please contact your local Vitesse sales representative for the document, *VSC7139 JTAG Access Port Functionality*, which provides a full description of JTAG functions for this device.

SPECIFICATIONS

DC Characteristics

Over Recommended Operating Conditions.

Table 3. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Condition
TTL Outputs						
V_{OH}	TTL output HIGH voltage	2.4			V	I_{OH} = –4.0mA
V_{OL}	TTL output LOW voltage			0.5	V	I_{OL} = +4.0mA
I_{OZ}	TTL output leakage current			50	µA	When set to high-impedance state through JTAG
TTL Inputs						
V_{IH}	TTL input HIGH voltage	2.0		5.5	V	5V tolerant inputs
V_{IL}	TTL input LOW voltage	0		0.8	V	
I_{IH}	TTL input HIGH current		50	500	µA	V_{IN} = 2.4V
I_{IL}	TTL input LOW current			–500	µA	V_{IN} = 0.5V
PECL Input (REF+/REF–)						
V_{IH}	PECL input HIGH voltage	V_{DD} – 1.1		V_{DD} – 0.7	V	
V_{IL}	PECL input LOW voltage	V_{DD} – 2.0		V_{DD} – 1.5	V	
I_{IH}	PECL input HIGH current			200	µA	$V_{IN} = V_{IH(MAX)}$
I_{IL}	PECL input LOW current	–50			µA	$V_{IN} = V_{IL(MIN)}$
ΔV_{IN}	PECL input differential peak-to-peak voltage swing	400			mV	$V_{IH(MIN)} – V_{IL(MAX)}$
High-Speed Outputs						
ΔV_{OUT75}(1)	TX output differential peak-to-peak voltage swing	1200		2200	mVp-p	75 Ω to V_{DD} – 2.0 V (TX+) – (TX–)
ΔV_{OUT50}(1)	TX output differential peak-to-peak voltage swing	1000		2200	mVp-p	50 Ω to V_{DD} – 2.0 V (TX+) – (TX–)
High-Speed Inputs						
ΔV_{IN}(1)	PECL differential peak-to-peak input voltage swing	200		2600	mV	(Rx+) – (Rx–)
Miscellaneous						
V_{DD}	Power supply voltage	3.14		3.47	V	3.3V ±5%
P_D	Power dissipation		2.2	2.67	W	Max at 3.47V, outputs open, 136 MHz clock, at + 25°C
I_{DD}	Supply current (all supplies)			770	mA	
I_{DDA}	Supply current on V_{DDA}		100		mA	

1. *Refer to Application Note, AN-37, for differential measurement techniques.*

AC Characteristics

Over Recommended Operating Conditions.

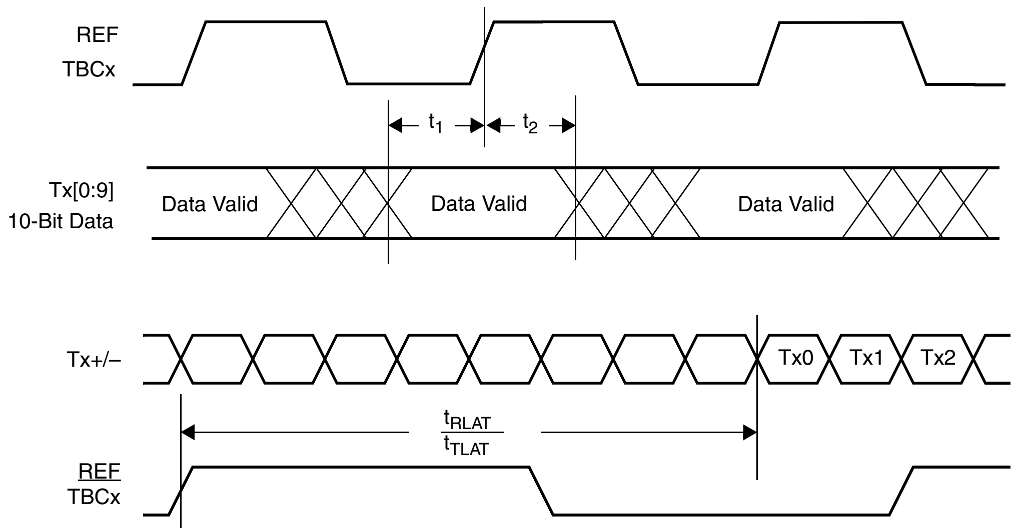


Figure 5. Transmitter Timing Waveforms

Table 4. Transmitter AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Condition
t_1	Tx[0:9] setup time to the rising edge of TBCx or REF	1.5			ns	Measured between the valid data level of Tx[0:9] to the 1.4V point of TBCx or REF.
t_2	Tx[0:9] hold time after the rising edge of TBCx or REF	1.0			ns	
t_{SDR},t_{SDF}	Tx+/Tx– rise and fall time			300	ps	20% to 80%, 75Ω load to V_{DD}/2, tested on a sample basis.
t_{RLAT}	Latency from rising edge of REF to Tx0 appearing on TX+/TX–	7bc + 0.66 ns		7bc + 1.46 ns		bc = bit clocks.
t_{TLAT}	Latency from rising edge of TBCx to Tx0 appearing on TX+/TX–	5bc + 0.66 ns		11bc + 1.46 ns	ns	bc = bit clocks.
Transmitter Output Jitter						
RJ	Random jitter (rms)		5	8	ps	Tested on a sample basis. 1 sigma deviation of 50% crossing point.
DJ	Serial data output deterministic jitter (peak-to-peak)		35	80	ps	IEEE 802.3Z Clause 38.68, tested on a sample basis.

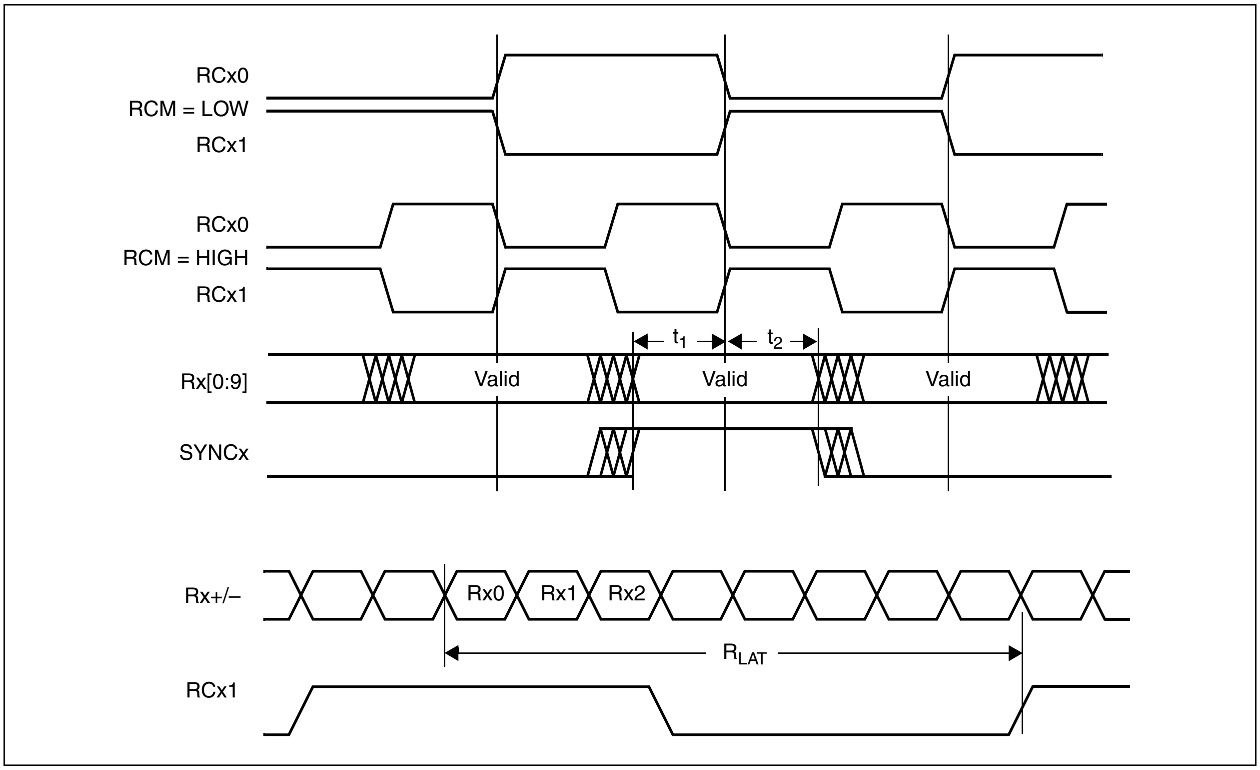


Figure 6. Receiver Timing Waveforms

Table 5. Receiver AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Condition
t_1	TTL outputs valid prior to RCx1/RCx0 rise	4.0 3.0 2.4			ns	At 1.0625Gbps At 1.25Gbps At 1.36Gbps
t_2	TTL outputs valid after RCx1 or RCx0 rise	3.0 2.0 1.8			ns	At 1.0625Gbps At 1.25Gbps At 1.36Gbps
t_3	Delay between rising edge of RCx1 to rising edge of RCx0	10 • T_{RX} –500		10 • T_{RX} +500	ps	T_{RX} is the bit period of the incoming data on Rx
t_4	Period of RCx1 and RCx0[(1)]	1.98 • T_{REF}		2.02 • T_{REF}	ps	Whether or not locked to serial data.
t_R, t_F	TTL output rise and fall time			2.4	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$, into 10pF load
R_{LAT}	Latency from serial bit Rx0 to rising edge RCx1	12bc + 2.77ns		13bc + 7.28ns		bc = bit clock
t_{LOCK}	Data acquisition lock time[(2)]			1400	bit times	8B/10B IDLE pattern Tested on a sample basis

1. *T_{REF} is either the incoming serial bit stream divided by 10, or the reference clock.*
2. *Probability of recovery for data acquisition is 95% per Section 5.3 of FC-PH, rev. 4.3.*

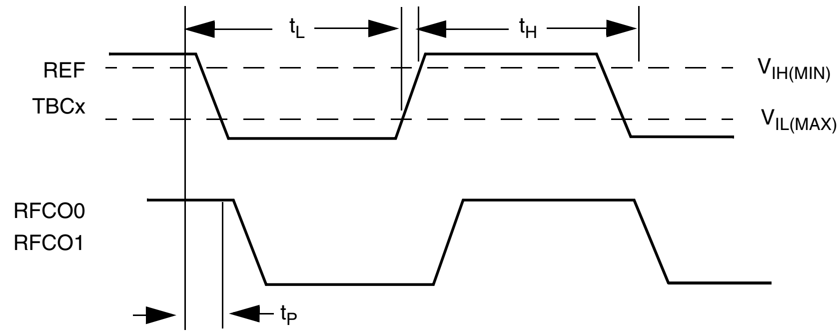
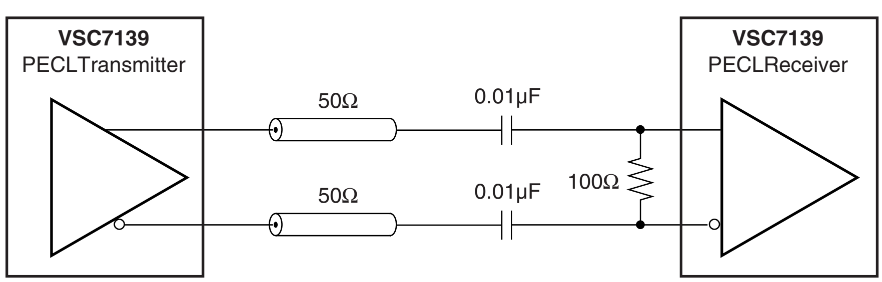


Figure 7. REF and TBCx Waveforms

Table 6. Reference Clock Requirements

Symbol	Parameter	Min	Typ	Max	Unit	Condition
$FR_{FULL\ RATE}$	Frequency range	105		136	MHz	Range over which both transmit and receive reference clocks on any link may be centered. RFCM = 1.
$FR_{HALF\ RATE}$	Frequency range	52.5		68	MHz	Range over which both transmit and receive reference clocks on any link may be centered. RFCM = 0.
FO	Frequency offset	–200		+200	ppm	Maximum frequency offset between transmit and receive reference clocks on one link.
t_P	Delay from REF to RFCO0/1	1.97		3.58	ns	
DC	RFC0/1 duty cycle	40		60	%	
t_R, t_F	RFC0/1 rise and fall time	0.25		1.5	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$.
DC	REF/TBCx duty cycle	35		65	%	Measured at 1.4V.
t_{RCR}, t_{RCF}	REF/TBCx rise and fall time			1.5	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$.



Additional pull-down resistors are not required for the VSC7139.

Figure 8. Typical PECL Interface Connection

Operating Conditions

Table 7. Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Power supply voltage	3.135	3.3	3.465	V
T	Operating temperature range[1]	0		+100	°C

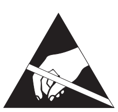
1. Lower limit of specification is ambient temperature and upper limit is case temperature.

Maximum Ratings

Table 8. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	Power supply voltage	–0.5	+4.0	V
	DC input voltage, PECL	–0.5	V_{DD} + 0.5	V
	DC input voltage, TTL	–0.5	+ 5.5	V
	DC output voltage, TTL	–0.5	V_{DD} + 0.5	V
	Output current, PECL and TTL	–50	+50	mA
T_S	Storage temperature	–65	+150	°C
V_{ESD}	ESD voltage (Human Body Model)		2900	V

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

Package Information

Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSST	VDD	VSST	SYNCB	RCB0	RB0	RB4	RB6	VDDT	VDD	VSST	RC1	VDDT	RC8	VSST	VDDT	VSST
B	RA7	RA8	RA9	VSST	RCB1	RB1	VDDT	RB7	VSS	SYNCC	RC0	RC2	RC5	RC9	SYNCD	RCD0	RCD1
C	RA4	RA5	RA6	VDDT	VDDT	RB2	VSST	RB8	SLPN	RCC0	VDDT	RC3	RC6	VDD	VDDT	VSST	RD0
D	RA0	RA1	VDDT	VSST	LPND	RB3	RB5	RB9	TMS	RCC1	VSST	RC4	RC7	RD1	RD2	RD3	RD4
E	RCA0	RCA1	RA2	RA3										VDDT	VSST	RD5	RD6
F	TBCB	SYNCA	VDDT	VSST										RD7	RD8	RD9	VSS
G	TB8	TB9	VSS	VDD										TC2	TC1	TC0	VDDT
H	TB4	TB5	TB6	TB7										TC6	TC5	TC4	TC3
J	TB0	TB1	TB2	TB3					NOT POPULATED					VDD	TC9	TC8	TC7
K	TBCA	TDO	VSS	LPNC										VSS	VSS	VDD	TBCC
L	TA8	TA9	VSS	VDD										TD3	TD2	TD1	TD0
M	TA4	TA5	TA6	TA7										TD7	TD6	TD5	TD4
N	TA0	TA1	TA2	TA3										PLUP	VDD	TD9	TD8
P	LTCN	RFCM	REF-	LPNB	TA-	VSS	TB-	VSS	CAP0	VSS	TC+	VSS	TD+	RFCO1	TDI	RFCO0	TBCD
R	REFT	REF+	LPNA	VDD	TA+	VSS	TB+	VSSA	CAP1	VSS	TC-	VSS	TD-	VDD	TRSTN	VDDTR	ENCDET
T	RCM	VSS	VDD	VDD	VDDPA	VSS	VDDPB	VSS	VDDA	VSS	VDDPC	VSS	VDDPD	VDD	VSS	VSSTR	TCK
U	VSS	VSS	RA-	RA+	VDD	RB-	RB+	VSS	VSS	RC-	RC+	VSS	RD-	RD+	VSS	VSS	VSS

Figure 9. Pin Diagram for 208-Pin TBGA (TW)

Pin Identifications

Table 9. Pin Identifications for 208-Pin TBGA (TW)

Pin	Name	I/O	Level	Description
N1, N2, N3 N4, M1, M2 M3, M4, L1 L2	TA0, TA1, TA2 TA3, TA4, TA5 TA6, TA7, TA8 TA9	I	TTL	10-Bit Transmit bus for Channel A. Parallel data on this bus is latched on the rising edge of REF, TBCC or TBCA. TA0 is transmitted first.
J1, J2, J3 J4, H1, H2 H3, H4, G1 G2	TB0, TB1, TB2 TB3, TB4, TB5 TB6, TB7, TB8 TB9	I	TTL	10-Bit Transmit bus for Channel B. Parallel data on this bus is latched on the rising edge of REF, TBCC or TBCB. TB0 is transmitted first.
G16, G15, G14 H17, H16, H15 H14, J17, J16 J15	TC0, TC1, TC2 TC3, TC4, TC5 TC6, TC7, TC8, TC9	I	TTL	10-Bit Transmit Bus for Channel C. Parallel data on this bus is latched on the rising edge of REF or TBCC. TC0 is transmitted first.
L17, L16, L15 L14, M17, M16 M15, M14, N17 N16	TD0, TD1, TD2 TD3, TD4, TD5 TD6, TD7, TD8 TD9	I	TTL	10-Bit Transmit Bus for Channel D. Parallel data on this bus is latched on the rising edge of REF, TBCC or TBCD. TD0 is transmitted first.
R2 P3	REF+ REF–	I	PECL or TTL	Differential. This rising edge of REF+/– provides the reference clock at 1/10th or 1/20th of the baud rate (depending on RFCM) to the clock multiplying PLL. If REF+/– is used, either leave REFT open or set REFT HIGH. Internally biased to V_{DD}/2. If all TBCx inputs are HIGH, the rising edge of REF will latch Tx[0:9] on all four channels.
R1	REFT	I	TTL	TTL Reference Clock. This rising edge of REFT provides the reference clock at 1/10th or 1/20th of the baud rate (depending on RFCM) to the clock multiplying PLL. If REFT is used, set REF+ HIGH and leave REF– open. If all TBCx inputs are HIGH, the rising edge of REFT will latch Tx[0:9] on all four channels.
P2	RFCM	I	TTL	Reference Clock Mode Select. When LOW, REF is at 1/20th of the transmit baud rate (such as 62.5 MHz for 1.25 Gbps). When HIGH, REF is at 1/10th the baud rate (such as 125 MHz for 1.25 Gbps).
P16 P14	RFCO0 RFCO1	O	TTL	These are identical copies of the transmit baud rate clock divided by 10.
K1, F1 K17, P17	TBCA, TBCB TBCC, TBCD	I	TTL	Per Channel Transmit Byte Clock for Channel x. All four channels' parallel Tx[0:9] inputs can be timed to REF, TBCC, or independently to TBCx. Refer to "Serializer" on page 4.
P1	LTCN	I	TTL	Latch Transmit Byte Clocks. When LOW, internal PLLs align clocks with each of the transmit byte clocks, if present. Data may be corrupted when LOW. When HIGH, alignment will remain static, regardless of actual TBCx location.
R5, P5 R7, P7 P11, R11 P13, R13	TA+, TA– TB+, TB– TC+, TC– TD+, TD–	O	PECL	Differential. AC-coupling recommended. These pins output the serialized transmit data for Channel x when PLUP = LOW. When PLUP is HIGH, Tx+ is HIGH and Tx– = LOW.
D1, D2, E3 E4, C1, C2 C3, B1, B2 B3	RA0, RA1, RA2 RA3, RA4, RA5 RA6, RA7, RA8 RA9	O	TTL	10-Bit Receive bus for Channel A. Parallel data on this bus is synchronous to RCA0 and RCA1. RA0 is the first bit received.

Table 9. Pin Identifications for 208-Pin TBGA (TW) *(continued)*

Pin	Name	I/O	Level	Description
A6, B6, C6 D6, A7, D7 A8, B8, C8 D8	RB0, RB1, RB2 RB3, RB4, RB5 RB6, RB7, RB8 RB9	O	TTL	10-Bit Receive bus for Channel B. Parallel data on this bus is synchronous to RCB0 and RCB1. RB0 is the first bit received.
B11, A12, B12 C12, D12, B13 C13, D13, A14 B14	RC0, RC1, RC2 RC3, RC4, RC5 RC6, RC7, RC8 RC9	O	TTL	10-Bt Receive bus for Channel C. Parallel data on this bus is synchronous to RCC0 and RCC1. RC0 is the first bit received.
C17, D14, D15 D16, D17, E16 E17, F14, F15, F16	RD0, RD1, RD2 RD3, RD4, RD5 RD6, RD7, RD8 RD9	O	TTL	10-Bit Receive bus for Channel D. Parallel data on this bus is synchronous to RCD0 and RCD1. RD0 is the first bit received.
T1	RCM	I	TTL	Recovered Clock Mode Control. When LOW, RCx0/RCx1 is $1/20^{th}$ of the incoming baud rate. When HIGH, RCx0/RCx1 is $1/10^{th}$ the incoming baud rate.
E1 E2	RCA0 RCA1	O	TTL	Recovered complementary clocks for Channel A at $1/10^{th}$ the incoming baud rate (RCM = HIGH) or $1/20^{th}$ (RCM = LOW). Synchronous to the RA[0:9] and SYNCA bus.
A5 B5	RCB0 RCB1	O	TTL	Recovered complementary clocks for Channel B at $1/10^{th}$ the incoming baud rate (RCM = HIGH) or $1/20^{th}$ (RCM = LOW). Synchronous to the RB[0:9] and SYNCB bus.
C10 D10	RCC0 RCC1	O	TTL	Recovered complementary clocks for Channel C at $1/10^{th}$ the incoming baud rate (RCM = HIGH) or $1/20^{th}$ (RCM = LOW). Synchronous to the RC[0:9] and SYNCC bus.
B16 B17	RCD0 RCD1	O	TTL	Recovered complementary clocks for Channel D at $1/10^{th}$ the incoming baud rate (RCM = HIGH) or $1/20^{th}$ (RCM = LOW). Synchronous to the RD[0:9] and SYNCD bus.
U4, U3 U7, U6 U11, U10 U14, U13	RA+, RA– RB+, RB– RC+, RC– RD+, RD–	I	PECL	Differential. These are the serial receive data inputs for Channel x that are selected when PLUP = LOW. AC-coupling recommended. (Internally biased to $V_{DD}/2$.)
N14	PLUP	I	TTL	Parallel Loopback Enable Input. Rx is input to the CRU for Channel x (normal operation) when PLUP = LOW. When HIGH, internal loopback paths from Tx to Rx are enabled. See Table 2 and “Loopback Operation” on page 7.
C9	SLPN	I	TTL	Serial Loopback Enable Input. Normal operation when HIGH. When LOW, Rx+/– is looped back to Tx+/– internally for diagnostic purposes. See Table 2 and “Loopback Operation” on page 7.
R3 P4 K4 D5	LPNA LPNB LPNC LPND	I	TTL	Loopback Enable Pins. When LPNx = LOW, PLUP/SLPN impact Channel x. When HIGH, PLUP/SLPN have no effect on Channel x.
R17	ENCDET	I	TTL	Enables SYNCx and word alignment when HIGH. When LOW, keeps current word alignment and disables SYNCx (always LOW).
F2 A4 B10 B15	SYNCA SYNCB SYNCC SYNCD	O	TTL	Comma Detect for Channel x. This output goes HIGH for half of an RCx1 period to indicate that Rx[0:9] contains a comma character (0011111XXX). SYNCx will go HIGH only during a cycle when RCX0 is rising. SYNCx is enabled when ENCDET is HIGH.

Table 9. Pin Identifications for 208-Pin TBGA (TW) *(continued)*

Pin	Name	I/O	Level	Description
P9 R9	CAP0 CAP1		Analog	Loop Filter capacitor for the CMU. Typically 0.1µF, connected between CAP0 and CAP1. Amplitude is less than 3.3V.
T17	TCK	I	TTL	JTAG Test Clock.
D9	TMS	I	TTL	JTAG Test Mode Select.
R15	TRSTN	I	TTL	JTAG Test Reset, Active LOW.
P15	TDI	I	TTL	JTAG Test Data Input.
K2	TDO	O	TTL	JTAG Test Data Output.
T9	VDDA		Pwr	Analog Power Supply.
R8	VSSA		Pwr	Analog Ground. Tie to common ground plane with V_{SS}.
A2, A10, C14, G4, J14, K16, L4, N15, R4, R14, T3, T4, T14, U5	VDD		Pwr	Digital Logic Power Supply.
C4, D3, F3, A9, B7, C5, A13, A16, C11, C15, E14, G17	VDDT		Pwr	TTL Output Power Supply.
T5 T7 T11 T13	VDDPA VDDPB VDDPC VDDPD		Pwr	PECL I/O Power Supply for Channel x.
R16	VDDTR		Pwr	TTL Output Power Supply for RFCO0 and RFCO1.
T16	VSSTR		Pwr	TTL Ground for RFCO0 and RFCO1.
A1, A3, A11, A15, A17, B4, C7, C16, D4, D11, E15, F4	VSST		Pwr	Ground for TTL Outputs.
B9, F17, G3, K3, K14, K15, L3, P6, P8, P10, P12, R6, R10, R12, T2, T6, T8, T10, T12, T15, U1, U2, U8, U9, U12, U15, U16, U17	VSS		Pwr	Ground.

Package Drawing

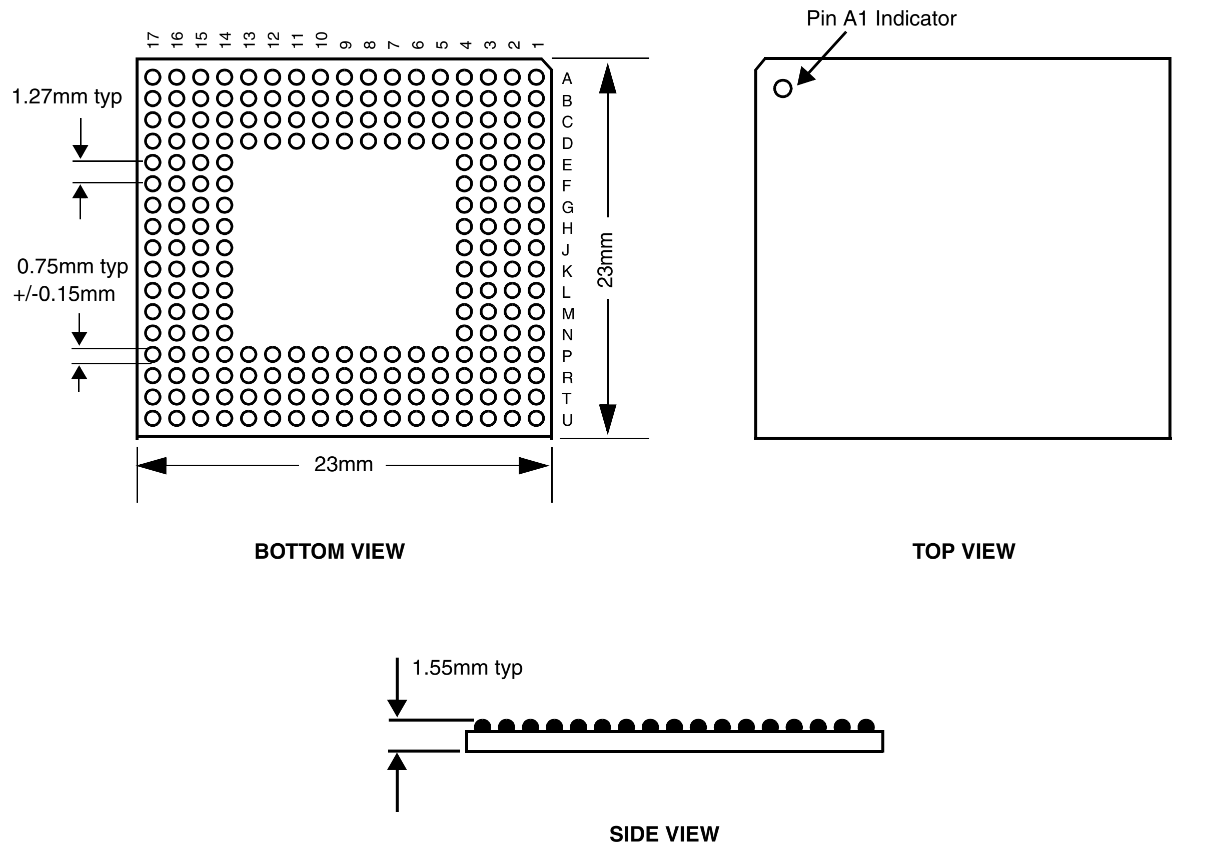


Figure 10. Package Drawing for 208-Pin TBGA (TW)

Moisture Sensitivity Level

This device is rated moisture sensitivity level 3 or better as specified in JEDEC standard IPC/JEDEC J-STD-020B. For more information, see the JEDEC standard.

ORDERING INFORMATION

VSC7139 Quad Transceiver for Gigabit Ethernet and Fibre Channel

Part Number	Description
VSC7139TW	208-Pin TBGA, 23mm x 1.55mm x 23mm Body

PRINTED IN THE U.S.A