Signetics

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Status	Product Specification
FAST Products	

FAST 74F676
Shift Register

16-Bit Serial/Parallel-In, Serial-Out Shift Register (3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F676	110MHz	48mA

FEATURES

- **16-bit parallel-to-serial conversion**
- **16-bit serial-in, serial-out**
- **Chip select control**
- **Power supply current 48mA typical**
- **Shift frequency 110 MHz typical**
- **Available in 300mil-wide 24-pin Slim DIP package**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F676N
24-Pin Plastic SOL	N74F676D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_{15}	Parallel data inputs	1.0/1.0	20µA/0.6mA
SI	Serial data input	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20µA/0.6mA
M	Mode select input	1.0/1.0	20µA/0.6mA
SO	Serial data output	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the mode (M) input is High, information present on the parallel data (D_0 - D_{15}) inputs is entered on the falling edge of the clock pulse ($\overline{CP}$) input signal. When M is Low, data is shifted out of the most significant bit position while information present on the serial (SI) input shifts into the least significant bit position. A High signal on the chip select ($\overline{CS}$) input prevents both parallel and serial operations. The 16 bit shift register operates in one of three modes, as indicated in the shift register Function Table.

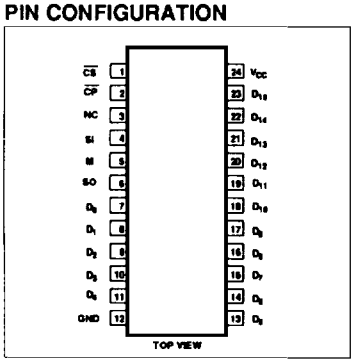
Hold : a High signal on the Chip Select ($\overline{CS}$) input prevents clocking, and data is stored in the 16 registers.

Shift/Serial load : data present on the SI pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks finally appearing on the SO pin.

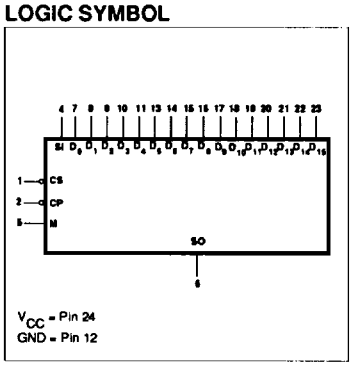
Parallel load : data present on D_0 - D_{15} are entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q_{15} register output.

To prevent false clocking, $\overline{CP}$ must be Low during a Low-to-High transition of $\overline{CS}$.

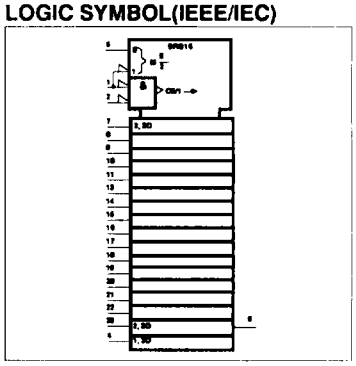
PIN CONFIGURATION



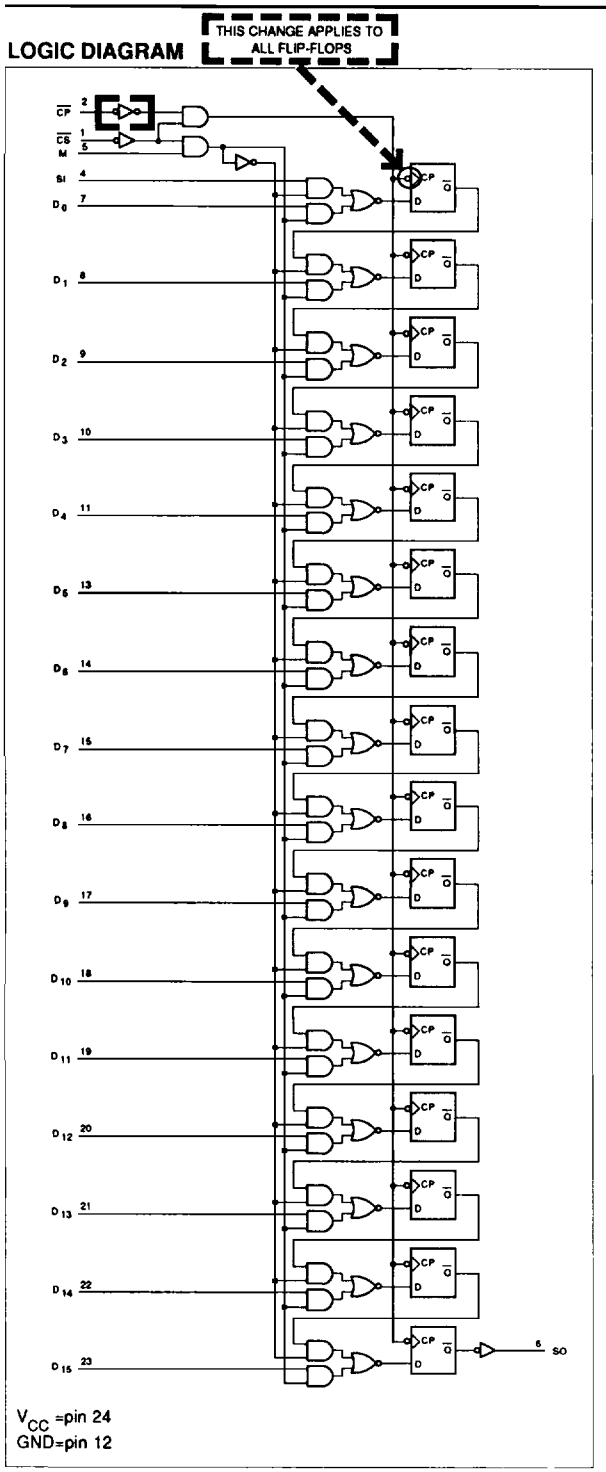
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

CONTROL INPUTS			OPERATING MODE
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	↓	Shift/Serial load
L	H	↓	Parallel load

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low transition of clock input

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