

74LS1801 Bit Stream Manager

Encoder/Decoder
Product Specification

Logic Products

DESCRIPTION

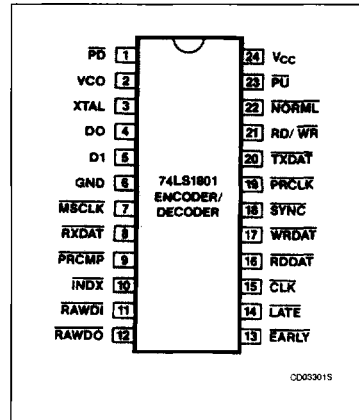
The 74LS1801 Encoder/Decoder (Figure 1) supports disk drive and data communications devices that require fast and reliable data separation capabilities. Although ideally suited for use with the 74LS1802 Serializer/Deserializer, the 74LS1801 is a flexible device which can be implemented in a variety of design applications.

Encoding is possible in FM, MFM, or Differential Manchester formats, making the 74LS1801 invaluable in designs requiring single density disk recording, double density disk recording, or in data communications applications. Included on-chip is a phase-comparator which can be bypassed; this feature is particularly useful in applications that use a complete external phase lock loop.

FEATURES

- Data rates up to 10MHz
- FM, MFM, and Differential Manchester encoding/decoding
- Precompensation in MFM write mode
- Built-in phase comparator
- Single 5V power supply
- Selectable encoding violation generation/detection formats

PIN CONFIGURATION



BLOCK DIAGRAM

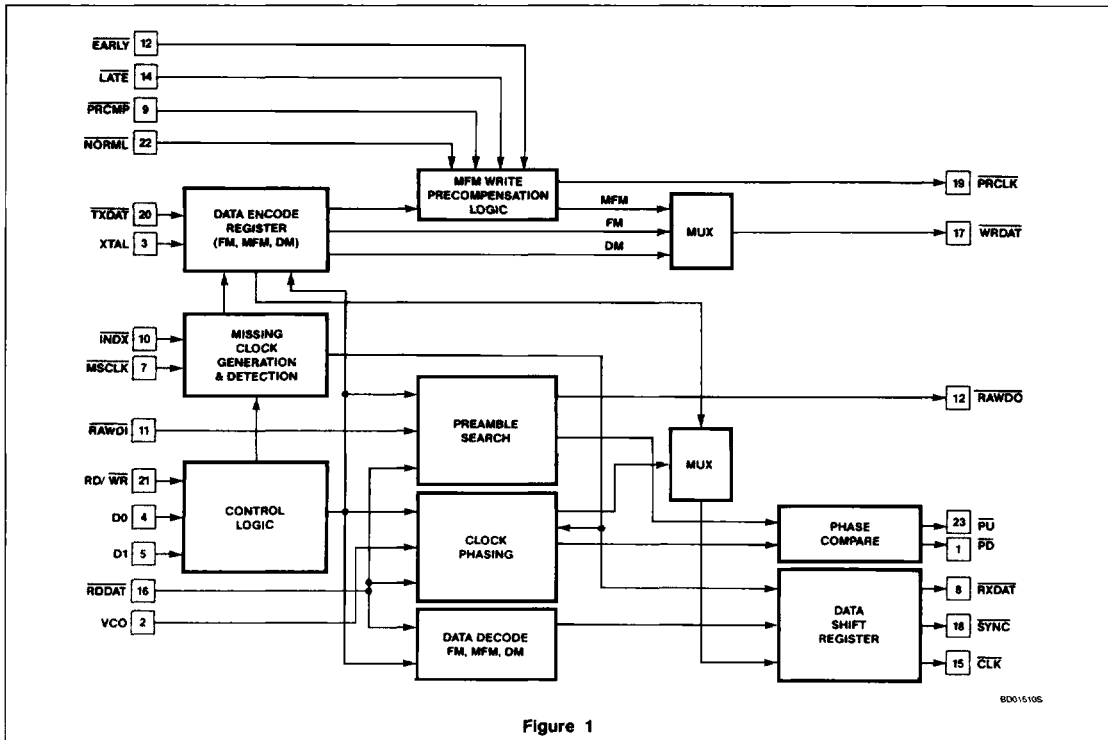


Figure 1

Bit Stream Manager

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PIN CONFIGURATION

			PIN NO.	IDENTIFIER	DESCRIPTION
			10	$\overline{\text{INDX}}$	INDeX – an input that designates the missing clock pattern to be generated during the write mode; in the read mode, determines which data/clock pattern must be recognized as an address mark (Table 2, 3).
			11	$\overline{\text{RAWDI}}$	RAW Data In – a shaped data pulse derived from $\overline{\text{RAWDO}}$. $\overline{\text{RAWDO}}$ is normally tied directly to $\overline{\text{RAWDI}}$.
			12	$\overline{\text{RAWDO}}$	RAW Data Out – a shaped data pulse derived from $\overline{\text{RDDAT}}$ that can be processed through an external phase lock loop. $\overline{\text{RAWDO}}$ is normally tied directly to $\overline{\text{RAWDI}}$.
			13	$\overline{\text{EARLY}}$	Modifies clock rate with respect to crystal reference when early precompensation is desired.
			14	$\overline{\text{LATE}}$	Modifies clock rate with respect to crystal reference when late pre-compensation is desired.
			15	$\overline{\text{CLK}}$	CLoCK – Clock input equal to the frequency of NRZ data.
			16	$\overline{\text{RDDAT}}$	ReaD DATa – an input of encoded serial data (MFM, FM, or Differential Manchester) that is to be converted to NRZ data.
			17	$\overline{\text{WRDAT}}$	WRite DATa – an output of encoded serial data (FM, MFM, or Differential Manchester) derived from NRZ data.
			18	$\overline{\text{SYNC}}$	SYNChronization output – when active low, indicates recognition of valid encoding violation in the $\overline{\text{RDDAT}}$.
			19	$\overline{\text{PRCLK}}$	PReCompensation CLoCK – an output used to excite an external delay line.
			20	$\overline{\text{TXDAT}}$	Transmit Data – an input of NRZ data that is to be encoded to FM, MFM, or Differential Manchester data.
			21	$\overline{\text{RD/WR}}$	ReaD/WRite – an input designating mode of operation: when high, a read is indicated; when low, a write is indicated.
			22	$\overline{\text{NORML}}$	$\overline{\text{NORMaL}}$ – a clock input that is used when no precompensation is desired.
			23	$\overline{\text{PU}}$	Pump Up – an output from the phase comparator that indicates the frequency of an external VCO is too low as compared to $\overline{\text{RDDAT}}$.
			24	V_{CC}	Supply voltage.
PIN NO.	IDENTIFIER	DESCRIPTION			
1	$\overline{\text{PD}}$	Pump Down – an output from the phase comparator that indicates the frequency of an external VCO is too high as compared to $\overline{\text{RDDAT}}$.			
2	VCO	Voltage Controlled Oscillator – an input used as a phase reference for the encoded read data ($\overline{\text{RDDAT}}$).			
3	XTAL	An input used to synchronize the 74LS1801 during write mode; the crystal frequency is twice the serial data rate.			
4	D0	Mode Select – inputs designating the format (FM, MFM, Differential Manchester) of serial I/O data that is to be encoded or decoded.			
5	D1				
6	GND	Ground.			
7	$\overline{\text{MSCLK}}$	MISSing CLoCK – missing clock bits are generated/detected in the data stream, depending upon the state of this input (Table 2, 3).			
8	$\overline{\text{RXDAT}}$	ReceiVe DATa – an output consisting of NRZ data decoded from MFM, FM, or Differential Manchester data.			
9	$\overline{\text{PRCMP}}$	PReCoMP – an input that allows precompensation of MFM encoded data.			

ORDERING CODE

PACKAGES	COMMERCIAL RANGES
	$\text{V}_{\text{CC}} = 5\text{V} \pm 10\%$; $\text{T}_{\text{A}} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$
Hermetic DIP	N74LS1801I
Plastic DIP	N74LS1801N

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FUNCTIONAL OPERATION

The 74LS1801 Encoder/Decoder serves to translate data between disk drive or data communications devices and the 74LS1802 Serializer/Deserialzer (or comparable device). Information entering or leaving the Serializer/Deserialzer interface is in the form of standard NRZ data and can be encoded to (or decoded from) one of three popular formats:

- Frequency Modulation (FM) — single density disk recordings.
- Modified Frequency Modulation (MFM) — double density disk recordings.
- Differential Manchester — data communications applications.

Read/Write and Format Control

The operational mode of the 74LS1801 is dictated by the RD/WR input: when low, a write (encode) is indicated; when high, a read (decode) is designated. In either mode, the format of data being decoded or encoded is controlled by the states of D0 and D1 inputs as shown below:

Table 1. Format Control

D0	D1	RESULTING FORMAT
L	L	MFM
H	L	FM
L	H	Differential Manchester

Following are discussions of the encoding and decoding functions of the 74LS1801, and the timing requirements necessary for accurate data transmittal.

Encoding Logic

When in the encode mode, NRZ data is input via the TXDAT input and, after about a three bit delay, is output on WRDAT. As described, output format is dependent on the states of D0 and D1. Address marks are distinguished from data by deleting clock pulses within the character.

These "missing clocks" are generated within the byte following a preamble of either all 0's (MFM and FM format) or all 1's (Differential Manchester format). As described in Table 2, clocks are eliminated according to inputs INDX, MSCLK, and the specified encoding format.

When encoding data in the MFM format, MSCLK may be enabled during preamble generation and up to the beginning of an address mark. MSCLK can then be disabled during the byte following an address mark, or before the final bit of a four bit series in which the first two bits are 0's (e.g., before the final 0 in 0010). In applications utilizing consecutive A1 characters (such as in the case of floppy disk soft-sectored formats), MSCLK

Table 2. Missing Clocks

MSCLK	INDX	FORMAT	RESULTING CLOCK PATTERN							
			Bit Cell Numbers:							
			0	1	2	3	4	5	6	7
L	H	FM			V	V	V			
L	L	FM				V	V			
L	H	Differential Manchester	V	V		V	V			
L	L	Differential Manchester	V	V			V			
L	X	MFM	2nd of 3 clocks missing							

NOTES:

- X = Don't care
- V = Missing Clock

Table 3. Address Mark Identification Requirements in Decode Mode

MSCLK	INDX	CONDITIONS FOR ACTIVE SYNC OUTPUT
H	X	First "1" bit after preamble
L	H	A1 ₁₆ with missing clocks
L	L	Any byte with missing clocks

would remain active until the beginning of the byte following the A1 series.

The 74LS1801 also provides pre-compensation capabilities when encoding data in the MFM format. Activating the PRCOMP signal (low) synchronizes output data according to a clock input provided on one of three inputs: EARLY — a clock shifted early in time, LATE — a clock shifted late in time, or NORML — a clock provided when no precompensation is needed. These inputs are supplied by an external delay line which, in turn, is excited by the PRCLK output (see Typical System Configuration, Figure 2.)

When encoding in FM or Differential Manchester formats, missing clocks are only generated in the first byte following a preamble of zeroes. The most significant bit of this byte must be a "1"; for example, address marks F8, FB, FC, or FE. MSCLK may be enabled up to the beginning of an address mark; once an address mark has been transmitted, it is not necessary to disable MSCLK.

Decoding Logic

In the decode mode, data (MFM, FM, or Differential Manchester) is input via the RDDAT input and, after an eleven bit delay, is output as NRZ data on RXDAT. As described above, input format is defined by the states of D0 and D1. In the MFM format, a minimum preamble length of 34 bits is required to allow for phase synchronization and location of an address mark; when in FM or Differential Manchester mode, a minimum length of 18 bits is required. After a preamble has been recognized, the 74LS1801 searches for an address mark. When an address mark is identified, the SYNC output becomes active low, and alerts the 74LS1802 of incoming data. Rules for positive address mark identi-

fication are described below and summarized in Table 3.

When MSCLK is inactive, SYNC is activated on the first "1" data bit following a preamble of zeroes (MFM and FM) or 1's (Differential Manchester). Data is contained in the byte following this bit.

If MSCLK is active, the byte following a preamble of all zeroes is checked for the required missing clocks (Table 3) and if detected, SYNC is activated.

PHASE LOCK LOOP AND DATA SEPARATION LOGIC

Data/clock separation logic requires a clock pulse that is synchronous with read data (RDDAT); to create this signal, the 74LS1801 employs a Phase Lock Loop. In its simplest form, the PLL consists of an internal phase comparator, an external low pass filter and an external voltage controlled oscillator (VCO). Output from the VCO is continuously fed back to the phase compare circuit and contrasted with data read from the disk or communications device (RDDAT). A difference in phase is represented as one of two quantized output pulses: Pump Up indicates VCO frequency is too low, whereas Pump Down indicates that the VCO frequency is too high. The resulting output (PU or PD) is then processed by a low-pass filter which outputs a DC voltage proportional to the phase deviation. Accordingly, the VCO frequency is precisely serviced to the rate at which data was recorded. The 74LS1801 provides the capability to bypass internal phase compare logic; a typical application of this feature would be in designs implementing a complete external PLL.

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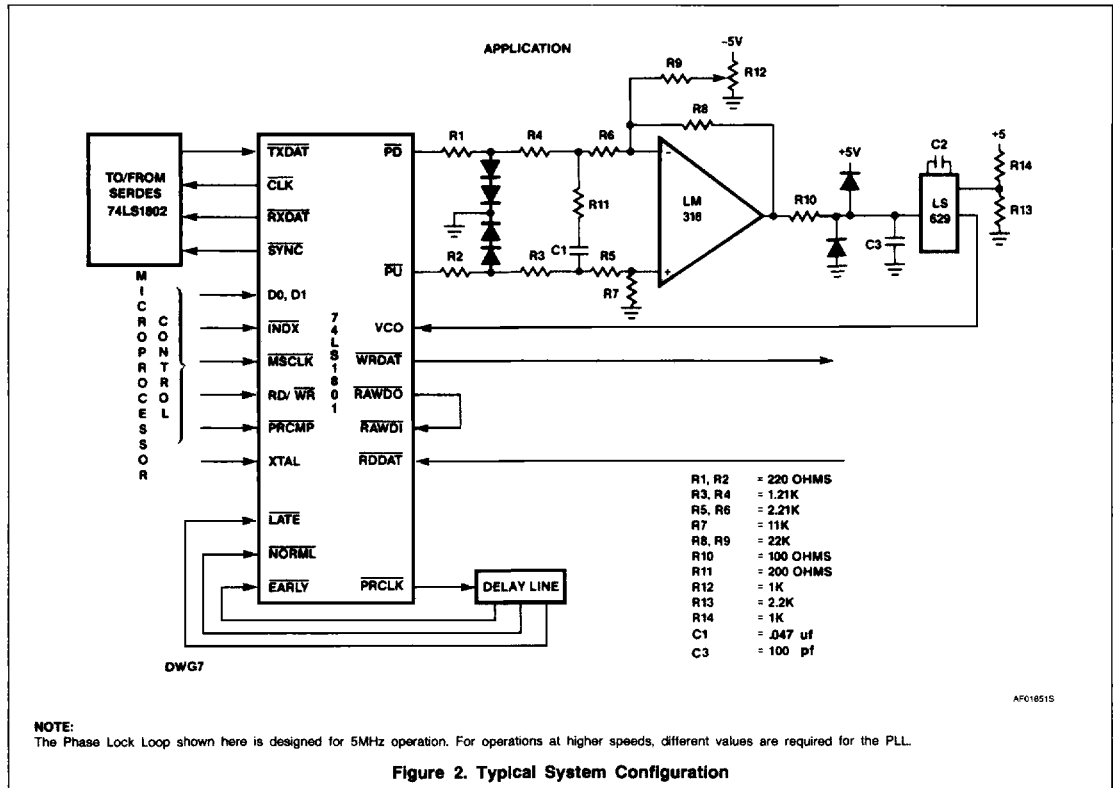


Figure 2. Typical System Configuration

Figure 3 illustrates this application and is discussed below.

RAW Data Out is a shaped data pulse derived directly from RDDAT. In MFM and FM modes, output is generated from the falling edge of RDDAT: in Differential Manchester mode, output is generated from both rising and falling edges. RAW Data In is a shaped data pulse derived from RAWDO and is used in internal data separation logic. The falling edge of RAWDI must be in phase with the falling edge of the VCO. RAWDI is normally tied directly to RAWDO.

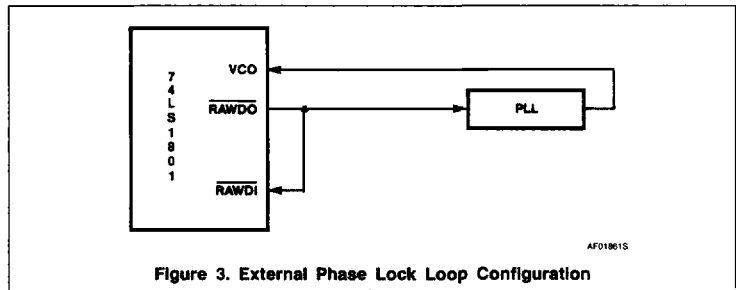
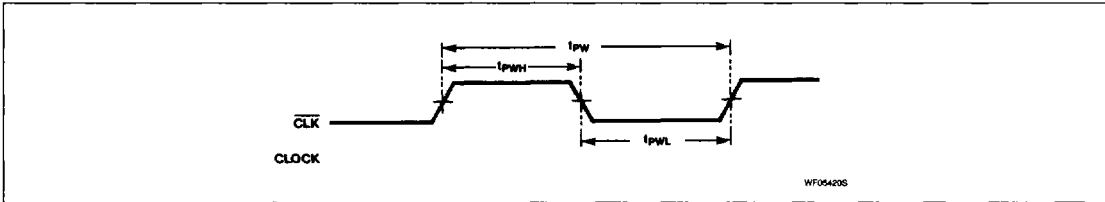


Figure 3. External Phase Lock Loop Configuration

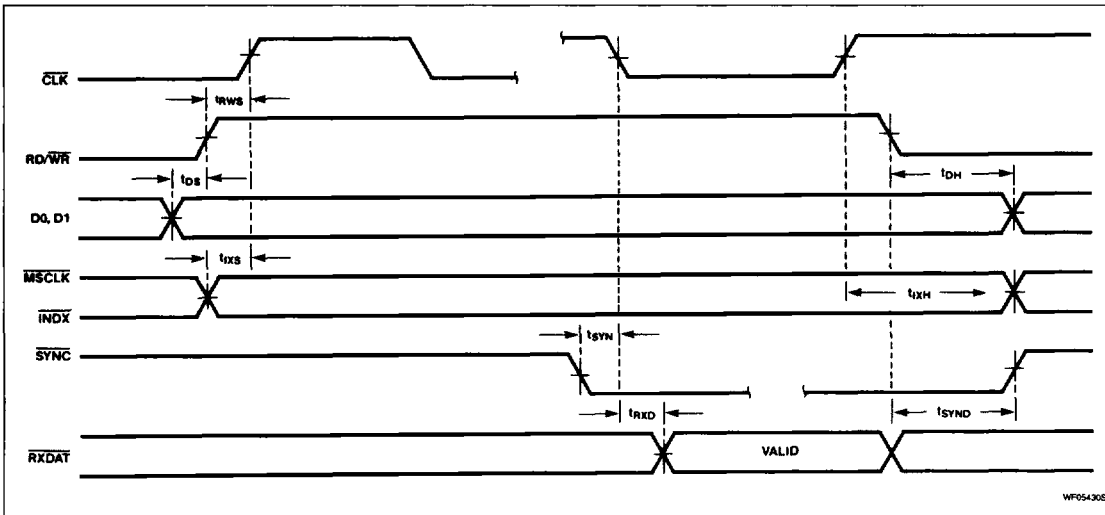
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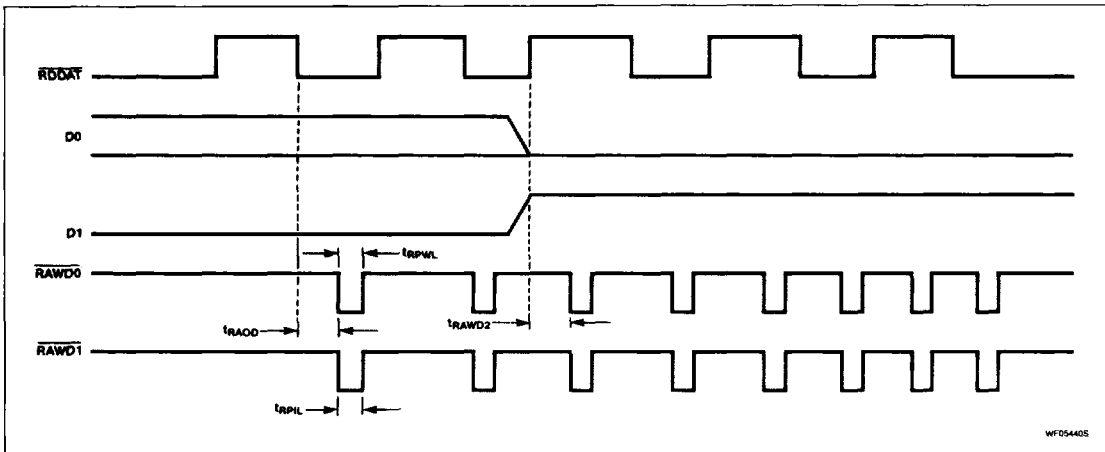
CLOCK CYCLE



READ CYCLE



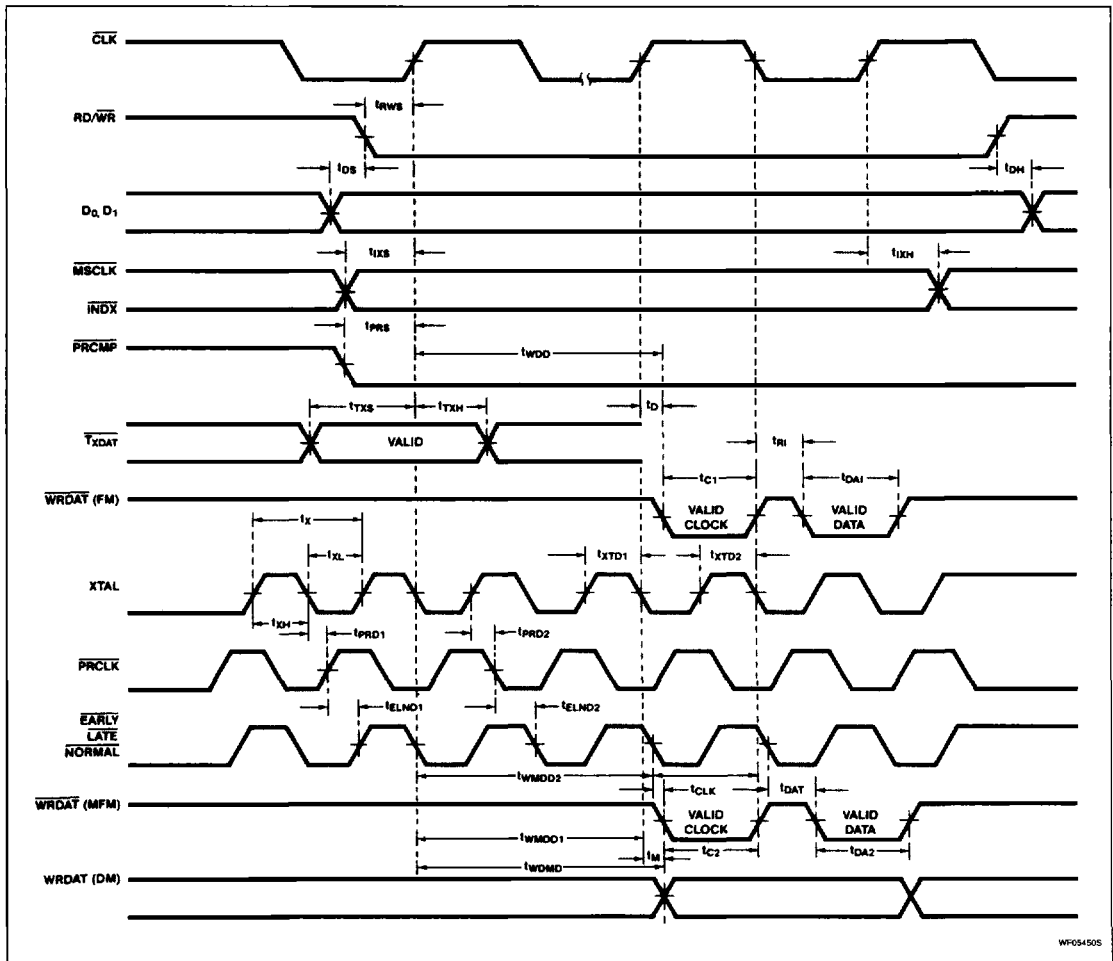
OTHER TIMING



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WRITE CYCLE TIMING



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ABSOLUTE MAXIMUM RATINGS

PIN	DESCRIPTION	RATING	UNIT
V _{CC}	Supply voltage	+7.0	V
All other pins	Logic input pins	5.5	V

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V±5%; TA = 0°C to +70°C

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	COMMENTS
		Min	Typ	Max		
V _{TH}	Input threshold voltage	0.8		2.0	V	
V _{CD}	Input clamp diode voltage	I _N = -18mA		-1.2	V	
I _{IL}	Input low current	V _{IN} = 0.4V		-20	μA	
I _{IH}	Input high current	V _{IN} = 2.7V		20	μA	
I _I	Max input high current	V _{IN} = 5.5V		100	μA	
V _{OL}	Output voltage low	I _{OL} = 8mA		0.5	V	Pins 8, 12, 15, 17, 18, 19 Pins 1, 23
		I _{OL} = 20mA		0.5	V	
V _{OH}	Output voltage high	V _{CC} = 4.5V	2.5		V	Pins 8, 12, 15, 17, 18, 19 Pins 1, 23
		I _{OH} = 400μA I _{OH} = 1mA	2.5		V	
I _{OS}	Output short circuit current	V _{OUT} = 0	-15	-100	mA	Pins 8, 12, 15, 17, 18, 19 Pins 1, 23
		V _{OUT} = 1	-15	-100	mA	
I _{CC}	Supply current			184	mA	

AC ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION	LIMITS (in ns)		
		Min	Typ	Max
t _{PW}	CLK pulse width	100		
t _{PWL}	CLK low time	50		
t _{PWH}	CLK high time	50		
t _X	XTAL cycle time	50		
t _{XH}	XTAL high time	25		
t _{XL}	XTAL low time	25		
t _{RWS}	RD/ \overline{WR} set-up to \uparrow CLK	0		
t _{DS}	D0, D1 set-up to RD/ \overline{WR}	0		
t _{IXS}	\overline{MSCLK} , \overline{INDX} set-up to \uparrow CLK		35.2	
t _{SYN}	\downarrow SYNC to \downarrow CLK	2		
t _{RXD}	\downarrow CLK to \overline{RXDAT} valid			4
t _{DH}	RD/ \overline{WR} to D0, D1 hold	0		
t _{SYND}	RD/ \overline{WR} to \overline{SYNC} inactive delay			36.4
t _{RAOD}	\downarrow RDDAT to \downarrow RAWDO delay		29.2	
t _{RPIL}	RAWDI pulse width	20*		
t _{RPWL}	RAWDO pulse width			40*
t _{WDMD}	\overline{TXDAT} to \overline{WRDAT} (DM)			t _{PW} + 41.2
t _M	\uparrow CLK to \overline{WRDAT} delay		41.2	
t _{RAWD2}	\uparrow RDDAT to \downarrow RAWDO delay		32.2	

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AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	DESCRIPTION	LIMITS (in ns)		
		Min	Typ	Max
t _{DA2}	DATA bit duration		23.0	
t _{iXH}	↑CLK to $\overline{\text{MSCLK}}$, $\overline{\text{INDX}}$ hold		14.8	
t _{PRS}	$\overline{\text{PRCMP}}$ set-up to ↑CLK			0
t _{TXS}	$\overline{\text{TXDAT}}$ set-up to ↑CLK		85.2	
t _{TXH}	$\overline{\text{TXDAT}}$ hold time		14.8	
t _{WDD}	$\overline{\text{TXDAT}}$ to $\overline{\text{WRDAT}}$ clock delay (FM data)		tpw + 36.3	
t _D	↑CLK to clock delay (FM data)		36.3	
t _{C1}	Clock bit duration (FM)		19.0	
t _{R1}	Clock & data bit separation		31.0	
t _{DA1}	Data bit duration (FM)		19.0	
t _{XTD1}	↑XTAL to ↑CLK delay		35.2	
t _{XTD2}	↑XTAL to ↓CLK delay		32.2	
t _{PRD1}	↓XTAL to ↑PRCLK delay		26.3	
t _{PRD2}	↑XTAL to ↓PRCLK delay		28.3	
t _{ELND1}	↑PRCLK to $\overline{\text{Early}}$, $\overline{\text{Late}}$, $\overline{\text{Normal}}$ rising edge	1/2 tpw		1/4 tpw
t _{ELND2}	↓PRCLK to $\overline{\text{Early}}$, $\overline{\text{Late}}$, $\overline{\text{Normal}}$ falling edge	1/4 tpw		0
t _{WMDD2}	$\overline{\text{TXDAT}}$ to $\overline{\text{WRDAT}}$ data delay (MFM)			3.5 x tpw
t _{WMDD1}	$\overline{\text{TXDAT}}$ to $\overline{\text{WRDAT}}$ clock delay (MFM)			3.0 x tpw
t _{CLK}	$\overline{\text{Early}}$, $\overline{\text{Late}}$, $\overline{\text{Normal}}$ falling edge to clock bit delay (MFM)		12.1	
t _{C2}	Clock bit duration (MFM)		23.0	
t _{DAT}	$\overline{\text{Early}}$, $\overline{\text{Late}}$, $\overline{\text{Normal}}$ falling edge to data bit delay (MFM)		12.1	

*Tabular entries with an asterisk are parameters that are guaranteed at the values listed; these values were determined either by system bench testing or by Signetics' characterization procedures. All other tabular entries are taken directly from simulation results run at range of operational frequencies; these values are not tested or guaranteed.