Signetics

FAST 74F784
Multiplier

8-Bit Serial/Parallel Multiplier (With Adder/Subtracter)
Preliminary Specification

FAST Products

FEATURES

- **Serial (n × 8)-bit multiplication**
- **Final stage adder/subtracter for optional use in adding a B bit to obtain S± B.**
- **Two's Complement multiplication**
- **Cascadable for any number of bits**
- **Full Adder and B – 1 input included for maximum flexibility**
- **Maximum clock frequency 50MHz guaranteed**
- **Supply current 100mA max**

DESCRIPTION

The 'F784 is a serial (n × 8)-bit multiplier with a final stage adder/subtracter for optional use in adding a B bit to obtain S± B. A 'B – 1' bit can also be added via an internal flip-flop to achieve a 1-bit delay. The X word is parallel loaded (8 bits wide) into latches and the Y word is clocked in serially from a shift register. The 'F784 is particularly useful for high-speed digital filtering or butterfly networks in fast Fourier transforms.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F784	65MHz	67mA

ORDERING INFORMATION

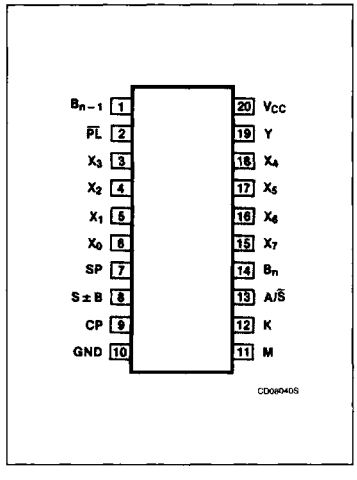
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F784N
20-Pin Plastic SOL	N74F784D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

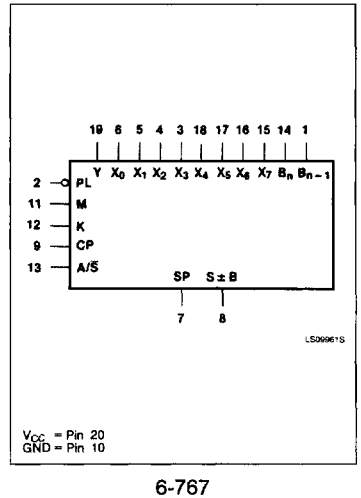
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$X_0 - X_7$	Multiplicand data inputs	1.0/1.0	20μA/0.6mA
Y	Serial multiplier input	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input	1.0/1.0	20μA/0.6mA
K	Serial expansion input	1.0/1.0	20μA/0.6mA
M	Mode control input	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Parallel Load input	1.0/2.0	20μA/1.2mA
A/$\overline{S}$	Add/subtract input	1.0/1.0	20μA/0.6mA
B_n	Serial B input	1.0/1.0	20μA/0.6mA
B_{n-1}	Delayed serial B input	1.0/1.0	20μA/0.6mA
SP	Serial X·Y product output	50/33.3	1mA/20mA
S± B	Serial Y·Y± B output	50/33.3	1mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

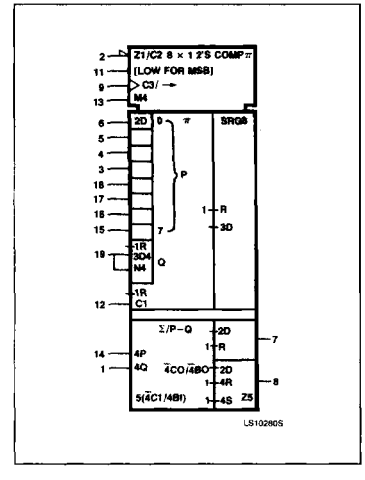
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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Multiplier

FAST 74F784

The 'F784 is a serial/parallel 8-bit multiplier. Also included is an adder/subtracter stage. The X word (multiplicand) is loaded into a register while simultaneously clearing the arithmetic cell flip-flops in preparation for a multiplication. The Y word (multiplier) is clocked in serially.

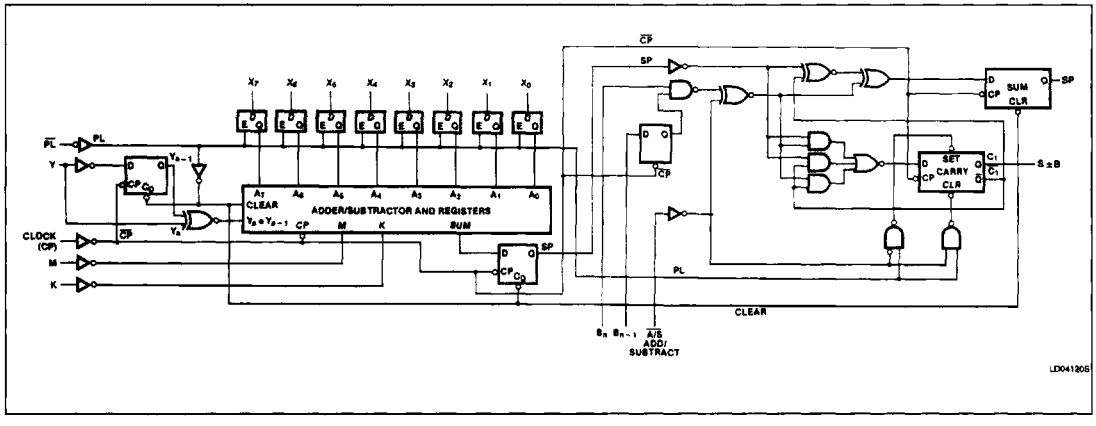
Expansion capability is provided via the M and K inputs. The K (cascade) input is connected to the SO output of the more significant chip. The M (mode) input is used to determine whether the multiplicand is to be treated as a Two's Complement or unsigned number.

The 'F784 has logic to enable complex arithmetic to be performed. A serial adder/subtracter enables constants to be added to the product. Typically, this feature would be used in FFT butterfly networks to reduce package count and power.

Two outputs are provided: the product X•Y and the product X•Y±B. Because of the internal adder/subtracter, a speed advantage is gained when using the 'F784 over using a separate adder and multiplier chip.

During a multiplication operation, the first clock cycle is used to load both the X word (multiplicand) and the first bit of the Y word (operand) into the input registers. At this time there is no valid data at the SP output, so that B bits added will not give the correct sum output. In order to load the first B bit on the same clock as X and Y, a B_{n-1} input is provided which delays the B data by one clock cycle. Thus, a valid output results.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		74F784			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX V_{IH} = MIN,	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	$\overline{PL}$	V_{CC} = MAX, V_I = 0.5V				−1.2	mA
		Others				−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			67	100	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F784					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	50	65		50		MHz
t_{PHL}	Propagation delay $\overline{PL}$ to SP	Waveform 2	6.0		13.0	5.0	14.5	ns
t_{PHL}	Propagation delay $\overline{PL}$ to S ± B	Waveform 2	5.5		12.0	4.5	13.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to SP	Waveform 1	4.0 4.5		9 10.5	3.5 4.0	10.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to S ± B	Waveform 1	4.0 4.0		9.0 9.0	3.5 3.5	10.0 10.0	ns

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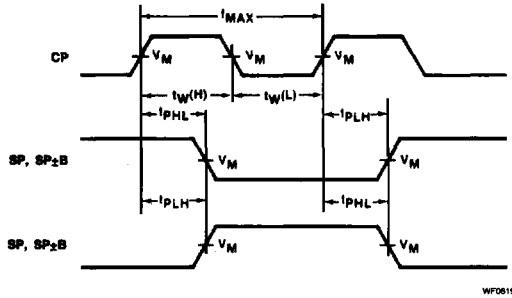
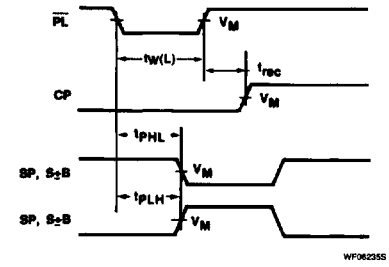
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F784					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time K to CP	Waveform 3	13.0 9.0			14.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time K to CP	Waveform 3	0 1.0			0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time Y to CP	Waveform 3	15 15			16.0 16.0		ns
$t_h(H)$ $t_h(L)$	Hold time Y to CP	Waveform 3	1.5 1.5			1.5 1.5		ns
$t_s(H)$ $t_s(L)$	Setup time X_3 to $\overline{PL}$	Waveform 3	5.0 5.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time X_3 to $\overline{PL}$	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Setup time B_n to CP	Waveform 3	7.0 7.0			8.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time B_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time $A/\overline{S}$ to CP	Waveform 3	12.0 12.0			13.0 13.0		ns
$t_h(H)$ $t_h(L)$	Hold time $A/\overline{S}$ to CP	Waveform 3	1.5 1.5			1.5 1.5		ns
$t_s(H)$ $t_s(L)$	Setup time B_n to CP	Waveform 3	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time B_n to CP	Waveform 3	0 0			1.0 1.0		ns
t_{rec}	Recovery time $\overline{PL}$ to CP	Waveform 2	6.5			7.5		ns
$t_w(L)$	Pulse width		5.0			6.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width	Waveform 1	5.0 5.0			6.0 6.0		ns

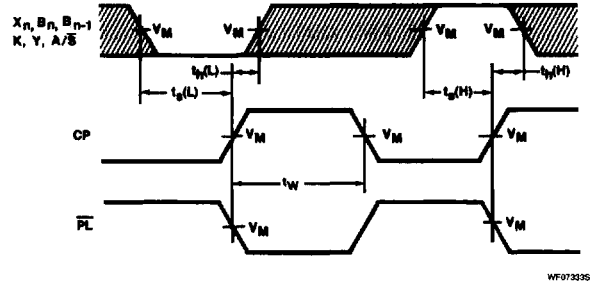
AC WAVEFORMS



Waveform 1. Clock to Output Delays, Clock Pulse Width, and Maximum Clock Frequency



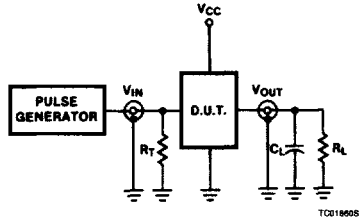
Waveform 2. Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time



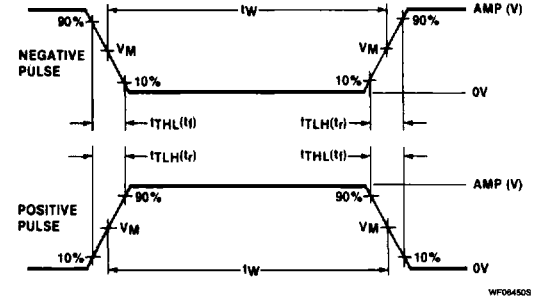
Waveform 3. Data Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

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