T-45-19-05

GigaBit Logic

10G065
10G065K

7 Stage Ripple Counter/Divider
3.0 GHz Clock Rate
10G PicoLogic™ Family

FEATURES

- 3.0 GHz operation (min. @ 25°C)
- 0°C to 85°C commercial temperature range, 10G065
- -40°C to 100°C extended temp. range, 10G065K
- Ripple counting prescaler, divide by 2, 4, 8, 16, 32, 64, and 128
- Ripple up counter with asynchronous clear and clock enable on last six stages
- 10G PicoLogic I/O compatible
- Wire-OR output capability
- Available in flatpack, C-leaded or leadless chip carrier and die form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

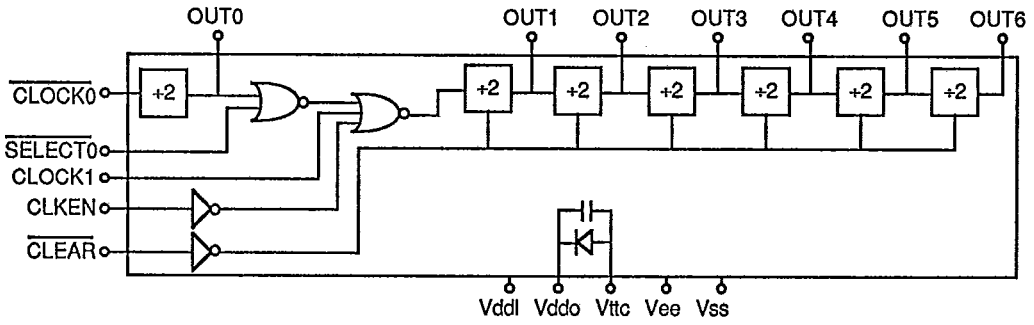
- Frequency Synthesis
- Phased Locked Loops
- Time Interval and Event Counting
- Up Counting

FUNCTIONAL DESCRIPTION

The 10G065 is an ultra- fast 3.0 GHz performance seven stage ripple up counter for frequency synthesis, phased locked loop, counting and time interval measurement applications.The device has two modes of operation; one with all seven stages driven from $\overline{\text{CLOCK0}}$, and another with the last six stages driven from a gated CLOCK1.

For seven stage operation, the $\overline{\text{SELECT0}}$ pin is strapped to VEE (-5.2V), selecting $\overline{\text{CLOCK0}}$ as the clock source. The counter counts up on each high-to-low transition of $\overline{\text{CLOCK0}}$. This mode permits the fastest clocking rate. For six stage operation, the $\overline{\text{SELECT0}}$ pin is strapped to VSS (-3.4V), selecting CLOCK1 as the clock source.

BLOCK DIAGRAM



10G065, 10G065K ORDERING INFORMATION

PACKAGE TYPE	SPEED				
	10G065 (0°C to 85°C)			10G065K (-40°C to 100°C)	
	2.3 GHz	2.0 GHz	1.5 GHz	2.0 GHz	1.5 GHz
36 pin Leadless carrier	10G065-2L36	10G065-L36	10G065-3L36	10G065K-2L36	10G065K-L36
36 pin Flatpack	10G065-2F	10G065-F	10G065-3F	10G065K-2F	10G065K-F
40 pin Leadless carrier	10G065-2L	10G065-L	10G065-3L	10G065K-2L	10G065K-L
40 pin C - Leaded carrier	10G065-2C	10G065-C	10G065-3C	10G065K-2C	10G065K-C
Unpackaged Die			10G065-3X		10G065K-X

T-45-19-05

GigaBit Logic

10G065
10G065K

FUNCTIONAL DESCRIPTION (cont.)

The counter counts up on each low-to-high transition of CLOCK1. A synchronous clock enable, CLKEN, allows CLOCK1 to be gated for counting applications. When CLKEN is high the device will count. When CLKEN is low the device will be inhibited from counting.

In both modes of operation, the asynchronous CLEAR input can be driven low to reset the last six stages of the counter. Because the first stage of the counter is optimized for speed in the seven stage operating mode it does not have a reset capability.

The 10G065 has optional clamp inputs to provide flexibility when interfacing to other components. When connected to a supply voltage at the input threshold of -1.3V, input clamps VICH and VICL allow the 10G065 to be driven with input signals greater than 2.0V p-p without damage to internal gates. This is particularly useful when either 10G065 clock input is driven directly from a voltage controlled oscillator (VCO). When not used, input clamp VICH should be connected to VDDL (GND) and VICL to VSS (-3.4V). Logic clamps VLCH and VLCL provide a means of limiting the voltage swing of internal gates, thus increasing the performance of the divider. The recommended voltages for VLCH and VLCL are indicated with the notes for the AC characteristics specifications. When not used the VLCH and VLCL pins may be left open. The output driver high level clamp, VDCH, may be used to limit VOH when driving ECL. See App. Note 4 for details. When driving GaAs devices, VDCH is typically connected to VDDO.

PIN DESCRIPTIONS

$\overline{\text{CLOCK0}}$	High speed clock input. Drives all seven stages. The falling edge of $\overline{\text{CLOCK0}}$ causes the outputs to change.
CLOCK1	High speed clock input. Drives last six stages. The rising edge of CLOCK1 causes the outputs to change. Must remain low if driving with $\overline{\text{CLOCK0}}$.
$\overline{\text{SELECT0}}$	Selects the mode of operation. For seven stage operation $\overline{\text{SELECT0}}$ is tied to VEE (-5.2V). For six stage operation $\overline{\text{SELECT0}}$ is tied to VSS (-3.4V).
CLKEN	Synchronous clock enable gates the CLOCK1 input to the last six stages. When CLKEN is high the device will count. When CLKEN is low the device will be inhibited from counting.
$\overline{\text{CLEAR}}$	CLEAR is an asynchronous clear function for the last six stages. When driven low it resets the last six stages of the counter to zero.
OUT0-OUT6	Divide by 2, 4, 8, 16, 32, 64, and 128 outputs, respectively.
VDDO	Output driver ground (0V).
VDDL	Internal logic ground (0V).
VSS	-3.4V power supply.
VEE	-5.2V power supply.
VTRIM	Input threshold adjustment voltage. Values of VTRIM more or less negative than VEE will adjust all input thresholds around their nominal value of -1.3V. Connect to VEE or leave open when not used.
VTTC	The AC return pin for the internal VDDO decoupling capacitor. VTTC is not brought into the 10G065 die. VTTC is typically tied to VTT (nominally -2.0V).
VDCH	Output driver clamp supply.When VDCH is connected to VTT = -2.0V the output driver high level is limited to approximately -0.6V, thus providing ECL output compatibility. Consult Application Note #4 for details. When not used, VDCH should be connected to VDDO.
VICH, VICL	Input protection clamp voltages. When connected to -1.3V, these allow an overdriven sine wave input signal to be truncated to a square wave, thus providing faster rise and fall times at either clock input.
VLCH, VLCL	Logic clamp voltages. When connected as specified in the AC Characteristic Notes these pins clamp the internal logic voltage swing of the device, thus enhancing the AC performance of the part. When not used these pins may be left open.

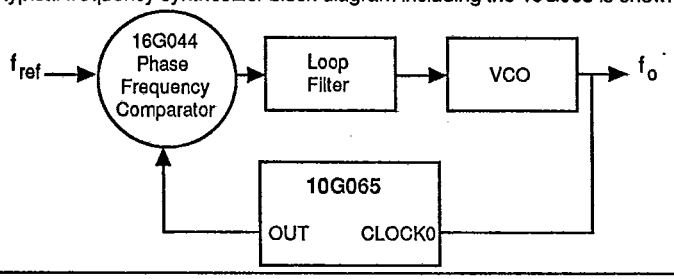
T-45-19-05

GigaBit Logic

10G065
10G065K

Frequency Synthesis Applications

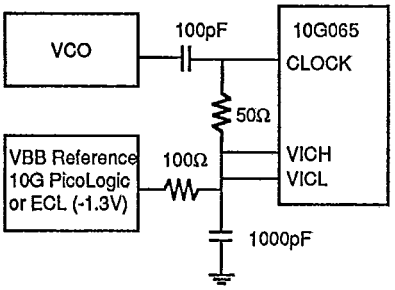
The 10G065 provides the necessary prescaler divider function for phase locked loop frequency synthesis applications. A typical frequency synthesizer block diagram including the 10G065 is shown below.



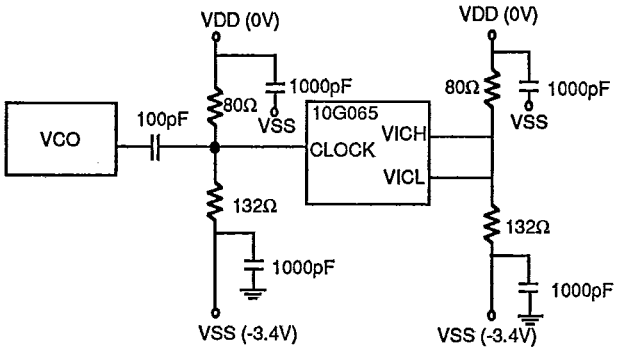
VOLTAGE CONTROLLED OSCILLATOR (VCO) INTERFACE

The CLOCK pin of the 10G065 has an input threshold of -1.3V. To interface the device to a general purpose VCO an AC coupling network is recommended. There are two common cases; one in which the threshold reference voltage (PicoLogic VBBS or ECL VBB output) is available, and another when this voltage is not available.

VCO Interface to 10G065 With VBB Reference



VCO Interface to 10G065 Without VBB Reference



Unlike most PicoLogic circuits, the input threshold of the 10G065 is not stabilized with a VBB feedback circuit. Therefore, the threshold of all inputs will vary from their nominal -1.3V room temperature level with variations in VSS and temperature. VTRIM may be used to adjust input threshold. Alternatively, it is necessary to drive each used input with a large peak-to-peak level signals as shown for VIH and VIL in the DC Characteristics table. Under high speed conditions, the clock input should be ≥2Vp-p to achieve maximum speed as described in the notes to the AC Characteristics tables. Other PicoLogic devices can be used as drivers to provide these levels by terminating driver outputs to VSS instead of VTT.

DESIGN HINTS - TTL OUTPUT LEVELS

The VDDO supply, normally at ground, is the current source for all seven 10G065 output source- follower driver FETs. Aplication Note 4, Fig. 5A recommends that VDDO be biased to -0.5V, when driving a small (100Ω) pull -up load for fast rise time TTL/CMOS output levels, with a 200Ω resistor between VDDO and ground. Since the 10G065 uses this supply (VDDO) for internal transistors, this 200Ω resistor must be changed to 18Ω.

GigaBit Logic

10G065
10G065K

ABSOLUTE MAXIMUM RATINGS
(Beyond which useful life may be impaired) (Note 1)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	-65°C to +150°C	
TJ	Junction Temperature	-55°C to +150°C	
TC	Case Temperature Under Bias	-55°C to +125°C	2
VDDO	Output Driver Supply Voltage	-0.8V to + 1.0 V	
VSS	Supply Voltage	-4.0 V to + 0.5 V	
VEE	Supply Voltage	-7.0 V to VSS + 0.5 V	
VIN	Voltage Applied to Any Input; Continuous VSS = -3.4 V, VEE = -5.2 V	-4.0 V to + 0.5 V	
I IN	Current Into Any Input; Continuous	-0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	-4.0V to + 7.0 V	3
IOUT	Current From Any Output; Continuous	-70 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	3
VTTC	VDDO Internal Decoupling Cap. Return	-6.0 V to VDDO	
VTT	Load Termination Supply	-6.0 V to VDDO + 6.0 V	
VDCH	Output Driver Clamp Voltage	VSS to VDDO	4
IDCH	Output Driver Clamp Current	-20 mA	
VICH	Input Clamp High Voltage	-2.0V to VDDL	5
IICH	Input Clamp High Current	-20mA	
VICL	Input Clamp Low Voltage	VSS to -0.4V	5
IICL	Input Clamp Low Current	20 mA	
VLCH	Logic Clamp High Voltage	-2.0V to VDDL	5
ILCH	Logic Clamp High Current	-40mA	
VLCL	Logic Clamp Low Voltage	VSS TO 0.4V	5
ILCL	Logic Clamp Low Current	-40 mA	

Notes:
1. All voltages specified with VDDL defined as 0 V. Positive current is defined as current into the device.
2. TC is measured at case bottom.
3. Subject to IOUT and power dissipation limitations.
4. Subject to IDCH and power dissipation limitations.
5. Subject to clamp current and power dissipation limitations

RECOMMENDED OPERATING CONDITIONS (note 3)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC1	Case Operating Temp. (10G065)	0	25	85	°C	1
TC2	Case Operating Temp. (10G065K)	-40	25	100	°C	1
VDDL	Logic Supply Voltage		GND		V	
VDDO	Output Driver Supply Voltage	-0.8	GND	1.0	V	
VSS	Supply Voltage	-3.5	-3.4	-3.3	V	
VEE	Supply Voltage	-5.5	-5.2	-5.1	V	
VTTC	VDDO Internal Decoupling Return	VSS	VTT	VDDO	V	
VTT	Load Termination Supply Voltage	VSS	-2.0	-2.0	V	2
RLOAD	Output Termination Load Resistance	25	50	100	Ω	2
VICH	Input Clamp High Voltage	-1.8	VDDL	VDDL	V	
VICL	Input Clamp Low Voltage	VSS	VSS	-0.8	V	
VLCH	Logic Clamp High Voltage	-1.8	VDDL	VDDL	V	
VLCL	Logic Clamp Low Voltage	VSS	VSS	-0.8	V	
VDCH	Output Driver Clamp High Voltage	-2.5	VDDO	VDDO	V	4
VTRIM	Input Threshold Adjust Voltage	VEE-1	VEE	VEE+1	V	

T-45-19-05

GigaBit Logic

10G065
10G065K

RECOMMENDED OPERATING CONDITIONS, cont.

NOTES

1. Tcase measured at case bottom. User attention to device thermal management is recommended. See GigaBit Application Note 3 for a complete discussion of all aspects of device thermal management.
2. The RLOAD and VTT combination used is subject to maximum output current and power restrictions.
3. See GigaBit Application Note 4 for a discussion of interfacing requirements to and from PicoLogic devices.
4. VDCH is not used when driving GaAs logic. To limit VOH when driving ECL logic, consult Application Note 4.

2

10G065/K DC CHARACTERISTICS (Notes1,2)

TC = -40°C to +100°C, VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
VOH	Output Voltage High	- 0.8	-0.6	-0.3	V		
VOL	Output Voltage Low	- 2.0	-1.9	- 1.8	V		
IOH	Output Current High		-70	-60	mA	VOH = -0.8V	
VIH1	Input Voltage High (65)	- 0.6		VDDL	V		4,5
VIL1	Input Voltage Low (65)	VSS		- 1.9	V		4,5
VIH2	Input Voltage High (65K)	-0.6		VDDL	V		4,5
VIL2	Input Voltage Low (65K)	VSS		-2.1	V		4,5
IIN	Input Current		200	500	uA	VIN = -0.7V to -1.9V	
ISS	Power Supply Current		110	200	mA		
IEE	Power Supply Current		18	25	mA		
PD	Power Dissipation		500	850	mW		3

Notes: 1. These characteristics are applicable from DC to 500MHz.
2. Test conditions (unless otherwise indicated) :
VTT = -2.0V VICH = VDDL VLCH = VDDL VDCH = VDDO VTRIM = VEE
VTTC = VTT VICL = VSS VLCL = VSS IOH is the available output current at VOH = -0.8V.
3. At nominal supply voltages and 50% duty cycle. Exclusive of VDDO output source follower power (typically 15 mW per output) and clamp power if any.
4. CLOCK0 and CLOCK1 input rise and fall times ≤ 2ns (measured from the 20% and 80% points).
5. Input levels are 10G PicoLogic level compatible.

PHASE NOISE

	OFFSET (Hz)	RAW L(f)	CORRECTED dBc/Hz
OUT1 (+4)	1K	-111.0	-99.0
	2.5K	-118.3	-106.3
	5.0K	-124.4	-112.4
	7.5K	-127.6	-115.6
	10.0K	-129.5	-117.5
	15.0K	-135.0	-123.0
	20.0K	-136.0	-124.0
	25.0K	-137.8	-125.0

NOTES:
1. Fin = 800MHz.
2. Noise Floor = -160dBc/Hz.
3. Correction is 12dBc/Hz to reference to input.

T-45-19-05

GigaBit Logic

10G065
10G065K

AC CHARACTERISTICS (Note 1)

10G065-2

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK0}}$ Max Toggle Freq.	2.3		3.0			2.3		GHz	2, 3
T2	$\overline{\text{CLOCK0}}$ Low Time	185		165			215		ps	2, 3
T3	$\overline{\text{CLOCK0}}$ High Time	185		165			215		ps	2,3
T4	$\overline{\text{CLOCK0}}$ Low to OUT0		1.7		1.1	1.5		2.0	ns	
T5	$\overline{\text{CLOCK0}}$ Low to OUT1		2.8		1.9	2.5		3.3	ns	
T6	$\overline{\text{CLOCK0}}$ Low to OUT2		3.9		2.6	3.5		4.6	ns	
T7	$\overline{\text{CLOCK0}}$ Low to OUT3		4.8		3.2	4.3		5.6	ns	
T8	$\overline{\text{CLOCK0}}$ Low to OUT4		5.7		3.8	5.1		6.6	ns	
T9	$\overline{\text{CLOCK0}}$ Low to OUT5		6.6		4.4	5.9		7.7	ns	
T10	$\overline{\text{CLOCK0}}$ Low to OUT6		7.5		5.0	6.7		8.7	ns	
T11	CLOCK1 Max Toggle Freq.	2.1		2.4			1.8		GHz	2, 3
T12	CLOCK1 Low Time	225		200			260		ps	2, 3
T13	CLOCK1 High Time	225		200			260		ps	2, 3
T14	CLOCK1 High to OUT1		1.7		1.1	1.5		2.0	ns	
T15	CLOCK1 High to OUT2		2.8		1.9	2.5		3.3	ns	
T16	CLOCK1 High to OUT3		3.9		2.6	3.5		4.6	ns	
T17	CLOCK1 High to OUT4		4.8		3.2	4.3		5.6	ns	
T18	CLOCK1 High to OUT5		5.7		3.8	5.1		6.6	ns	
T19	$\overline{\text{CLOCK1}}$ High to OUT6		6.6		4.4	5.9		7.7	ns	
T20	$\overline{\text{CLEAR}}$ Setup Time				160				ps	
T21	$\overline{\text{CLEAR}}$ Hold Time				160				ps	
T22	$\overline{\text{CLEAR}}$ Pulse Width				550				ps	
T23	$\overline{\text{CLEAR}}$ High to OUT1-6 Low				700				ps	
T24	CLKEN Setup Time				110				ps	
T25	CLKEN Hold Time				110				ps	
Tr	Output Rise Time				500				ps	4
Tf	Output Fall Time				250				ps	4

AC CHARACTERISTICS (Note 1)

10G065

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK0}}$ Max Toggle Freq.	2.0		2.5			2.0		GHz	2, 3
T2	$\overline{\text{CLOCK0}}$ Low Time	250		200			250		ps	2, 3
T3	$\overline{\text{CLOCK0}}$ High Time	250		200			250		ps	2, 3
T4	$\overline{\text{CLOCK0}}$ Low to OUT0		2.4		1.3	1.8		2.4	ns	
T5	$\overline{\text{CLOCK0}}$ Low to OUT1		3.9		2.3	3.0		3.9	ns	
T6	$\overline{\text{CLOCK0}}$ Low to OUT2		5.4		3.1	4.2		5.4	ns	
T7	$\overline{\text{CLOCK0}}$ Low to OUT3		6.4		3.8	5.1		6.4	ns	
T8	$\overline{\text{CLOCK0}}$ Low to OUT4		7.6		4.5	6.1		7.6	ns	
T9	$\overline{\text{CLOCK0}}$ Low to OUT5		8.8		5.3	7.1		8.8	ns	
T10	$\overline{\text{CLOCK0}}$ Low to OUT6		10.0		6.0	8.1		10.0	ns	
T11	CLOCK1 Max Toggle Freq.	1.6		1.7			1.6		GHz	2, 3

T-45-19-05

GigaBit Logic

10G065
10G065K

AC CHARACTERISTICS (Note 1)

10G065

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T12	CLOCK1 Low Time	310		290			310		ps	2, 3
T13	CLOCK1 High Time	310		290			310		ps	2, 3
T14	CLOCK1 High to OUT1		2.3		1.3	1.8		2.3	ns	
T15	CLOCK1 High to OUT2		3.8		2.3	3.0		3.8	ns	
T16	CLOCK1 High to OUT3		5.2		3.1	4.2		5.2	ns	
T17	CLOCK1 High to OUT4		6.4		3.8	5.1		6.4	ns	
T18	CLOCK1 High to OUT5		7.6		4.5	6.1		7.6	ns	
T19	CLOCK1 High to OUT6		8.8		5.3	7.1		8.8	ns	
T20	CLEAR Setup Time				190				ps	
T21	CLEAR Hold Time				190				ps	
T22	CLEAR Pulse Width				650				ps	
T23	CLEAR High to OUT1-6 Low				800				ps	
T24	CLKEN Setup Time				110				ps	
T25	CLKEN Hold Time				110				ps	
Tr	Output Rise Time				500				ps	4
Tf	Output Fall Time				250				ps	4

AC CHARACTERISTICS (Note 1)

10G065-3

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	CLOCK0 Max Toggle Freq.	1.5		2.0			1.5		GHz	2, 3
T2	CLOCK0 Low Time	330		250			330		ps	2, 3
T3	CLOCK0 High Time	330		250			330		ps	2,3
T4	CLOCK0 Low to OUT0		2.9		1.9	2.4		2.9	ns	
T5	CLOCK0 Low to OUT1		4.9		2.9	3.9		4.9	ns	
T6	CLOCK0 Low to OUT2		6.9		3.9	5.4		6.9	ns	
T7	CLOCK0 Low to OUT3		8.5		4.8	6.4		8.5	ns	
T8	CLOCK0 Low to OUT4		11.0		5.7	7.6		11.0	ns	
T9	CLOCK0 Low to OUT5		12.0		6.6	8.8		12.0	ns	
T10	CLOCK0 Low to OUT6		14.0		7.5	10.0		14.0	ns	
T11	CLOCK1 Max Toggle Freq.	1.4		1.6			1.4		GHz	2, 3
T12	CLOCK1 Low Time	350		310			350		ps	2, 3
T13	CLOCK1 High Time	350		310			350		ps	2, 3
T14	CLOCK1 High to OUT1		2.9		1.7	2.4		2.9	ns	
T15	CLOCK1 High to OUT2		4.9		2.9	3.9		4.9	ns	
T16	CLOCK1 High to OUT3		6.9		3.9	5.4		6.9	ns	
T17	CLOCK1 High to OUT4		8.5		4.8	6.4		8.5	ns	
T18	CLOCK1 High to OUT5		11.0		5.7	7.6		11.0	ns	
T19	CLOCK1 High to OUT6		12.0		6.6	8.8		12.0	ns	
T20	CLEAR Setup Time				260				ps	
T21	CLEAR Hold Time				260				ps	
T22	CLEAR Pulse Width				1100				ps	

T-45-19-05

GigaBit Logic

10G065
10G065K

AC CHARACTERISTICS (Note 1)

10G065-3

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T23	$\overline{\text{CLEAR}}$ High to OUT1-6 Low				1200				ps	
T24	CLKEN Setup Time				140				ps	
T25	CLKEN Hold Time				140				ps	
Tr	Output Rise Time				500				ps	4
Tf	Output Fall Time				250				ps	4

AC CHARACTERISTICS (Note 1)

10G065K-2

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= -40°C		Tc = +25°C			Tc= +100°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK0}}$ Max Toggle Freq.	2.0		3.0			2.0		GHz	2, 3
T2	$\overline{\text{CLOCK0}}$ Low Time	250		165			250		ps	2, 3
T3	$\overline{\text{CLOCK0}}$ High Time	250		165			250		ps	2,3
T4	$\overline{\text{CLOCK0}}$ Low to OUT0		2.4		1.1	1.5		2.4	ns	
T5	$\overline{\text{CLOCK0}}$ Low to OUT1		3.9		1.9	2.5		3.9	ns	
T6	$\overline{\text{CLOCK0}}$ Low to OUT2		5.4		2.6	3.5		5.4	ns	
T7	$\overline{\text{CLOCK0}}$ Low to OUT3		6.4		3.2	4.3		6.4	ns	
T8	$\overline{\text{CLOCK0}}$ Low to OUT4		7.6		3.8	5.1		7.6	ns	
T9	$\overline{\text{CLOCK0}}$ Low to OUT5		8.8		4.4	5.9		8.8	ns	
T10	$\overline{\text{CLOCK0}}$ Low to OUT6		10.0		5.0	6.7		10.0	ns	
T11	CLOCK1 Max Toggle Freq.	1.6		2.4			1.6		GHz	2, 3
T12	CLOCK1 Low Time	200		200			310		ps	2, 3
T13	CLOCK1 High Time	200		200			310		ps	2, 3
T14	CLOCK1 High to OUT1		2.3		1.1	1.5		2.3	ns	
T15	CLOCK1 High to OUT2		3.8		1.9	2.5		3.8	ns	
T16	CLOCK1 High to OUT3		5.2		2.6	3.5		5.2	ns	
T17	CLOCK1 High to OUT4		6.4		3.2	4.3		6.4	ns	
T18	CLOCK1 High to OUT5		7.6		3.8	5.1		7.6	ns	
T19	$\overline{\text{CLOCK1}}$ High to OUT6		8.8		4.4	5.9		8.8	ns	
T20	$\overline{\text{CLEAR}}$ Setup Time				160				ps	
T21	$\overline{\text{CLEAR}}$ Hold Time				160				ps	
T22	$\overline{\text{CLEAR}}$ Pulse Width				550				ps	
T23	CLEAR High to OUT1-6 Low				700				ps	
T24	CLKEN Setup Time				110				ps	
T25	CLKEN Hold Time				110				ps	
Tr	Output Rise Time				500				ps	4
Tf	Output Fall Time				250				ps	4

T-45-19-05

GBL GigaBit Logic

10G065
10G065K

10G065K

AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc= -40°C		Tc = +25°C			Tc= +100°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	$\overline{\text{CLOCK0}}$ Max Toggle Freq.	1.5		2.5			1.5		GHz	2, 3
T2	$\overline{\text{CLOCK0}}$ Low Time	330		200			330		ps	2, 3
T3	$\overline{\text{CLOCK0}}$ High Time	330		200			330		ps	2, 3
T4	$\overline{\text{CLOCK0}}$ Low to OUT0		2.9		1.3	1.8		2.9	ns	
T5	$\overline{\text{CLOCK0}}$ Low to OUT1		4.9		2.3	3.0		4.9	ns	
T6	$\overline{\text{CLOCK0}}$ Low to OUT2		6.9		3.1	4.2		6.9	ns	
T7	$\overline{\text{CLOCK0}}$ Low to OUT3		8.5		3.8	5.1		8.5	ns	
T8	$\overline{\text{CLOCK0}}$ Low to OUT4		11.0		4.5	6.1		11.0	ns	
T9	$\overline{\text{CLOCK0}}$ Low to OUT5		12.0		5.3	7.1		12.0	ns	
T10	CLOCK0 Low to OUT6		14.0		6.0	8.1		14.0	ns	
T11	CLOCK1 Max Toggle Freq.	1.4		1.7			1.4		GHz	2, 3
T12	CLOCK1 Low Time	350		290			350		ps	2, 3
T13	CLOCK1 High Time	350		290			350		ps	2, 3
T14	CLOCK1 High to OUT1		2.9		1.3	1.8		2.9	ns	
T15	CLOCK1 High to OUT2		4.9		2.3	3.0		4.9	ns	
T16	CLOCK1 High to OUT3		6.9		3.1	4.2		6.9	ns	
T17	CLOCK1 High to OUT4		8.5		3.8	5.1		8.5	ns	
T18	CLOCK1 High to OUT5		11.0		4.5	6.1		11.0	ns	
T19	$\overline{\text{CLOCK1}}$ High to OUT6		12.0		5.3	7.1		12.0	ns	
T20	$\overline{\text{CLEAR}}$ Setup Time				190				ps	
T21	$\overline{\text{CLEAR}}$ Hold Time				190				ps	
T22	$\overline{\text{CLEAR}}$ Pulse Width				650				ps	
T23	CLEAR High to OUT1-6 Low				800				ps	
T24	CLKEN Setup Time				110				ps	
T25	CLKEN Hold Time				110				ps	
Tr	Output Rise Time				500				ps	4
Tf	Output Fall Time				250				ps	4

NOTES: 1. Test Conditions, unless otherwise stated:

Ta = 25°C	VICH = 0V	VDCH = 0V
VDDL = VDDO = 0V	VICL = VSS	VDCL = VSS
VEE = -5.2V	VLCH = -1.5V	VOH ≥ -0.8V
VSS = -3.4V	VLCL = -1.25V	VOL ≤ -1.8V
RLOAD = 50Ω to -2.0V	VTTC = -2.0V	VTRIM = VEE

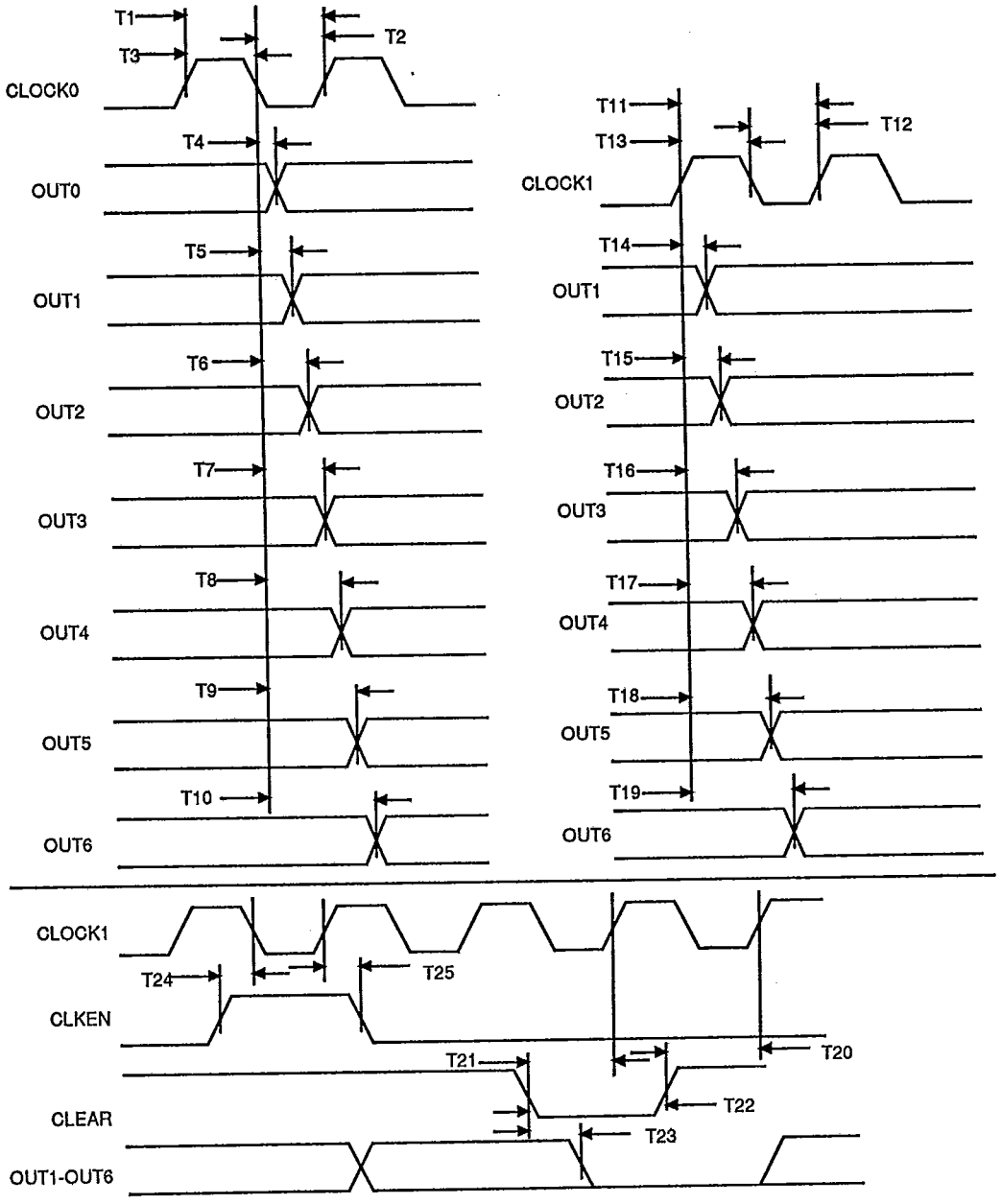
2. $\overline{\text{CLOCK0}}$ and CLOCK1 rise and fall times ≤150ps (measured from the 20% and 80% points)
3. $\overline{\text{CLOCK0}}$ and CLOCK1 input = 2V pp sine wave, -1.3V DC offset.
4. Rise and Fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

T-45-19-05

GigaBit Logic

10G065
10G065K

SWITCHING WAVEFORMS



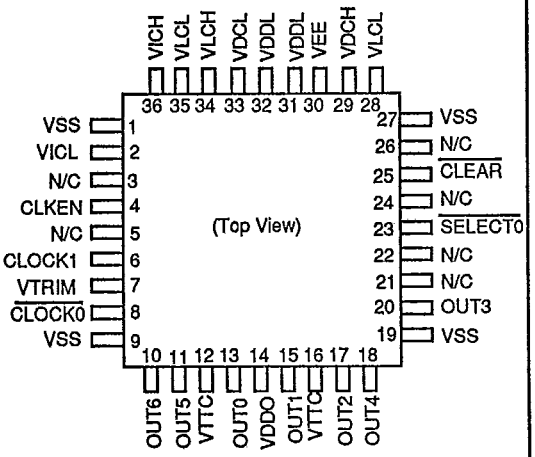
T-45-19-05

GigaBit Logic

10G065
10G065K

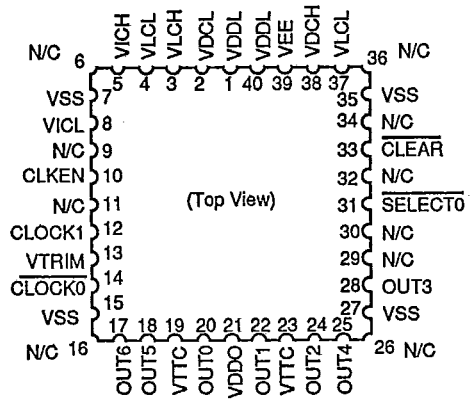
PACKAGE PINOUT DIAGRAM

36 LEAD FLATPACK
PACKAGE TYPE "F"



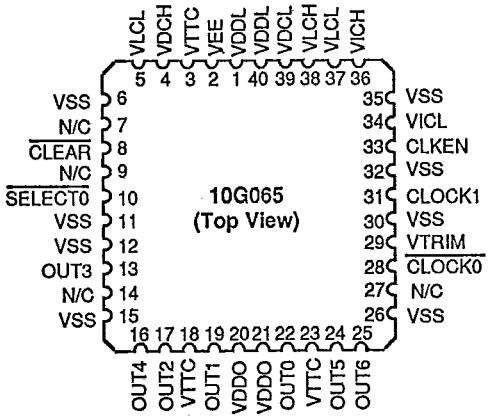
NOTES: Pin 1 is marked for orientation. N/C = No Connection. The package bottom surface is at VSS potential.

36 I/O LEADLESS CHIP CARRIER
PACKAGE TYPE "L36"



NOTES: Pin 1 is marked for orientation. N/C = No Connection. The package lid, bottom heat vias, and 4 N/C corner pins (6,16,26,36) are at Vss potential.

Pin Functions - 40 Pin Type "C" and "L" Packages



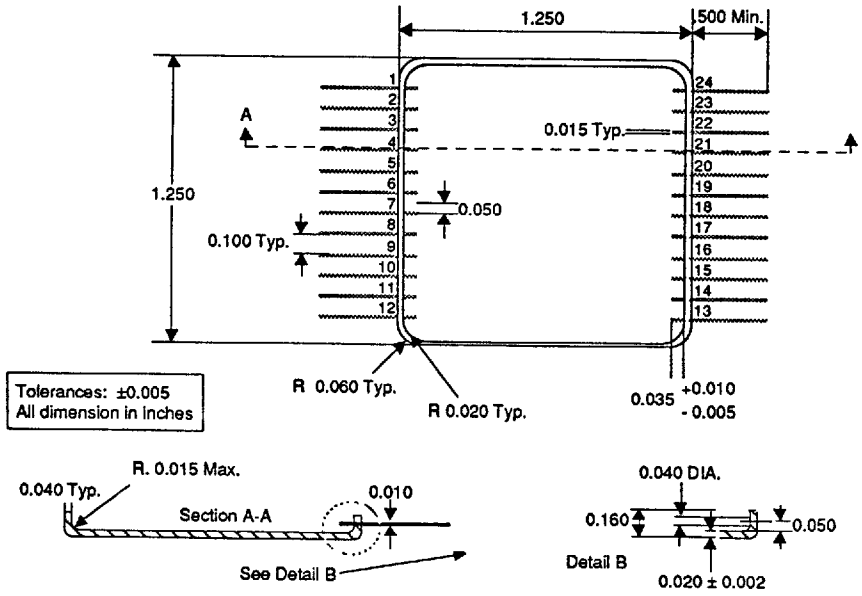
N/C = No Connection

T-90-20

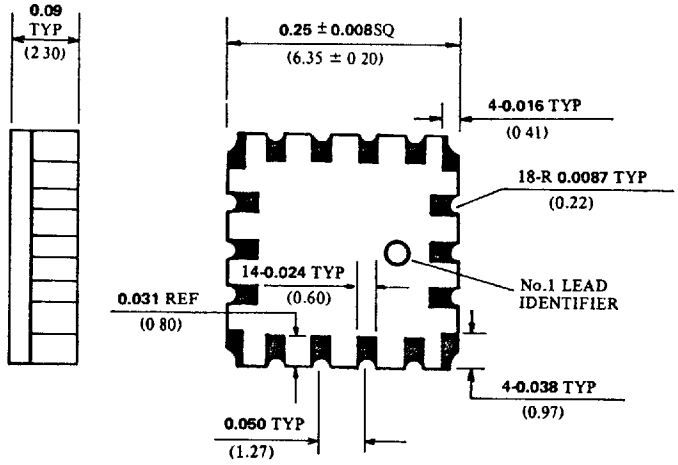
GigaBit Logic

24 PIN METAL FLATPACK
18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H



18 PIN LEADLESS CHIP CARRIER
TYPE L1



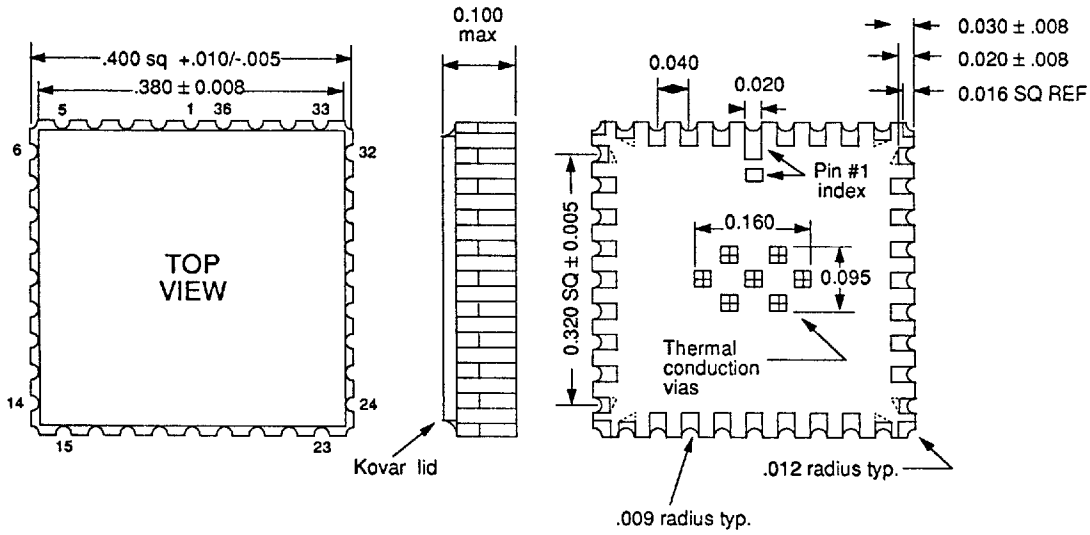
All dimensions shown in inches and (millimeters)

11

GigaBit Logic

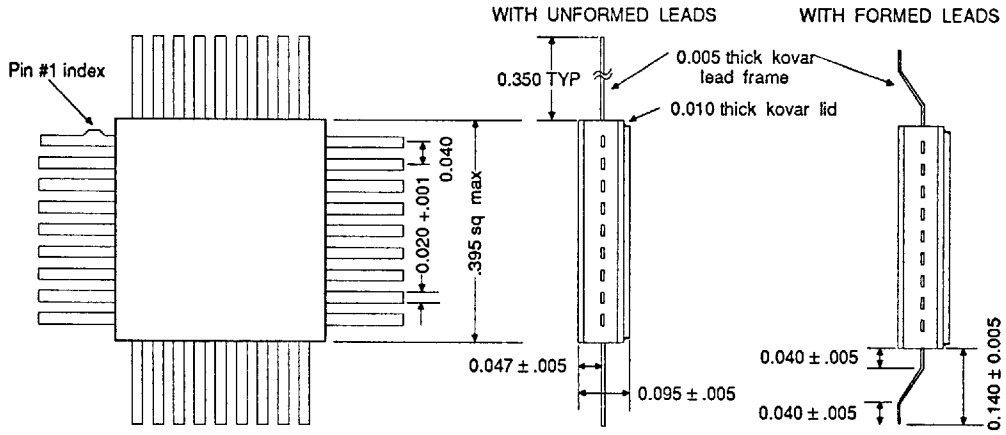
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F

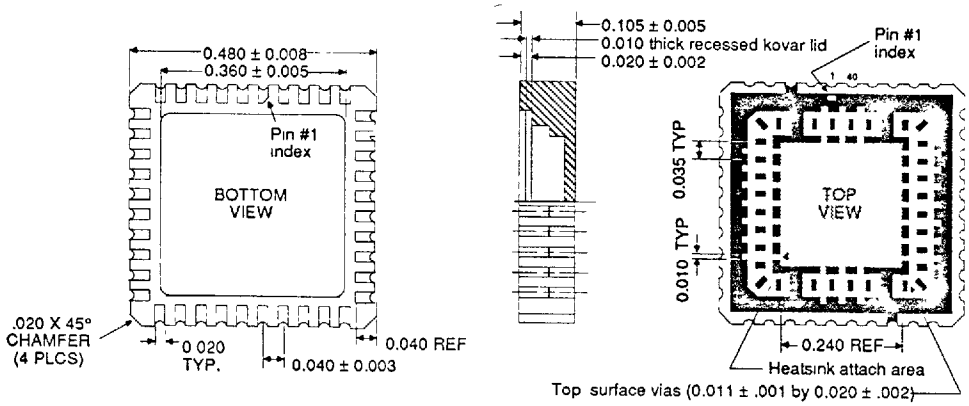


T-90-20

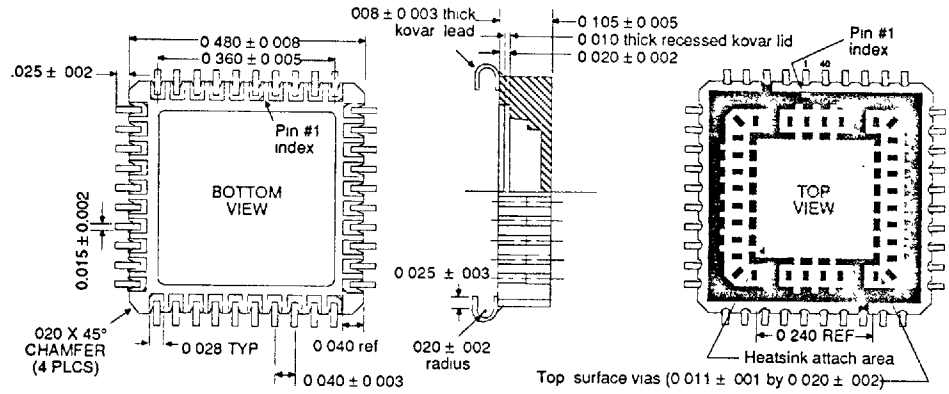
GigaBit Logic

40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L

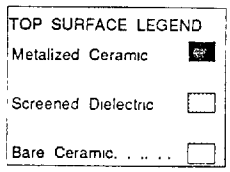


40 PIN LEADED CHIP CARRIER
TYPE C

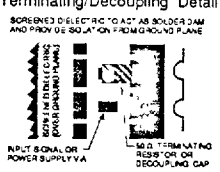


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip resistors are 0 040 long by 0 020 wide by 0 010 thick typ 100 mw min nominal power rating (Mini-Systems MSR 21 or equivalent)
(5) Recommended top surface chip capacitors are 0 040 long by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks are GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width



Top Surface Terminating/Decoupling Detail

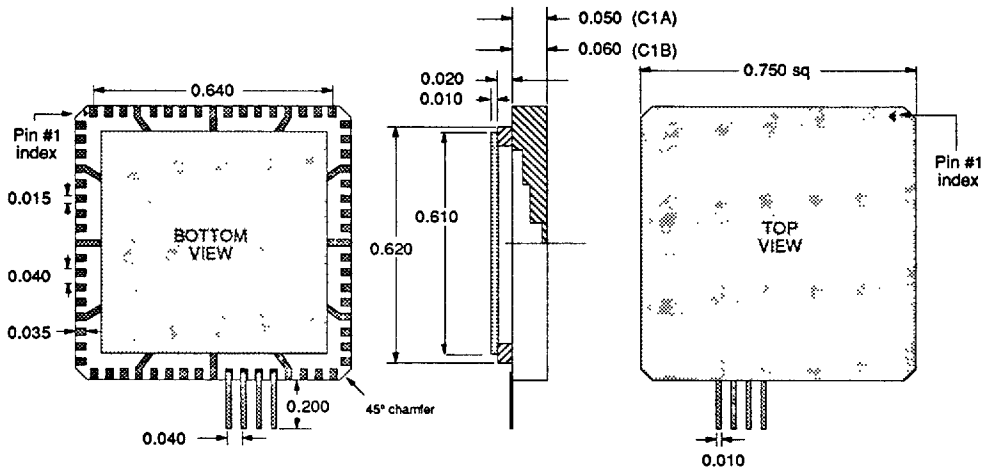


T-90-20

GigaBit Logic

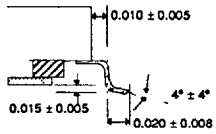
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3