VITESSE

VSC838
Data Sheet

3.2Gb/s 36x36 Crosspoint Switch

FEATURES

- 36 Input by 36 Output Crosspoint Switch
- 3.2Gb/s NRZ Data Bandwidth
- Non-Blocking Architecture Broadcast and Multicast Capabilities
- LVTTL/2.5V CMOS Control I/O (3.3V tolerant)
- Input Signal Activity (ISA) Monitoring Function
- Integrated Signal Equalization (ISE) for Deterministic Jitter Reduction
- 66MHz Dual Programming Port
- Parallel and Serial Programming Modes
- Programmable On-Chip I/O Termination
- Differential CML Output Drivers
- Single 2.5V Supply
- 6W Typical, Low Drive Mode
  7W Typical, High Drive Mode
- High Performance 37.5mm, 480-Pin TBGA Package

GENERAL DESCRIPTION

The VSC838 is a monolithic 36x36 asynchronous crosspoint switch, designed to carry broadband data streams. The VSC838 also has an internal 37th output channel which is used in conjunction with the Input Signal Activity Monitoring to allow in system diagnostics. A high degree of signal integrity is maintained throughout the chip via fully differential signal paths.

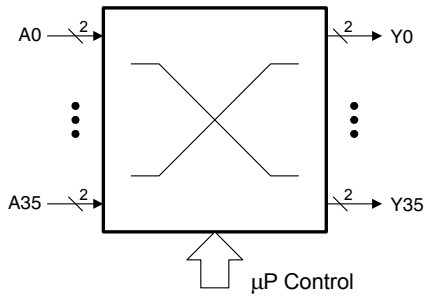
The crosspoint function is based on a multiplexer array architecture. Each data output is driven by a 36:1 multiplexer that can be programmed to one and only one of its 36 inputs. The signal path is unregistered and fully asynchronous, so there are not any restrictions on the phase, frequency, or signal pattern at each input.

Each high-speed output is a fully differential, switched current driver with switchable on-die terminations for maximum signal integrity. Data inputs are terminated on-die through 100Ω impedance between true and complement inputs (see "Input Terminations" on page 9 for further details).

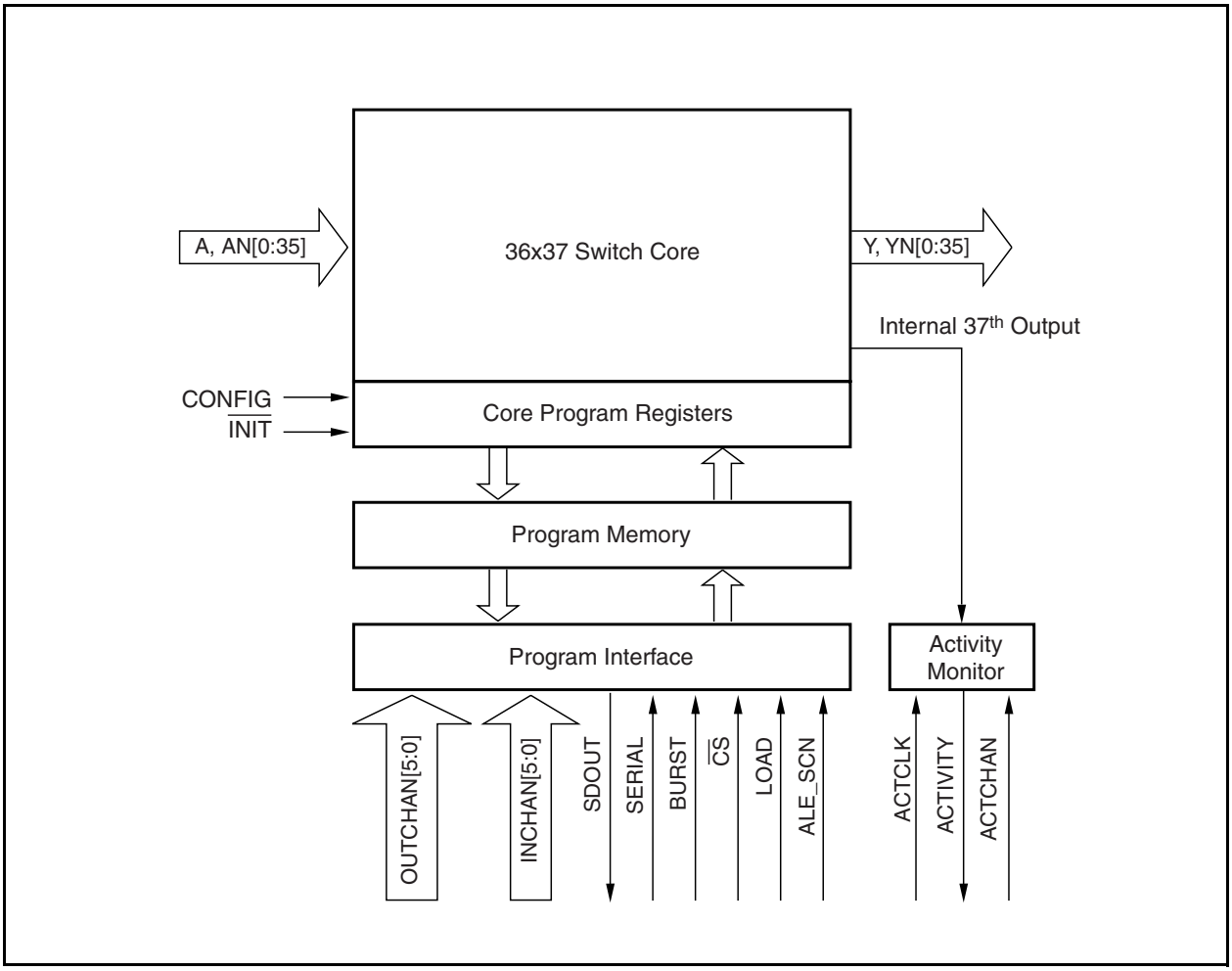
A dual mode programming interface is provided that allows programming commands to be sent as serial data or parallel data. Core programming can be random for each port address, or multiple program assignments can be queued and issued simultaneously. The programming may be initialized to a "straight-through" configuration (A0 to Y0, A1 to Y1, etc.) using the $\overline{\text{INIT}}$ pin.

Unused channels may be powered down to allow efficient use of the switch in applications that require only a subset of the channels. Power-down can be accomplished in hardware via dedicated power pins for pairs of input and output channels, or in software by programming individual unused outputs with a disable code.

VSC838 Block Diagram



VSC838 Functional Block Diagram



FUNCTIONAL DESCRIPTION

Input/Output Characteristics

All input data must be differential and should be nominally biased to +2.0V or AC-coupled. Other levels are allowed as described under "Input Terminations" on page 9. On-chip terminations are provided, with a nominal impedance of 100Ω differential. All input termination resistors float with an internal bias provided for AC-coupling.

For direct interconnection of multiple VSC838 devices, a CML termination mode is provided by tying the ITC pin to V_{CC}, which ties the center point of the 100Ω termination to V_{CC}, causing the terminations to act as loads for an open-drain or open-collector differential output.

Data outputs are provided through differential current switches with on-chip back-termination. The output circuit is capable of driving external 50Ω far-end termination (recommended). The output back-terminations are electronically switchable to enable a power savings of 1W (max) by reducing the output driver current.

Programming Interface

Parallel Mode

In parallel mode (SERIAL=0), the binary word on INCHAN[5:0] is the numerical identifier of the input that will be routed to the specified output. OUTCHAN[5:0] is the numerical identifier of the output being programmed. A rising edge on the LOAD signal will transfer the programming data to the shadow register in the program memory. Raising CONFIG (asynchronously) will transfer the programming data to the main latches in the program memory and cause the internal select signals in the core to re-configure the multiplexer. Lowering CONFIG will latch the main latches. CONFIG may be tied HIGH to enable programming to take effect instantaneously.

This interface may be used with multiplexed address/data buses by using only INCHAN[5:0] without OUTCHAN[5:0] and dropping ALE when the address of the output to be programmed is present on INCHAN[5:0]. After the address is latched, the input address may be presented on INCHAN[5:0] and programming proceeds as above.

No read-back capability is provided in parallel mode. Read-back for diagnostic purposes is provided in serial mode via the scan function.

Serial Mode

In serial mode (SERIAL=1), the INCHAN[0] pin becomes the serial data input SDIN and the INCHAN[1] pin becomes the serial clock SCLK (rising edge triggered). A serial word of the form [Output][Input] is shifted into the internal shift register, and the LOAD pin is asserted (HIGH) coincident with the last bit of the data word to signal that the word is to be applied. This transfers the input identifier to the shadow register of the addressed output. CONFIG is then applied (asynchronously) to transfer one or more program commands to the main latches of the program memories.

The SDOUT pin follows the data on the INCHAN[0](SDIN) pin 14 clock cycles later. This enables the user to chain the serial ports of several crosspoints, shift program data for all switches through such a chain, and assert LOAD on all switches to program all of the connections simultaneously.

The output field is 7 bits long, representing the binary numerical identifier of the output to be programmed. The input field is 7 bits long, representing the numerical identifier of the input that will be routed to the specified output.

Serial Read-Back

Read-back of the program memory contents is accomplished in serial mode by setting the ALE_SCN pin HIGH. This will serially shift out the contents of the main latches in the program memories, slice 36 first and slice 0 last, and MSB-first, LSB-last for each 7-bit word (see Figure 3 on page 7). One rising edge of INCHAN[1](SCLK) with ALE_SCN=0 and SERIAL=1 must occur to load the entire 483-bit shift register prior to shifting out data. At a clock rate of 66MHz, this operation takes 7.26µs.

Activity Monitoring

The activity monitor observes the output of the internal 37th output from the core. By programming the 37th output to observe various inputs, the input signals can be scanned for activity or lack thereof. Each rising edge of ACTCLK causes the monitor to read out the activity state from the previous ACTCLK period and clears the internal activity state until a data transition triggers it again. There must be a minimum of one rising and one falling edge on the observed input data pin during the ACTCLK period for activity to be detected. After power-on the output of ACTIVITY after the first ACTCLK rising edge is unknown.

To program the activity channel, ACTCHAN must be set HIGH and OUTCHAN[5:0] must be set to 100000. Set INCHAN[5:0] to the desired input channel to be monitored. For all other programming operations, ACTCHAN must be LOW.

Selective Power-Down

Unused input and output channels can be made to consume little or no power via one of two methods of selective power-down.

Software Power-Down

Using this feature, unused outputs may be disabled, saving approximately 150 mW per output channel for maximum dissipation conditions. This is accomplished by programming each unused output to look at input 63 (3F Hex), which represents a non-existent input channel. The channel may be subsequently activated by programming a valid input address. It is recommended, however, that any changes in power programming only be executed as part of an initialization sequence to guard against the effects of any switching transients that might result from changing the power supply current suddenly. Software mode does not affect the functioning or power of unused input channels.

Hardware Power-Down

Using this feature, the power associated with given input channel pairs may be shut off by tying the corresponding V_{EE} pin to V_{CC} (see Table 11 on page 12). Up to seventeen outputs may be powered off in this manner. Approximately 150mW per input channel pairs is saved under the maximum dissipation conditions. The power associated with given output channel pairs, including their contribution to the core power, can be shut off by tying the corresponding V_{EE} pin to V_{CC} (see Table 11 on page 12). Approximately 300mW per two output channels is saved under the maximum dissipation conditions.

Certain V_{EE} pins must always be active. In other words, tied to the most negative supply, so the corresponding inputs and outputs will always be on and consuming power. See Figure 6 on page 11 and Table 11 on page 12 for the location of these pins.

SPECIFICATIONS

AC Characteristics

All characteristics are specified over the recommended operating conditions.

Table 1. Data Path

Symbol	Parameter	Min	Typ	Max	Unit
f_{RATE}	Maximum data rate			3.2	Gb/s
t_{SKW}	Channel-to-channel delay skew		300		ps
t_{PDAY}	Propagation delay from an A input to a Y output		750		ps
t_R, t_F	High-speed input and output rise/fall times, 20% to 80%[1]			150	ps
t_{JR}	Output added delay jitter, rms[2, 3]			10	ps
t_{JP}	Output added delay jitter, peak-to-peak[2, 3]			40	ps

1. *The high-speed input rise/fall time must be ≤150ps.*
2. *Guaranteed by design, but not tested.*
3. *Broadband (unfiltered) deterministic jitter added to a jitter-free input. 2^{23}-1 PRBS data pattern.*

Table 2. Program Interface Timing[1]

Symbol	Parameter	Min	Typ	Max	Unit
$t_{s\overline{WR}}$	Setup time from INCHAN[5:0] or OUTCHAN[5:0] to rising edge of $\overline{WR}$	3.35			ns
$t_{h\overline{WR}}$	Hold time from rising edge of $\overline{WR}$ to INCHAN[5:0] or OUTCHAN[5:0]	1.45			ns
t_{pwLW}	Pulse width (HIGH or LOW) on LOAD	6.75			ns
$t_{s\overline{CS}}$	Setup time from $\overline{CS}$ to falling edge of LOAD or ALE_SCN in parallel, or rising edge of LOAD in serial mode.	0			ns
$t_{h\overline{CS}}$	Hold time of $\overline{CS}$ rising edge after LOAD or ALE_SCN rising in parallel, falling edge of LOAD in serial mode, or falling edge of CONFIG in any mode.	0			ns
t_{pwCFG}	Pulse width (HIGH or LOW) on CONFIG	6.75			ns
t_{sSDIN}	Setup time from INCHAN0_SDIN to INCHAN1_SCLK rising	1.65			ns
t_{hSDIN}	Hold time of INCHAN0_SDIN after INCHAN1_SCLK rising	1.0			ns
$t_{perSCLK}$	Minimum period of SCLK in serial mode	15			ns
t_{sLOAD}	Setup time from LOAD to INCHAN1_SCLK rising	1.85			ns
t_{hLOAD}	Hold time of LOAD after INCHAN1_SCLK rising	0.95			ns
$t_{sSERIAL}$	Setup time from SERIAL rising to INCHAN1_SCLK rising when entering serial mode or SERIAL falling to LOAD falling when entering parallel mode.	0.90			ns
$t_{hSERIAL}$	Hold time from INCHAN1_SCLK rising to SERIAL falling when exiting serial mode.	0			ns
t_{dsDOUT}	Delay from INCHAN1_SCLK rising to SDOUT, 20pF load.			6.20	ns
$t_{pw\overline{INIT}}$	Pulse width (HIGH or LOW) on $\overline{INIT}$	6.75			ns
t_{sSCAN}	Setup time from ALE_SCN to INCHAN1_SCLK rising when starting or completing a serial read-back sequence.	1.65			ns
t_{hSCAN}	Hold time of ALE_SCN after INCHAN1_SCLK rising when starting or completing a serial read-back sequence.	1.0			ns

1. *Specifications are guaranteed by design, but not tested.*

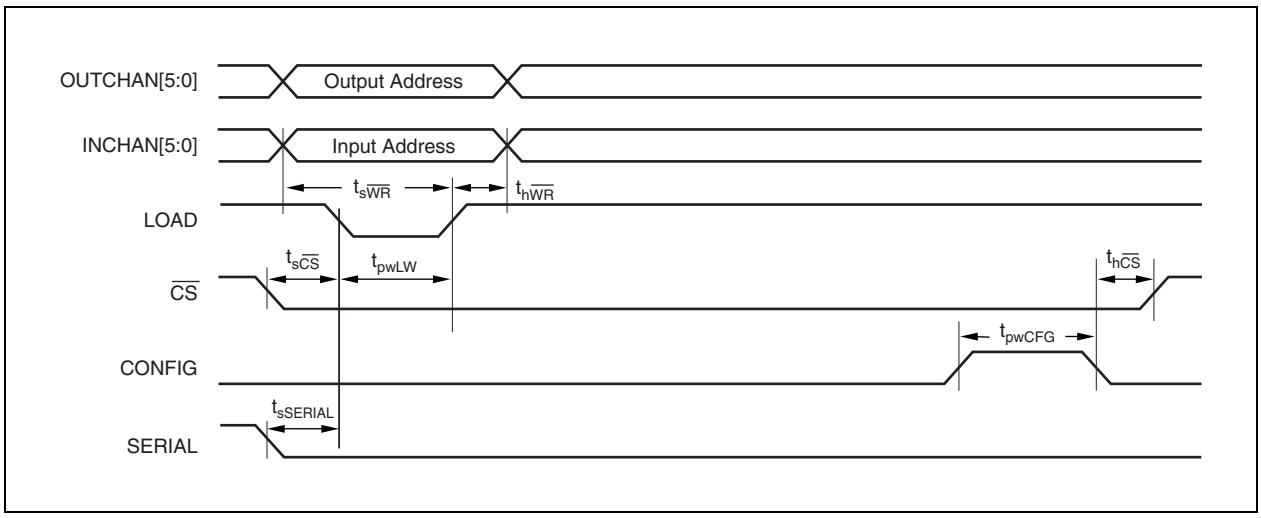


Figure 1. Parallel Mode—Separate Address/Data (leave ALE_SCN pin HIGH)

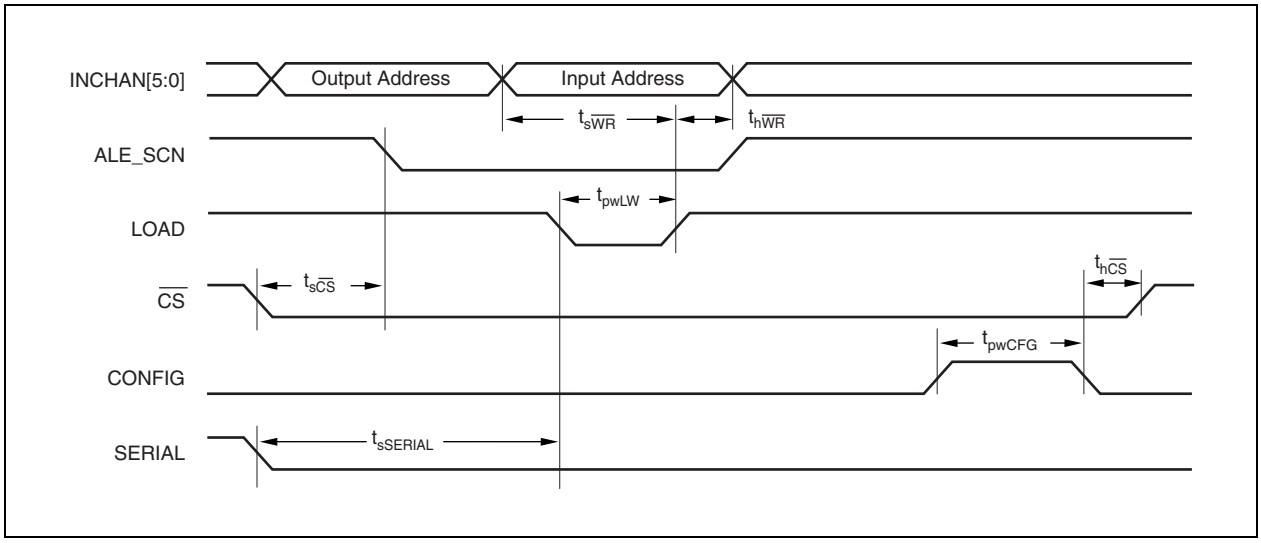


Figure 2. Parallel Mode—Multiplexed Address/Data

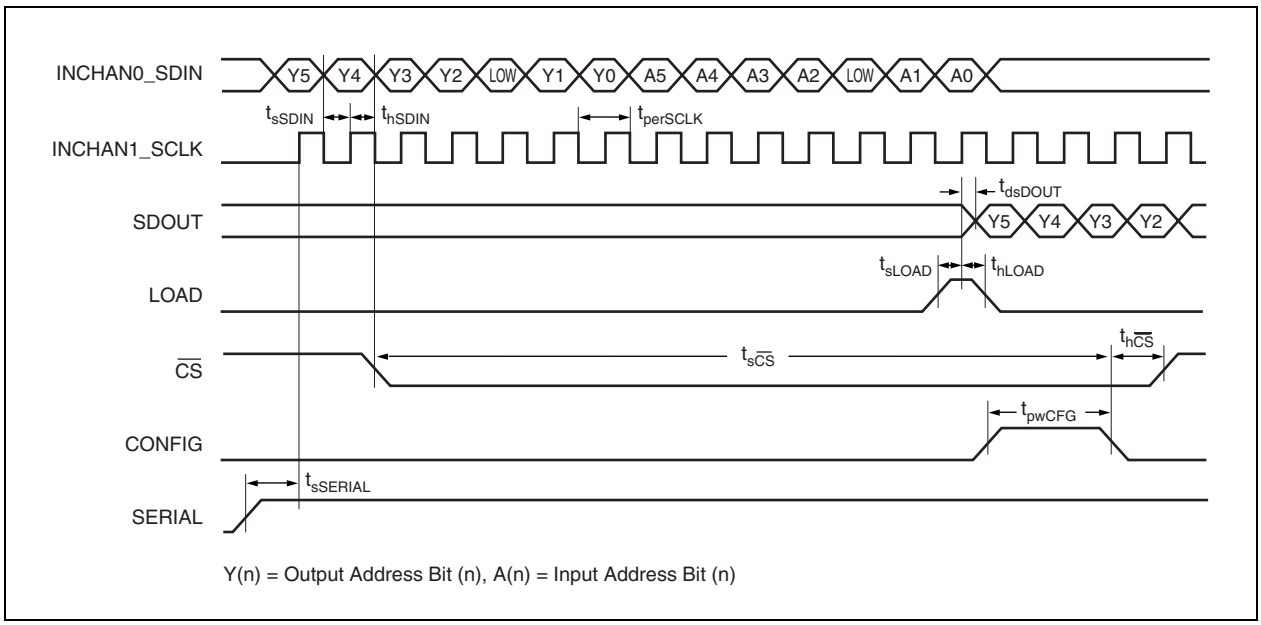


Figure 3. Serial Mode (leave ALE_SCN pin LOW during programming)

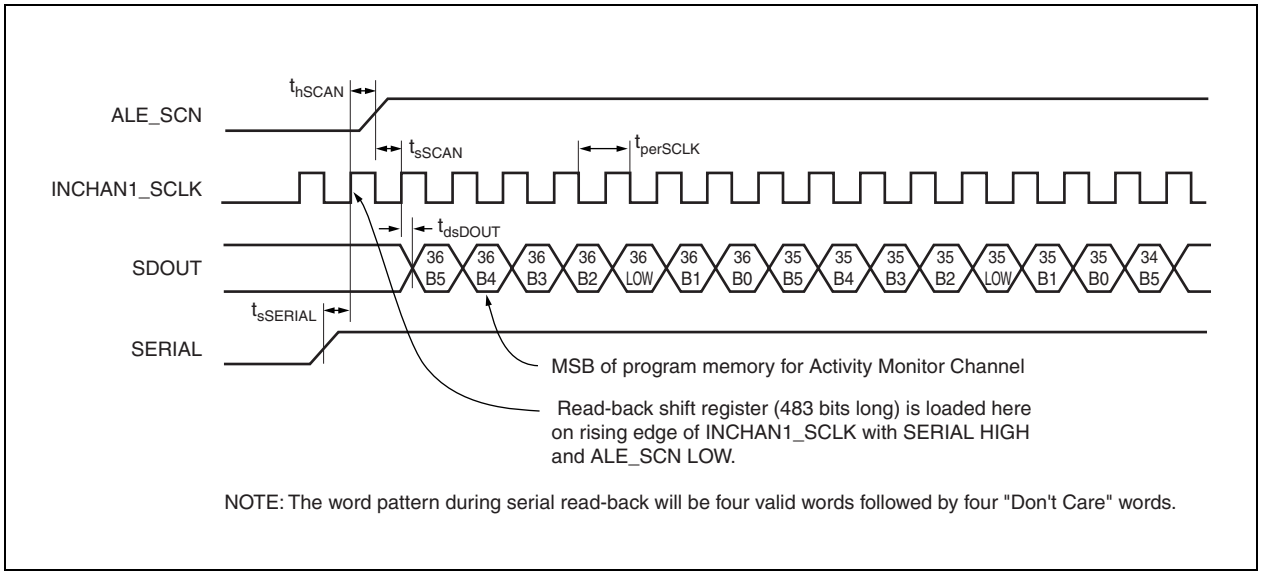


Figure 4. Serial Readback

DC Characteristics

All characteristics are specified over the recommended operating conditions.

Table 3. Power Supply Requirements

Symbol	Parameter	Min	Typ	Max	Unit	Condition
I_{CC}	V_{CC} supply current		2286	3428	mA	
P_T	Total chip power (with I_{TERM} = 0 and back-terminations ON, high drive)		6	9	W	Max P_T is with +5% supply, +85°C case temperature and high drive

Table 4. Control Port Input Levels (LVTTL/CMOS)[1]

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH voltage	1.7		V_{CC} + 1.0	V	
V_{IL}	Input LOW voltage	0		0.8	V	
$I_{IH\_2.5V}$	Input HIGH current		100		µA	When driven with 2.5V logic.
$I_{IH\_3.3V}$	Input HIGH current		200		µA	When driven with 3.3V logic.
I_{IL}	Input LOW current		100		µA	
V_{OH}	Output HIGH voltage	V_{CC} _ 0.2		V_{CC}	V	DC load <500µA
V_{OL}	Output LOW voltage	0		0.2	V	DC load <2mA
V_{OHPU}	V_{OH} with external pull-up	2.4			V	250Ω to 3.3V (5%)
V_{OLPU}	V_{OL} with external pull-up			0.4	V	250Ω to 3.3V (5%)

1. Specifications are guaranteed by design, but not tested.

Table 5. Signal Input levels (high-speed signal path)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IN}	Input voltage amplitude[1]	150		1100	mV	See Note 1
V_{ICM}	Input common-mode voltage[2]	V_{CC} – 0.7		V_{CC} – 0.2	V	See Note 2

1. *Mean peak-to-peak amplitude measurement of either true or complement of the differential signal.*

2. *V_{CC} = V_{CCP} = 2.5V, V_{EE} = 0V.*

Table 6. Signal Output Levels (high-speed signal path) TERM_CTRL=ON, DRIVE_CTRL=HI

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{OUT}	Output differential voltage[1, 2]	400		600	mV	See Notes 1, 3
V_{OCM}	Output common-mode voltage[2, 3]	V_{CC} - 0.3		V_{CC} - 0.2	V	See Notes 2, 3

1. *Mean peak-to-peak amplitude measurement of either true or complement of the differential signal.*

2. *Terminated in 50Ω to V_{CC}. This termination is used for testing the part, but other terminations are allowed—see Table 8 on page 10.*

3. *V_{CC} = V_{CCP} = 2.5V, V_{EE} = 0V.*

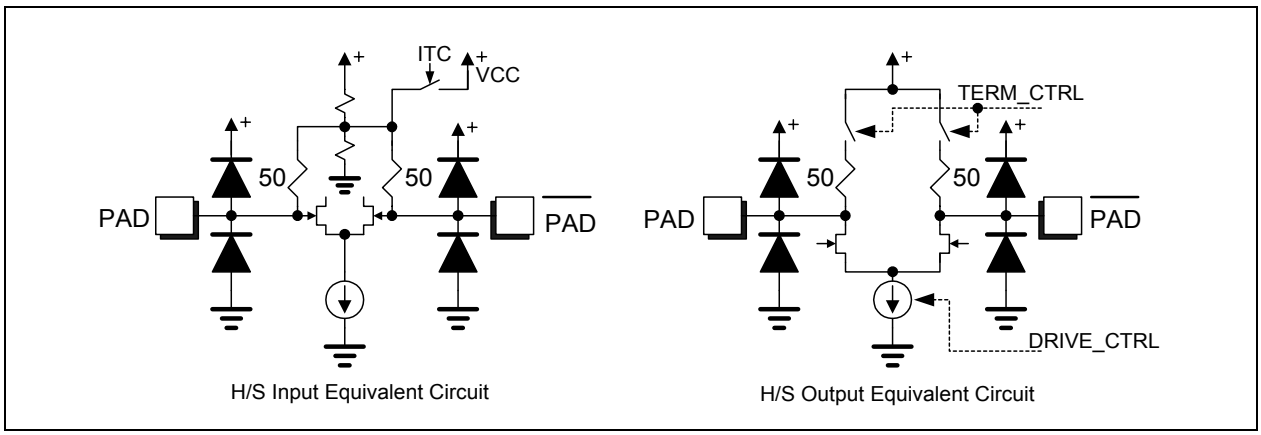


Figure 5. Equivalent Circuits

Input Terminations

The high-speed inputs of the VSC838 are internally terminated by a 100Ω impedance between true and complement inputs. Termination resistors are isolated from each other on-chip. The termination will self-bias to +2.0V (nominal) for AC-coupled applications. The ITC pin enables direct interconnection of multiple VSC838 devices. With ITC tied to V_{CC}, the center point of the 100Ω termination resistance is tied to V_{CC}, causing the terminations to act as loads for an open-drain or open-collector differential output. **See description in Table 11 on page 12 for proper connection of ITC pin.**

Table 7. Allowed Input Termination Schemes

Type	Description	Comments
1	AC-coupled input	Tie ITC LOW, 100Ω differential input termination, input self-biased
2	DC-coupled from open-drain CML	Tie ITC HIGH, termination acts as 50Ω load to V_{CC}
3	DC-coupled from back-terminated 2.5V CML	Tie ITC HIGH, termination acts as 50Ω load to V_{CC}
4	DC-coupled from back-terminated 2.5V CML	Tie ITC LOW, 100Ω differential termination (preferred over Type 3)
5	DC-coupled from back-terminated 3.3V LVPECL	Tie ITC LOW, 100Ω differential termination

Some allowed termination schemes result in additional I_{CC} current and power dissipation on-chip.

Output Terminations

The high-speed outputs of the VSC838 are internally back-terminated by 50Ω to V_{CC} when the TERM_CTRL pin is HIGH. When this pin is LOW, the output driver functions as an open-drain CML driver. Setting DRIVE_CTRL LOW (GND) saves approximately 1W under maximum power dissipation conditions. See Table 8 for allowable types of terminations and modes of operation.

Table 8. Allowed High-Speed Output Terminations and Modes of Operation

Type	Description	DRIVE_CTRL	TERM_CTRL	V_{OD}[1] (mV) typ	V_{OCM}[1] (V) typ
1	AC-coupled to 50Ω termination to any voltage	V_{CC} (HIGH)	V_{CC} (ON)	500	2.0
2	AC-coupled to 100Ω differential termination	V_{CC} (HIGH)	V_{CC} (ON)	500	2.0
3	DC-coupled, terminated in 50Ω to V_{CC} at far-end only	GND (LOW)	GND (OFF)	500	2.25
4	DC-coupled, terminated in 50Ω to V_{CC} at far-end only	V_{CC} (HIGH)	GND (OFF)	1000	2.0
5	DC-coupled, source and far-end terminated in 50Ω to V_{CC}	GND (LOW)	V_{CC} (ON)	250	2.375
6	DC-coupled, source and far-end terminated in 50Ω to V_{CC}	V_{CC} (HIGH)	V_{CC} (ON)	500	2.25
7	DC-coupled, 100Ω differential termination	GND (LOW)	V_{CC} (ON)	250	2.25
8	DC-coupled, 100Ω differential termination	V_{CC} (HIGH)	V_{CC} (ON)	500	2.0

1. Measured at output of VSC838, with V_{CC} = 2.5V.

Table 9. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{EE}	Power supply voltage		0		V	
V_{CC}, V_{CCP}	Power supply voltage	2.375	+2.5	2.625	V	
T_C	Case temperature operating range[1]	0		+85	°C	

1. Lower limit of specification is amibient temperature and upper limit is case temperature.

Table 10. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Condition
V_{CC}	Power supply voltage, potential to ground	-0.5	+4.0	V	
	Input voltage applied (LVTTL)	-0.5	V_{CC} + 1.0	V	
	Input voltage applied (ECL)	-0.5	V_{CC} + 0.5	V	
I_{OUT}	Output current	-50	+50	mA	
T_C	Case temperature under bias	-55	+125	°C	
T_S	Storage temperature	-65	+150	°C	
V_{ESD}	ESD (human body model)		500	V	

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliabiility of the device.

PACKAGE INFORMATION

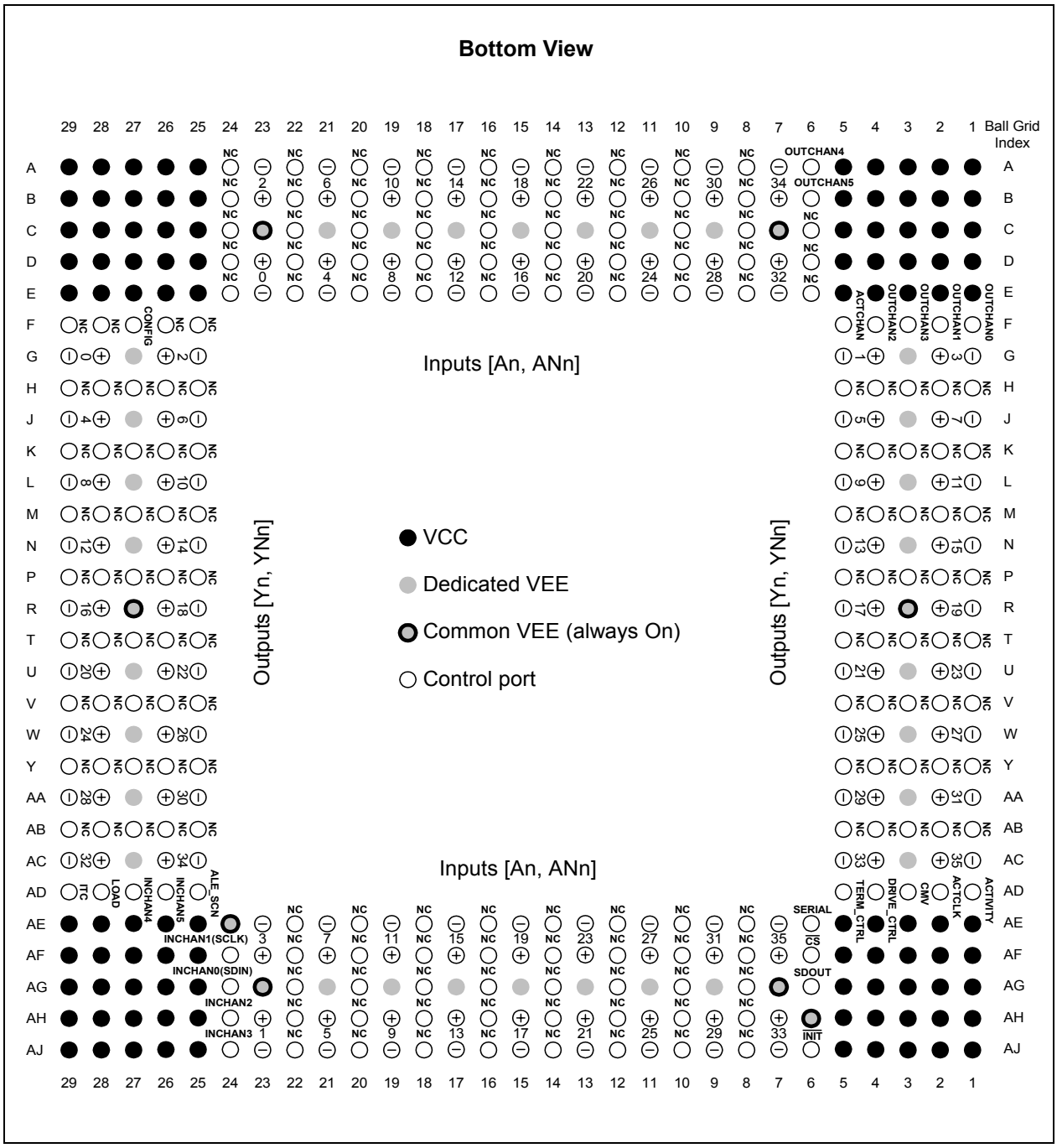


Figure 6. Pin Diagram for 480-Pin TBGA (UG)

Table 11. Pin Identification for 480-Pin TBGA (UG)

Signal	Ball Site	I/O	Level	Description
High-Speed Data Inputs				
A0, AN0	D23, E23	I	PECL	High-Speed Data Input Channel 0; True, Complement
A1, AN1	AH23, AJ23	I	PECL	High-Speed Data Input Channel 1; True, Complement
A2, AN2	B23, A23	I	PECL	High-Speed Data Input Channel 2; True, Complement
A3, AN3	AF23, AE23	I	PECL	High-Speed Data Input Channel 3; True, Complement
A4, AN4	D21, E21	I	PECL	High-Speed Data Input Channel 4; True, Complement
A5, AN5	AH21, AJ21	I	PECL	High-Speed Data Input Channel 5; True, Complement
A6, AN6	B21, A21	I	PECL	High-Speed Data Input Channel 6; True, Complement
A7, AN7	AF21, AE21	I	PECL	High-Speed Data Input Channel 7; True, Complement
A8, AN8	D19, E19	I	PECL	High-Speed Data Input Channel 8; True, Complement
A9, AN9	AH19, AJ19	I	PECL	High-Speed Data Input Channel 9; True, Complement
A10, AN10	B19, A19	I	PECL	High-Speed Data Input Channel 10; True, Complement
A11, AN11	AF19, AE19	I	PECL	High-Speed Data Input Channel 11; True, Complement
A12, AN12	D17, E17	I	PECL	High-Speed Data Input Channel 12; True, Complement
A13, AN13	AH17, AJ17	I	PECL	High-Speed Data Input Channel 13; True, Complement
A14, AN14	B17, A17	I	PECL	High-Speed Data Input Channel 14; True, Complement
A15, AN15	AF17, AE17	I	PECL	High-Speed Data Input Channel 15; True, Complement
A16, AN16	D15, E15	I	PECL	High-Speed Data Input Channel 16; True, Complement
A17, AN17	AH15, AJ15	I	PECL	High-Speed Data Input Channel 17; True, Complement
A18, AN18	B15, A15	I	PECL	High-Speed Data Input Channel 18; True, Complement
A19, AN19	AF15, AE15	I	PECL	High-Speed Data Input Channel 19; True, Complement
A20, AN20	D13, E13	I	PECL	High-Speed Data Input Channel 20; True, Complement
A21, AN21	AH13, AJ13	I	PECL	High-Speed Data Input Channel 21; True, Complement
A22, AN22	B13, A13	I	PECL	High-Speed Data Input Channel 22; True, Complement
A23, AN23	AF13, AE13	I	PECL	High-Speed Data Input Channel 23; True, Complement
A24, AN24	D11, E11	I	PECL	High-Speed Data Input Channel 24; True, Complement
A25, AN25	AH11, AJ11	I	PECL	High-Speed Data Input Channel 25; True, Complement
A26, AN26	B11, A11	I	PECL	High-Speed Data Input Channel 26; True, Complement
A27, AN27	AF11, AE11	I	PECL	High-Speed Data Input Channel 27; True, Complement
A28, AN28	D9, E9	I	PECL	High-Speed Data Input Channel 28; True, Complement
A29, AN29	AH9, AJ9	I	PECL	High-Speed Data Input Channel 29; True, Complement
A30, AN30	B9, A9	I	PECL	High-Speed Data Input Channel 30; True, Complement
A31, AN31	AF9, AE9	I	PECL	High-Speed Data Input Channel 31; True, Complement
A32, AN32	D7, E7	I	PECL	High-Speed Data Input Channel 32; True, Complement
A33, AN33	AH7, AJ7	I	PECL	High-Speed Data Input Channel 33; True, Complement
A34, AN34	B7, A7	I	PECL	High-Speed Data Input Channel 34; True, Complement
A35, AN35	AF7, AE7	I	PECL	High-Speed Data Input Channel 35; True, Complement
High-Speed Data Outputs				
Y0, YN0	G28, G29	O	CML	High-Speed Data Output Channel 0; True, Complement
Y1, YN1	G4, G5	O	CML	High-Speed Data Output Channel 1; True, Complement
Y2, YN2	G26, G25	O	CML	High-Speed Data Output Channel 2; True, Complement

Table 11. Pin Identification for 480-Pin TBGA (UG) (continued)

Signal	Ball Site	I/O	Level	Description
Y3, YN3	G2, G1	O	CML	High-Speed Data Output Channel 3; True, Complement
Y4, YN4	J28, J29	O	CML	High-Speed Data Output Channel 4; True, Complement
Y5, YN5	J4, J5	O	CML	High-Speed Data Output Channel 5; True, Complement
Y6, YN6	J26, J25	O	CML	High-Speed Data Output Channel 6; True, Complement
Y7, YN7	J2, J1	O	CML	High-Speed Data Output Channel 7; True, Complement
Y8, YN8	L28, L29	O	CML	High-Speed Data Output Channel 8; True, Complement
Y9, YN9	L4, L5	O	CML	High-Speed Data Output Channel 9; True, Complement
Y10, YN10	L26, L25	O	CML	High-Speed Data Output Channel 10; True, Complement
Y11, YN11	L2, L1	O	CML	High-Speed Data Output Channel 11; True, Complement
Y12, YN12	N28, N29	O	CML	High-Speed Data Output Channel 12; True, Complement
Y13, YN13	N4, N5	O	CML	High-Speed Data Output Channel 13; True, Complement
Y14, YN14	N26, N25	O	CML	High-Speed Data Output Channel 14; True, Complement
Y15, YN15	N2, N1	O	CML	High-Speed Data Output Channel 15; True, Complement
Y16, YN16	R28, R29	O	CML	High-Speed Data Output Channel 16; True, Complement
Y17, YN17	R4, R5	O	CML	High-Speed Data Output Channel 17; True, Complement
Y18, YN18	R26, R25	O	CML	High-Speed Data Output Channel 18; True, Complement
Y19, YN19	R2, R1	O	CML	High-Speed Data Output Channel 19; True, Complement
Y20, YN20	U28, U29	O	CML	High-Speed Data Output Channel 20; True, Complement
Y21, YN21	U4, U5	O	CML	High-Speed Data Output Channel 21; True, Complement
Y22, YN22	U26, U25	O	CML	High-Speed Data Output Channel 22; True, Complement
Y23, YN23	U2, U1	O	CML	High-Speed Data Output Channel 23; True, Complement
Y24, YN24	W28, W29	O	CML	High-Speed Data Output Channel 24; True, Complement
Y25, YN25	W4, W5	O	CML	High-Speed Data Output Channel 25; True, Complement
Y26, YN26	W26, W25	O	CML	High-Speed Data Output Channel 26; True, Complement
Y27, YN27	W2, W1	O	CML	High-Speed Data Output Channel 27; True, Complement
Y28, YN28	AA28, AA29	O	CML	High-Speed Data Output Channel 28; True, Complement
Y29, YN29	AA4 , AA5	O	CML	High-Speed Data Output Channel 29; True, Complement
Y30, YN30	AA26, AA25	O	CML	High-Speed Data Output Channel 30; True, Complement
Y31, YN31	AA2, AA1	O	CML	High-Speed Data Output Channel 31; True, Complement
Y32, YN32	AC28, AC29	O	CML	High-Speed Data Output Channel 32; True, Complement
Y33, YN33	AC4, AC5	O	CML	High-Speed Data Output Channel 33; True, Complement
Y34, YN34	AC26, AC25	O	CML	High-Speed Data Output Channel 34; True, Complement
Y35, YN35	AC2, AC1	O	CML	High-Speed Data Output Channel 35; True, Complement
Control Pins				
ACTCLK	AD2		LVTTL	Clock for Activity Monitor, <10MHz.
ACTIVITY	AD1		LVTTL	Activity Result from Previous ACTCLK Period
ALE_SCN	AD25		LVTTL	Address Latch Enable for Multiplexed Parallel Mode; Scan Enable for Serial Mode. See Figure 1 through Figure 4 for proper use.
CMV	AD3		Analog	Output Drive Current Control. Leave floating.
CONFIG	F27		LVTTL	Logic HIGH Transfers Programming to Main Program Memory
$\overline{CS}$	AF6		LVTTL	Chip Select, Active LOW. Selects between multiple devices.
DRIVE_CTRL	AD4		TTL	Output Drive Current Switch. LOW = 10mA, HIGH = 20mA.

Table 11. Pin Identification for 480-Pin TBGA (UG) (continued)

Signal	Ball Site	I/O	Level	Description
INCHAN0_SDIN	AG24		LVTTL	Input Channel, Bit 0 and Serial Data in Serial Mode
INCHAN1_SCLK	AF24		LVTTL	Input Channel, Bit 1 and Serial Clock in Serial Mode
INCHAN2	AH24		LVTTL	Input Channel, Bit 2
INCHAN3	AJ24		LVTTL	Input Channel, Bit 3
INCHAN4	AD27		LVTTL	Input Channel, Bit 4
INCHAN5	AD26		LVTTL	Input Channel, Bit 5
$\overline{\text{INIT}}$	AJ6		LVTTL	$\overline{\text{INIT}}$=0 Forces “Straight-Through” Program
ITC	AD29		Analog	Input Termination Control. GND = floating input termination, V_{CC} = CML mode. See Table 7 on page 9. **NOTE:** Do not connect to V_{CC} or V_{EE} supplies using a high value resistor. If a resistor is used to connect ITC to V_{CC} or V_{EE}, the resistor value must be < 100Ω.
LOAD	AD28		LVTTL	Rising Edge Writes Data in Parallel Mode. See Figure 4 on page 7 for Serial Mode.
OUTCHAN0	F1	O	LVTTL	Output Channel, Bit 0
OUTCHAN1	F2	O	LVTTL	Output Channel, Bit 1
ACTCHAN	F5		LVTTL	Activity Channel Enable Bit, HIGH = Enable
OUTCHAN2	F4	O	LVTTL	Output Channel, Bit 2
OUTCHAN3	F3	O	LVTTL	Output Channel, Bit 3
OUTCHAN4	A6	O	LVTTL	Output Channel, Bit 4
OUTCHAN5	B6	O	LVTTL	Output Channel, Bit 5
SDOUT	AG6		LVTTL	Serial Data Out for Serial Mode and Scan
SERIAL	AE6		LVTTL	SERIAL = 1 Sets Serial Mode
TERM_CTRL	AD5		LVTTL	Output Back-Termination Control. LOW = no back-termination; HIGH = 50Ω back-termination to V_{CC}. See Table 8 on page 10.

Table 12. Power Supplies

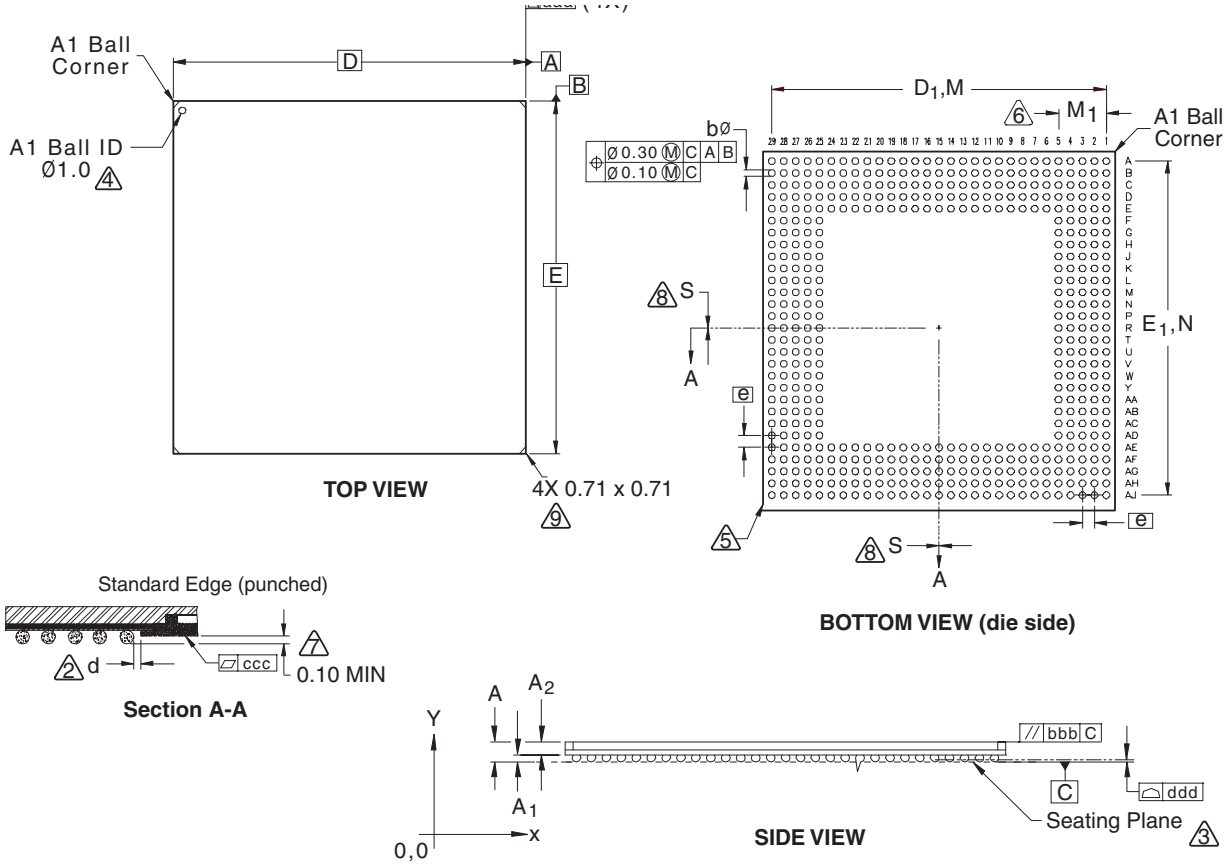
Signal	Ball Site	Description
NC	D22, AH22, B22, AF22 D20, AH20, B20, AF20 D18, AH18, B18, AF18 D16, AH16, B16, AF16 D14, AH14, B14, AF14 D12, AH12, B12, AF12 D10, AH10, B10, AF10 D8, AH8, B8, AF8 E22, AJ22, A22, AE22 E20, AJ20, A20, AE20 E18, AJ18, A18, AE18 E16, AJ16, A16, AE16 E14, AJ14, A14, AE14 E12, AJ12, A12, AE12 E10, AJ10, A10, AE10 E8, AJ8, A8, AE8	No Connect

Table 12. Power Supplies (continued)

Signal	Ball Site	Description
NC	H28, H4, H26, H2 K28, K4, K26, K2 M28, M4, M26, M2 P28, P4, P26, P2 T28, T4, T26, T2 V28, V4, V26, V2 Y28, Y4, Y26, Y2 AB28, AB4, AB26, AB2 H29, H5, H25, H1 K29, K5, K25, K1 M29, M5, M25, M1 P29, P5, P25, P1 T29, T5, T25, T1 V29, V5, V25, V1 Y29, Y5, Y25, Y1 AB29, AB5, AB25, AB1	No Connect
NC	E6, D6, C6 A24, B24, D24, E24, C24 F29, F28, F25, F26	No Connect
VEE	C23, C7, R3, AG7 AG23, R27, AH6, AE24P	Common Negative Supply
VCC	A1, A2, A3, A4, A5 B1, B2, B3, B4, B5 C1, C2, C3, C4, C5 D1, D2, D3, D4, D5 E1, E2, E3, E4, E5 A25, A26, A27, A28, A29 B25, B26, B27, B28, B29 C25, C26, C27, C28, C29 D25, D26, D27, D28, D29 E25, E26, E27, E28, E29 AE1, AE2, AE3, AE4, AE5 AF1, AF2, AF3, AF4, AF5 AG1, AG2, AG3, AG4, AG5 AH1, AH2, AH3, AH4, AH5 AJ1, AJ2, AJ3, AJ4, AJ5 AE25,AE26,AE27,AE28,AE29 AF25,AF26,AF27,AF28,AF29 AG25,AG26,AG27,AG28,AG29 AH25,AH26,AH27,AH28,AH29 AJ25,AJ26,AJ27,AJ28,AJ29	Positive Power Supply
NC	C22, C20, C18, C16, C14, C12, C10, C8, AG22, AG20, AG18, AG16, AG14, AG12, AG10, AG8, H3, K3, M3, P3, T3, V3, Y3, AB3, H27, K27, M27, P27, T27, V27, Y27, AB27	No Connect
VEEP_T1	C21	Negative Power Supply for Inputs A4/AN4, A6/AN6
VEEP_T2	C19	Negative Power Supply for Inputs A8/AN8, A10/AN10
VEEP_T3	C17	Negative Power Supply for Inputs A12/AN12, A14/AN14

Table 12. Power Supplies (continued)

Signal	Ball Site	Description
VEEP_T4	C15	Negative Power Supply for Inputs A16/AN16, A18/AN18
VEEP_T5	C13	Negative Power Supply for Inputs A20/AN20, A22/AN22
VEEP_T6	C11	Negative Power Supply for Inputs A24/AN24, A26/AN26
VEEP_T7	C9	Negative Power Supply for Inputs A28/AN28, A30/AN30
VEEP_B1	AG21	Negative Power Supply for Inputs A5/AN5, A7/AN7
VEEP_B2	AG19	Negative Power Supply for Inputs A9/AN9, A11/AN11
VEEP_B3	AG17	Negative Power Supply for Inputs A13/AN13, A15/AN15
VEEP_B4	AG15	Negative Power Supply for Inputs A17/AN17, A19/AN19
VEEP_B5	AG13	Negative Power Supply for Inputs A21/AN21, A23/AN23
VEEP_B6	AG11	Negative Power Supply for Inputs A25/AN25, A27/AN27
VEEP_B7	AG9	Negative Power Supply for Inputs A29/AN29, A31/AN31
VEEP_L0	G3	Negative Power Supply for Outputs Y1/YN1, Y3/YN3
VEEP_L1	J3	Negative Power Supply for Outputs Y5/YN5, Y7/YN7
VEEP_L2	L3	Negative Power Supply for Outputs Y9/YN9, Y11/YN11
VEEP_L3	N3	Negative Power Supply for Outputs Y13/YN13, Y15/YN15
VEEP_L4	U3	Negative Power Supply for Outputs Y21/YN21, Y23/YN23
VEEP_L5	W3	Negative Power Supply for Outputs Y25/YN25, Y27/YN27
VEEP_L6	AA3	Negative Power Supply for Outputs Y29/YN29, Y31/YN31
VEEP_L7	AC3	Negative Power Supply for Outputs Y33/YN33, Y35/YN35
VEEP_R0	G27	Negative Power Supply for Outputs Y0/YN0, Y2/YN2
VEEP_R1	J27	Negative Power Supply for Outputs Y4/YN4, Y6/YN6
VEEP_R2	L27	Negative Power Supply for Outputs Y8/YN8, Y10/YN10
VEEP_R3	N27	Negative Power Supply for Outputs Y12/YN12, Y14/YN14
VEEP_R4	U27	Negative Power Supply for Outputs Y20/YN20, Y22/YN22
VEEP_R5	W27	Negative Power Supply for Outputs Y24/YN24, Y26/YN26
VEEP_R6	AA27	Negative Power Supply for Outputs Y28/YN28, Y30/YN30
VEEP_R7	AC27	Negative Power Supply for Outputs Y32/YN32, Y34/YN34



SYMBOL	MIN	TYP	MAX	NOTE
A	1.85	1.8	1.25	Overall thickness
A_1	0.60	0.65	0.70	Ball height
A_2	1.05	1.15	1.25	Body thickness
D	37.30	37.50	37.70	Body size
D_1	35.46	35.56	35.66	Ball footprint
E	37.30	37.5	37.70	Body size
E_1		35.56		Ball footprint
M, N		29 x 29		Ball matrix
M1 6		5		Number of rows deep
b	0.65	0.75	0.85	Ball diameter
d	0.25			Min distance encap to balls
e		1.27		Ball pitch
aaa			0.20	Package body profile
bbb			0.25	Parallel
ccc			0.20	Encap flatness over die
ddd			0.20	Coplanarity
S		0.00		Solder ball placement

All dimensions are in millimeters unless otherwise noted.

NOTES:

1. All dimensions and tolerances conform to ASME Y14.5M-1994.
2. Dimension “d” is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
4. Pin A1 I.D. mark, half etched.
5. Shape at corner:

6. Number of rows in from edge to center.
7. Seating plane clearance: maximum height of encapsulant above seating plane.
8. "S" is measured with respect to A and B and defines the position of the center solder ball in the outer row. When there is an odd number of solder balls in the outer row, "S" = 0.000; when there is an even bumber of solder balls in the outer row, the value "S" = e/2. "S" may be either 0.000 or e/2 for each variation.
9. Heat spreader corner profile, square or chamfered, is determined by heat spreader strip configuration.

Figure 7. Package Drawing for 480-Pin TBGA (UG)

Thermal Considerations

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 13. Thermal Resistances

Part Number	θ_{JC}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	100	200
VSC838UG	0.15	11	10.1	8.6

Moisture Sensitivity Level

This device is rated moisture sensitivity level 3 or better as specified in JEDEC standard IPC/JEDEC J-STD-020B. For more information, see the JEDEC standard.

ORDERING INFORMATION

VSC838 3.2Gb/s 36x36 Crosspoint Switch

Part Number	Description
VSC838UG	480-Pin TBGA, 37.5mm x 37.5mm Body Temperature Range: 0°C ambient to +85°C case

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