OKI Semiconductor

MSM7580

5V ADPCM Transcoder

DESCRIPTION

The MSM7580 is a single-rail, low-voltage, two-channel ADPCM transcoder which performs bi-directional digital conversion from PCM (Pulse Code Modulation) serial voice data to ADPCM (Adaptive Differential Pulse Code Modulation) serial data. Serial data rates are 64 Kbps to 2048 Kbps for PCM serial voice data and 32 Kbps to 2048 Kbps for ADPCM serial data. The MSM7580 offers full-duplex operation in both PCM or ADPCM data directions, reducing the data rate required to transmit and synchronize voice signals. Coder/decoder and channel synchronous operations implement the two most common companding schemes accepted worldwide, both μ-law and A-law.

As the telecommunications industry quickly expands with enhanced applications in next generation digital cordless telephone base stations connected to digital lines or digital PBX, OKI's MSM7580 keeps power consumption to a minimum during operation and power-down, saving valuable battery life, while minimizing overall noise. By integrating discrete components on-chip, OKI reduces systems costs while saving board space.

The MSM7580 ADPCM transcoder was designed using OKI's high-quality CMOS process, providing superior low-power performance. Designers will find our space-saving 28-pin SOP (GS-VK) package perfect for a variety of applications.

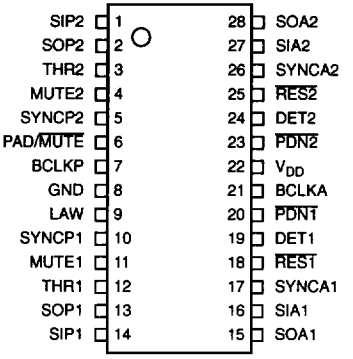
FEATURES

- Single 5V power supply eliminates second supply requirement
- Low supply voltage/current consumption: +5V ±10%, 2.5 mA/channel
- Two-channel, full-duplex transcoder operation offers one-chip solutions
- Both companding methods, μ-law or A-law, simplify designs
- Coder/decoder and synchronous channel operation ease timing considerations
- Serial ADPCM data rates of 32 Kbps to 2048 Kbps
- Serial PCM data rate of 64 Kbps to 2048 Kbps
- Hard reset for each channel simplifies software support (CCITT G.721 optional reset)
- ADPCM system conforms to CCITT recommendations G.721 (32 Kbps)
- Master clock unnecessary
- Power-down mode for each channel minimizes system consumption
- Decoder (ADPCM → PCM) mute and PAD mode for each channel reduces system costs
- ADPCM data-through mode increases throughput
- Time slot conversion meets enhanced design requirements
- ADPCM data input "0000" code detection pin minimizes external circuitry for each channel
- 430 mil 28-pin SOP package available

MSM7580 PACKAGING

Part Number	Package Type	Pins	Package Number
MSM7580GS	SOP	28-pin	SOP28-P-430-K

PIN CONNECTIONS



28-Pin SOP

Pin	Description	Pin	Description
SIP2	PCM serial data input, channel 2	SOA2	ADPCM serial output, channel 2
SOP2	PCM serial data output, channel 2	SIA2	ADPCM serial input, channel 2
THR2	Mode settings data through control, channel 2	SYNCA2	ADPCM synchronous signal input, channel 2
MUTE2	MUTE mode, channel 2	$\overline{RES2}$	Reset signal input, channel 2
SYNCP2	Synchronous signal input, channel 2	DET2	ADPCM input data pattern detect, channel 2
PAD/$\overline{MUTE}$	PAD/MUTE mode select	$\overline{PDN2}$	Power-down mode, channel 2
BCLKP	PCM bit clock input	V_{DD}	+5V power supply
GND	Ground pin	BCLKA	ADPCM bit clock input
LAW	Encoding law select	$\overline{PDN1}$	Power-down mode, channel 1
SYNCP1	Synchronous signal input, channel 1	DET1	ADPCM input data pattern detect, channel 1
MUTE1	MUTE mode, channel 1	$\overline{RES1}$	Reset signal input, channel 1
THR1	Mode settings data through control, channel 1	SYNCA1	ADPCM synchronous signal input, channel 1
SOP1	PCM serial data output, channel 1	SIA1	ADPCM serial input, channel 1
SIP1	PCM serial data input, channel 1	SOA1	ADPCM serial output, channel 1

CIRCUIT CONFIGURATION

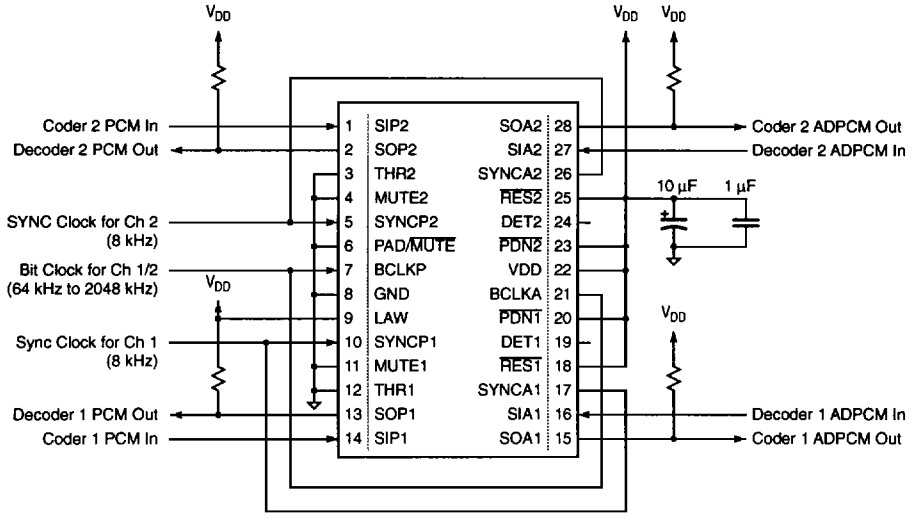


Figure 1. Example Circuit Wiring

BLOCK DIAGRAM

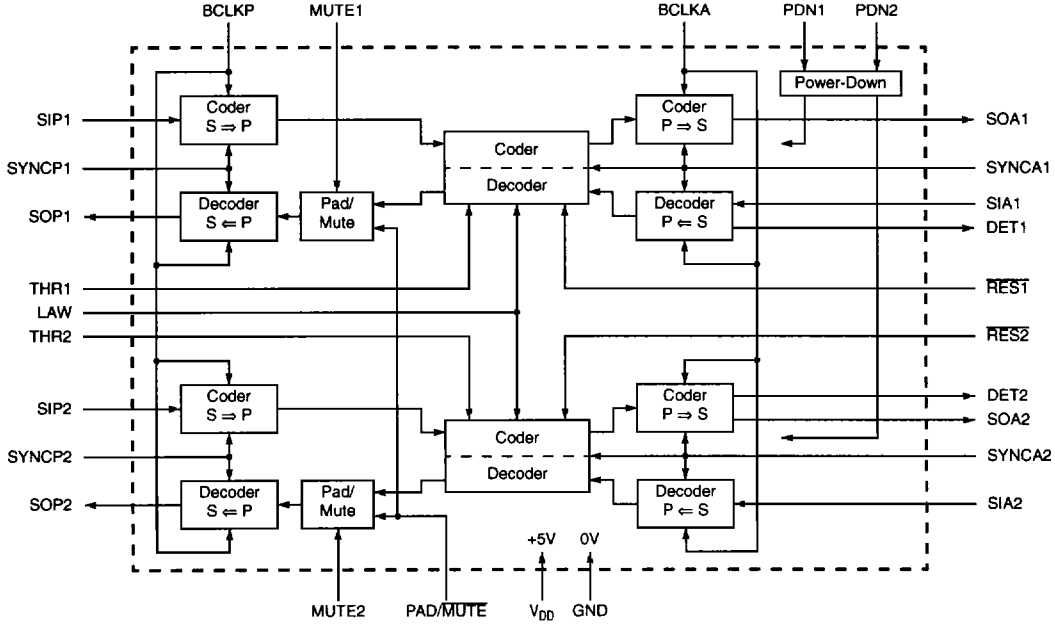


Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin Name	Description
GND	Ground pin
SIP1, SOP1	PCM serial data input and output pins for channel 1 side. SOP1 (output) is an open drain pin, and enters high impedance status after 8-bit serial data is output.
SIP2, SOP2	PCM serial data input and output pins for channel 2 side. SOP2 (output) is an open drain pin, and enters high impedance status after 8-bit serial data is output.
PAD/$\overline{\text{MUTE}}$	PAD mode / MUTE mode select pin. Digital "1" selects PAD mode, and digital "0" selects MUTE mode.
THR1, THR2	Control pins for the through mode settings. Digital "1" selects data through mode. In this mode, when 8-bits of serial data is input to ADPCM serial input pins SIA1 and SIA2 at channels 1 and 2, that 8-bit serial data is then output to PCM output pins SOP1 and SOP2 as is (becomes high impedance status after 8-bits are output). 8-bit data input to the PCM serial pins SIP1 and SIP2 is then output to ADPCM output pins SOA1 and SOA2 as is (becomes high impedance status after 8-bit output). THR1 is for channel 1, and THR2 is for channel 2. Note: Since ADPCM side and PCM side have different synchronous signal input pins, it is possible to exchange the data input/output time slots.
MUTE1, MUTE2	The MUTE mode is set by the PAD/$\overline{\text{MUTE}}$ pin. When these pins (MUTE1, MUTE2) are both set to digital "1", the PCM output of channel 1 (SOP1) and channel 2 (SOP2) is set to a pattern when there is no talking (idle pattern), regardless of the ADPCM input. In the PAD mode, the ADPCM output has a 12 dB loss. In normal operation these pins are set to "0". This function is invalid in the data through mode.
SYNCP1, SYNCP2	Synchronous signal input pins that specify the PCM data input/output timing of channel 1 (SIP1, SOP1) and channel 2 (SIP2, SOP2). There are also other synchronous signal pins, SYNCA1 (for channel 1) and SYNCA2 (for channel 2) that specify the ADPCM data input/output timing. This means that a PCM and ADPCM data interface can be executed using different timings.
BCLKP	Bit clock input pin that specifies the data speed of the PCM data interface. BCLKP is commonly used for channels 1 and 2. There is also BCLKA that specifies the data speed of the ADPCM data interface. This means that a PCM and ADPCM data interface can be specified to different data speeds.
LAW	Selects the recommended rule (A-law/μ-law) of the PCM data. Digital "1" selects A-law, "0" selects μ-law.
$\overline{\text{PDN1}}$, $\overline{\text{PDN2}}$	Channel 1 ($\overline{\text{PDN1}}$) and channel 2 ($\overline{\text{PDN2}}$) can be set to power-down mode independently. Digital "0" selects power-down mode.
SIA1, SOA1	ADPCM serial data input (SIA1) and output (SOA1) pins for channel 1. SOA1 is an open drain pin, and normally enters high impedance status after 4-bits of data is output. In the through mode, SOA1 enters high impedance status after 8-bits of data is output.
SIA2, SOA2	ADPCM serial data input (SIA2) and output (SOA2) pins for channel 2. SOA2 is an open drain pin, and normally enters high impedance status after 4-bits of data is output. In through mode, SOA2 enters high impedance status after 8-bits of data is output.
SYNCA1, SYNCA2	Synchronizing signal input pins that specify ADPCM data input/output timing. SYNCA1 is for channel 1 (SIA1, SOA1), and SYNCA2 is for channel 2 (SIA2, SOA2). Because of this function, the ADPCM data interface can be executed under different timings from the PCM data interface.
DET1, DET2	These pins output digital "1" when "0000" is input in serial to the ADPCM data input of channel 1 (SIA1) and channel 2 (SIA2) respectively. For output timing, digital "1" is output at the rise of the clock next to bit clock (BCLKA) when LSB (4th data) is fetched. Digital "1" is held until the rise of the same clock in the next frame. If "0000" is input in the next frame, digital "1" is continuously output. These pins are invalid when THR1 and THR2 pins are digital "1" (data through mode).
$\overline{\text{RES1}}$, $\overline{\text{RES2}}$	Algorithm reset signal input pins of channel 1 ($\overline{\text{RES1}}$) and channel 2 ($\overline{\text{RES2}}$). When digital "0" is selected, the transcoder is initialized. This is an optional reset specified by CCITT G.721.
BCLKA	Bit clock input pin that specifies the speed of the ADPCM data interface, commonly used for channels 1 and 2. Because of this function, the ADPCM data interface can be specified under different speeds from the PCM data interface.
V_{DD}	+5V ±10% power supply

FUNCTIONAL DESCRIPTION

The MSM7580 transcoder signal conversion process comes in three steps, independent of data direction. The input signal is first converted from serial data stream to a parallel format, allowing efficient and accurate operation of the coder/decoder circuitry. Since PCM and ADPCM data can be executed at different timing intervals, a synchronous I/O pin is available to ensure stability. Once converted, the bit stream is encoded to the selected companding scheme and modulation algorithm consistent with CCITT recommendation G.721.

Before a serial bit stream is output to the system, a final conversion from parallel to serial occurs with the speed of the interface under the control of the bit clock (BCLKX). The I/O enters a high impedance state once either 4-bits (ADPCM) or 8-bits (PCM) are transferred to minimize power consumption. Through data modes, implementing no change to the data occurs via THRX.

Additional functionality was incorporated to ease overall system design, including power-down modes for each channel, decoder mute mode, and time slot conversion. By integrating discrete components on-chip, OKI reduces system costs while saving board space.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rated Value	Unit
Power supply voltage	V_{DD}	0 ~ 7	V
Digital input voltage	V_{DIN}	-0.3 ~ V_{DD}+ 0.3	
Operating temperature	T_{OP}	-30 ~ +80	°C
Storage temperature	T_{stg}	-55 ~ +150	

Recommended Operating Conditions

Parameter	Symbol	Condition	Rated Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{DD}		+4.5	–	+5.5	V
Operating temperature	T_a		-30	–	+80	°C
Digital input high voltage	V_{IH}	All input pins	+2.2	–	V_{DD}	V
Digital input low voltage	V_{IL}	All input pins	0	–	+0.6	
Bit clock frequency	FB_{CLKA}	BCLKA	32	–	2048	kHz
	FB_{CLKP}	BCLKP	64	–	2048	
Synchronizing pulse frequency	F_{SYNC}	SYNCP12, SYNCP2, SYNCA12, SYNCA2	–	8.0	–	kHz
Bit clock duty cycle	D_C	BCLKA, BCLKP	30	50	70	%
Digital input rise time	T_{IR}	All input pins	–	–	50	ns
Digital input fall time	T_{IF}					
Coder synchronous timing	T_{XS}	BCLKA, BCLKP → SYNCP (refer to *Figure 1*)	100	–	–	ns
	T_{SX}	SYNCP → BCLKA, BCLKP (refer to *Figure 1*)				
Decoder synchronous timing	T_{RS}	BCLKA, BCLKDP → SYNCA (refer to *Figure 1*)	100	–	–	ns
	T_{SR}	SYNCA → BCLKA, BCLKP (refer to *Figure 1*)				
Synchronizing signal width	T_{WS}	SYNCP12, SYNCP2, SYNCA12, SYNCA2	1BCLK	–	100	µs
Setup time	T_{DS}	Refer to *Figure 3* and *Figure 4*	100	–	–	ns
Hold time	T_{DH}					
Digital output load	R_{DL}	SOP1, SOP2, SOA1, SOA2 (pull-up resistor)	500	–	–	Ω
	C_{DL}	SOP1, SOP2, SOA1, SOA2, DET1, DET2	–	–	100	pF

DC Characteristics (V_{DD} = +4.5 ~ +5.5V, T_a = -30 ~ +80 °C)

Parameter	Symbol	Condition	Rated Value			Unit
			Min	Type	Max	
Power supply current	I_{DD1}	When both channels are operating	–	5	10	mA
	I_{DD2}	When both channels are in power-down	–	0.1	0.2	
Input high level voltage	V_{IH}		2.0	–	V_{DD}	V
Input low level voltage	V_{IL}		0.0	–	0.6	
Input high leakage current	I_{IH}	$V_I = V_{DD}$	–	–	2.0	µA
Input low leakage current	I_{IL}	V_I = 0V	–	–	0.5	
Output high voltage	V_{OH}	DET1, DET2, I_{OH} = -0.4 mA	2.8	–	V_{DD}	V
Output low voltage	V_{OL1}	1LSTTL, pull-up = 500 Ω	0.0	0.2	0.4	V
	V_{OL2}	DET1, DET2, I_{OL} =1.6 mA	0.0	0.2	0.4	
Output leakage current	I_{OL}	SOP1, SOP2, SOA1, SOA2	–	–	10	µA
Input capacitance	C_{IN}		–	5	–	pF

AC Characteristics (V_{DD} = +4.5 ~ +5.5V, T_a = -30 ~ +80 °C)

Parameter	Symbol	Condition	Rated Value			Unit
			Min	Type	Max	
Digital output delay time	t_{SDX}	C_L = 1LSTTL + 100 pF Pull-up = 500 Ω (refer to *Figure 3* and *Figure 4*)	50	–	200	ns
	t_{SDR}					
	t_{XD1}/ t_{RD1}					
	t_{XD2}/ t_{RD2}					
	t_{XD3}/ t_{RD3}					
	t_{DD1}					
	t_{DD2}					

TIMING WAVEFORMS

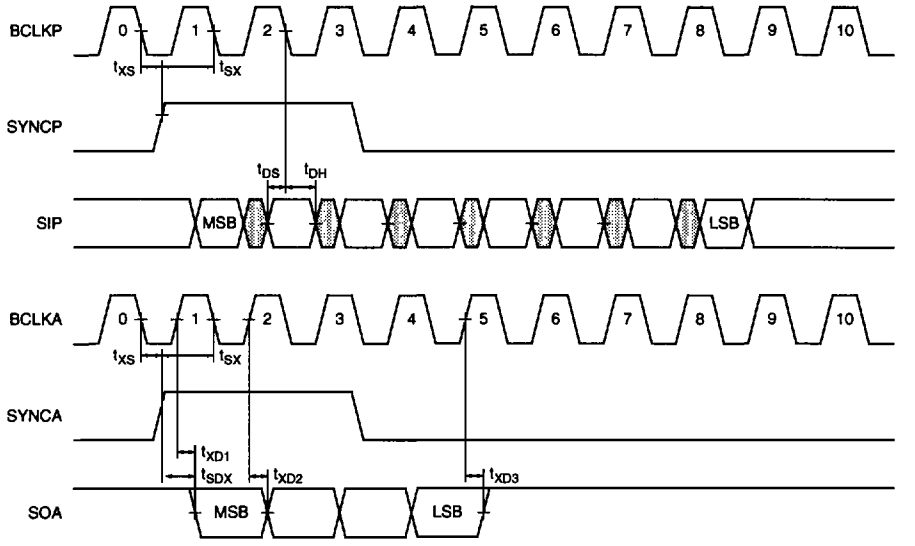


Figure 3. Coder Data Transfer Timing

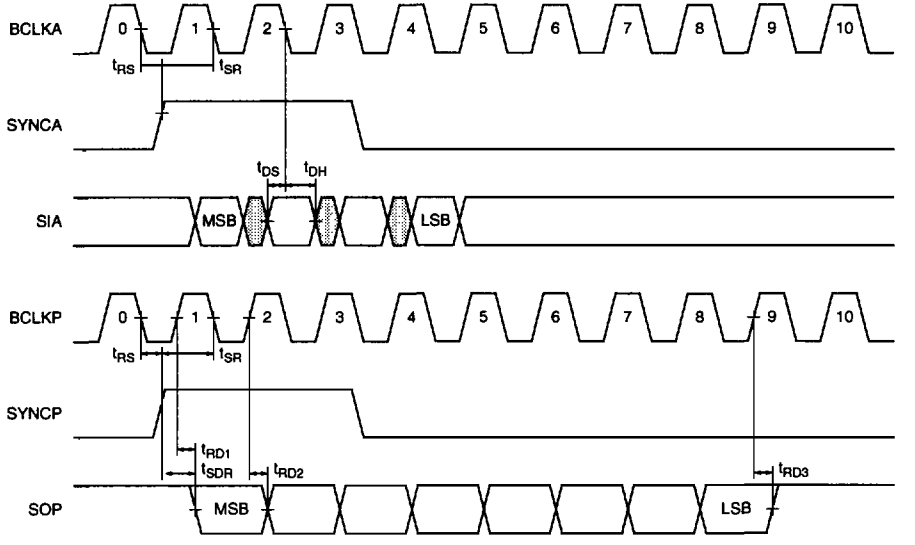


Figure 4. Decoder Data Transfer Timing

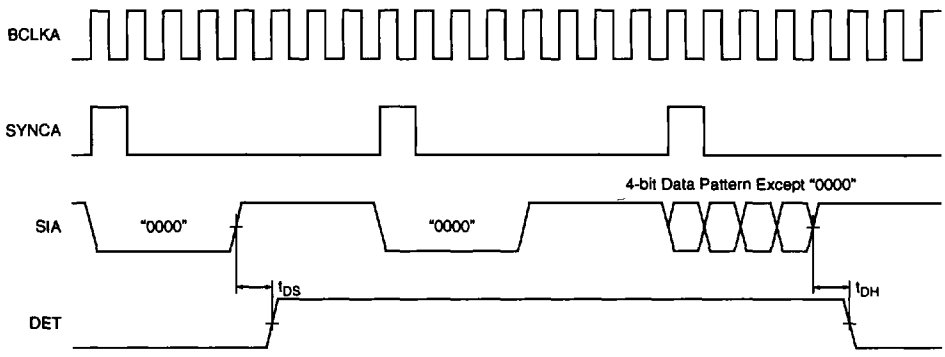


Figure 5. DET ("0000") Output Timing