HARRIS

82C89/883

T-52-33-03

June 1989

CMOS Bus Arbiter

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Pin Compatible with Bipolar 8289
- Compatible with 5MHz and 8MHz 80C86 and 80C88
- Provides Multi-Master System Bus Control and Arbitration
- Provides Simple Interface with 82C88/8288 Bus Controller
- Synchronizes 80C86/8086, 80C88/8088 Processors with Multi-Master Bus
- Bipolar Drive Capability
- Four Operating Modes for Flexible System Configuration
- Low Power Operation
  - ICCSB ..... 10µA Maximum
  - ICCOP ..... 1mA/MHz Maximum
- Military Operating Temperature Range ..... -55°C to +125°C

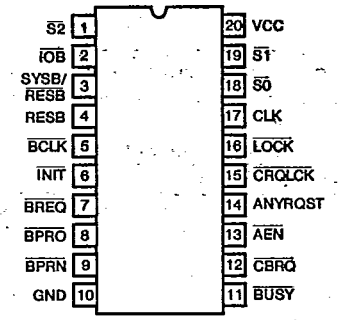
Description

The Harris 82C89/883 Bus Aribiter is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). This circuit, along with the 82C88 bus controller, provides full bus arbitration and control for multi-processor systems. The 82C89/883 is typically used in medium to large 80C86 or 80C88 systems where access to the bus by several processors must be coordinated. The 82C89/883 also provides high output current and capacitive drive to eliminate the need for additional bus buffering.

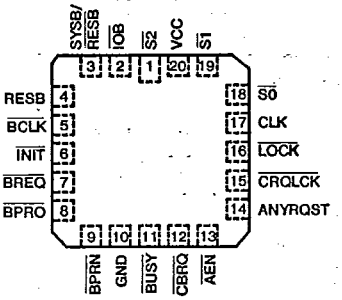
Static CMOS circuit design insures low operating power. The advanced Harris SAJI CMOS process results in performance equal to or greater than existing equivalent products at a significant power savings.

Pinouts

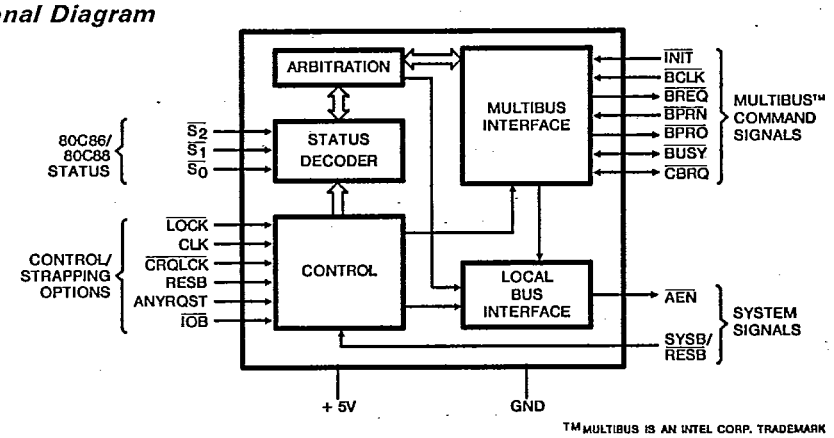
82C89/883 (CERAMIC DIP)
TOP VIEW



82C89/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



TM MULTIBUS IS AN INTEL CORP. TRADEMARK

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
VCC	20		VCC: The +5V Power supply pin. A 0.1µF capacitor between pins 10 and 20 is recommened for decoupling.
GND	10		GROUND.
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	1, 18–19	I	STATUS INPUT PINS: The status input pins from an 80C86, 80C88 or 8089 processor. The 82C89/883 decodes these pins to initiate bus request and surrender actions. (See Table A in Design Information.)
CLK	17	I	CLOCK: From the 82C84A or 82C85 clock chip and serves to establish when bus arbiter actions are initiated.
$\overline{LOCK}$	16	I	LOCK: A processor generated signal which when activated (low) prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter, regardless of its priority.
$\overline{CRQLCK}$	15	I	COMMON REQUEST LOCK: An active low signal which prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter requesting the bus through the $\overline{CBRQ}$ input pin.
RESB	4	I	RESIDENT BUS: A strapping option to configure the arbiter to operate in systems having both a multi-master system bus and a Resident Bus. Strapped high, the multi-master system bus is requested or surrendered as a function of the SYSB/$\overline{RESB}$ input pin. Strapped low, the SYSB/$\overline{RESB}$ input is ignored.
ANYRQST	14	I	ANY REQUEST: A strapping option which permits the multi-master system bus to be surrendered to a lower priority arbiter as if it were an arbiter of higher priority (i.e., when a lower priority arbiter requests the use of the multi-master system bus, the bus is surrendered as soon as it is possible). When ANYRQST is strapped low, the bus is surrendered according to Table A in Design Information. If ANYRQST is strapped high and $\overline{CBRQ}$ is activated, the bus is surrendered at the end of the present bus cycle. Strapping $\overline{CBRQ}$ low and ANYRQST high forces the 82C89/883 arbiter to surrender the multi-master system bus after each transfer cycle. Note that when surrender occurs $\overline{BREQ}$ is driven false (high).
$\overline{IOB}$	2	I	IO BUS: A strapping option which configures the 82C89/883 Arbiter to operate in systems having both an IO Bus (Peripheral Bus) and a multi-master system bus. The arbiter requests and surrenders the use of the multi-master system bus as a function of the status line, $\overline{S2}$. The multi-master system bus is permitted to be surrendered while the processor is performing IO commands and is requested whenever the processor performs a memory command. Interrupt cycles are assumed as coming from the peripheral bus and are treated as an IO command.
$\overline{AEN}$	13	O	ADDRESS ENABLE: The output of the 82C89/883 Arbiter to the processor's address latches, to the 82C88 Bus Controller and 82C84A or 82C85 Clock Generator. $\overline{AEN}$ serves to instruct the Bus Controller and address latches when to three-state their output drivers.
$\overline{INIT}$	6	I	INITIALIZE: An active low multi-master system bus input signal used to reset all the bus arbiters on the multi-master system bus. After initialization, no arbiters have the use of the multi-master system bus.
SYSB/ $\overline{RESB}$	3	I	SYSTEM BUS/RESIDENT BUS: An input signal when the arbiter is configured in the System/Resident Mode ($\overline{RESB}$ is strapped high) which determines when the multi-master system bus is requested and multi-master system bus surrendering is permitted. The signal is intended to originate from a form of address-mapping circuitry, such as a decoder or PROM attached to the resident address bus. Signal transitions and glitches are permitted on this pin from ϕ1 of T4 to ϕ1 of T2 of the processor cycle. During the period from ϕ1 of T2 to ϕ1 of T4, only clean transitions are permitted on this pin (no glitches). If a glitch occurs, the arbiter may capture or miss it, and the multi-master system bus may be requested or surrendered, depending upon the state of the glitch. The arbiter requests the multi-master system bus in the System/Resident Mode when the state of the SYSB/$\overline{RESB}$ pin is high and permits the bus to be surrendered when this pin is low.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{CBRQ}$	12	I/O	COMMON BUS REQUEST: An input signal which instructs the arbiter if there are any other arbiters of lower priority requesting the use of the multi-master system bus. The $\overline{CBRQ}$ pins (open-drain output) of all the 82C89/883 Bus Arbiters which surrender to the multi-master system bus upon request are connected together. The Bus Arbiter running the current transfer cycle will not itself pull the $\overline{CBRQ}$ line low. Any other arbiter connected to the $\overline{CBRQ}$ line can request the multi-master system bus. The arbiter presently running the current transfer cycle drops its $\overline{BREQ}$ signal and surrenders the bus whenever the proper surrender conditions exist. Strapping $\overline{CBRQ}$ low and ANYRQST high allows the multi-master system bus to be surrendered after each transfer cycle. See the pin definition of ANYRQST.
$\overline{BCLK}$	5	I	BUS CLOCK: The multi-master system bus clock to which all multi-master system bus interface signals are synchronized.
$\overline{BREQ}$	7	O	BUS REQUEST: An active low output signal in the Parallel Priority Resolving Scheme which the arbiter activates to request the use of the multi-master system bus.
$\overline{BPRN}$	9	I	BUS PRIORITY IN: The active low signal returned to the arbiter to instruct it that it may acquire the multi-master system bus on the next falling edge of $\overline{BCLK}$. $\overline{BPRN}$ active indicates to the arbiter that it is the highest priority requesting arbiter presently on the bus. The loss of $\overline{BPRN}$ instructs the arbiter that it has lost priority to a higher priority arbiter.
$\overline{BPRO}$	8	O	BUS PRIORITY OUT: An active low output signal used in the serial priority resolving scheme where $\overline{BPRO}$ is daisy-chained to $\overline{BPRN}$ of the next lower priority arbiter.
$\overline{BUSY}$	11	I/O	BUSY: An active low open-drain multi-master system bus interface signal used to instruct all the arbiters on the bus when the multi-master system bus is available. When the multi-master system bus is available the highest requesting arbiter (determined by $\overline{BPRN}$) seizes the bus and pulls $\overline{BUSY}$ low to keep other arbiters off of the bus. When the arbiter is done with the bus, it releases the $\overline{BUSY}$ signal, permitting it to go high and thereby allowing another arbiter to acquire the multi-master system bus.

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	80°C/W	21°C/W
Ceramic LCC Package	76°C/W	19°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 620mW
Ceramic LCC Package 664mW
Gate Count ..... 200 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... +4.5V to +5.5V

TABLE 1. 82C89/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical "1" Input Voltage	VIH	VCC = 5.5V, Note 2	1, 2, 3	$-55°C \le T_A \le +125°C$	2.2	-	V
Logical "0" Input Voltage	VIL	Note 2	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.8	V
CLK Logical "1" Input Voltage	VIHC	VCC = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	70% VCC	-	V
CLK Logical "0" Input Voltage	VILC		1, 2, 3	$-55°C \le T_A \le +125°C$	-	20% VCC	V
Output HIGH Voltage, $\overline{BUSY}$, $\overline{CBRQ}$	VOH1	Open Drain, Note 3 DIP Pins 11, 12	1, 2, 3	$-55°C \le T_A \le +125°C$	-	-	V
Output HIGH Voltage, All Other Outputs	VOH2	IOH = -2.5mA, Note 3 IOH = -100µA, Note 3	1, 2, 3	$-55°C \le T_A \le +125°C$	3.0 VCC-0.4	- -	V V
Output LOW Voltage, $\overline{BUSY}$, $\overline{CBRQ}$	VOL1	IOL = 20mA, Note 3, DIP Pins 11, 12	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.45	V
Output LOW Voltage, $\overline{AEN}$	VOL2	IOL = 16mA, Note 3, DIP Pin 13	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.45	V
Output LOW Voltage, $\overline{BPRO}$, $\overline{BREQ}$	VOL3	IOL = 8mA, Note 3, DIP Pins 7, 8	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.45	V
Input Leakage Current	II	VCC = 5.5V, VIN = GND or VCC DIP Pins 1-6, 9, 14-19	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Output Leakage Current	IO	VCC = 5.5V, VOUT = GND or VCC DIP Pins 11, 12	1, 2, 3	$-55°C \le T_A \le +125°C$	-10	+10	µA
Standby Power Supply Current	ICCSB	VCC = 5.5V, VIN = GND or VCC Outputs Open	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	µA
Operating Power Supply Current	ICCOP	VCC = 5.5V, f = 1MHz, Outputs Open, Note 4	1, 2, 3	$-55°C \le T_A \le +125°C$	-	1	mA/MHz

NOTES: 1. VCC = 4.5V unless otherwise specified. All voltage referenced to device GND.
2. Does not apply to $\overline{IOB}$, RESB, or ANYRQST. These are strap options and should be held to VCC or GND.
3. Interchanging of force and sense conditions is permitted.
4. Maximum current defined by CLK or $\overline{BCLK}$, whichever has the highest operating frequency.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. 82C89/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CLK Cycle Time	(1)TCLCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	125	-	ns
CLK Low Time	(2)TCLCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	55	-	ns
CLK High Time	(3)TCHCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	35	-	ns
Status Active Setup Time	(4)TSVCH	Note 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	65	-	ns
Status Inactive Setup Time	(5)TSHCL	Note 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Status Inactive Hold Time	(6)THVCH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Status Active Hold Time	(7)THVCL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
$\overline{BUSY}$** Setup to $\overline{BCLK}$	(8)TBYSBL	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
$\overline{CBRQ}$** Setup to $\overline{BCLK}$	(9)TCBSBL	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
$\overline{BCLK}$ Cycle Time	(10)TBLBL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
$\overline{BCLK}$ High Time	(11)TBHCL	Note 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	ns
$\overline{LOCK}$ Inactive Hold Time	(12)TCLLL1		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
$\overline{LOCK}$ Active Setup Time	(13)TCLLL2		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
$\overline{BPRN}$** to $\overline{BCLK}$ Setup Time	(14)TPNBL	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
SYSB/$\overline{RESB}$ Setup Time	(15)TCLSR1		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
SYSB/$\overline{RESB}$ Hold Time	(16)TCLSR2		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	ns
Initialization Pulse Width	(17)TIVIH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	675	-	ns
$\overline{BCLK}$ to $\overline{BREQ}$** Delay Time	(18)TBLBRL	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	35	ns
$\overline{BCLK}$ to $\overline{BPRO}$**	(19)TBLPOH	Notes 3, 4	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	35	ns
$\overline{BPRN}$** to $\overline{BPRO}$** Delay Time	(20)TPNPO	Notes 3, 4	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	22	ns
$\overline{BCLK}$ to $\overline{BUSY}$ Low	(21)TBLBYL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	60	ns
CLK to $\overline{AEN}$ High	(23)TCLAEH		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	65	ns
$\overline{BCLK}$ to $\overline{AEN}$ Low	(24)TBLAEL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
$\overline{BCLK}$ to $\overline{CBRQ}$ Low	(25)TBLCBL		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	60	ns
Output Rise Time	(27)TOLOH	From 0.8V to 2.0V Except $\overline{BUSY}$ and $\overline{CBRQ}$	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	20	ns
Output Fall Time	(28)TOHOL	From 2.0V to 0.8V Except $\overline{BUSY}$ and $\overline{CBRQ}$	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	12	ns

NOTES:
1. VCC = 4.5V and 5.5V unless otherwise specified. Tested as follows: f = 1MHz, VIH = 2.6V, VIL = 0.4V, VIHC = VCC - 0.4V, VILC = 0.4V. Load per appropriate A.C. test circuit, VOH $\geq$ 1.5V and VOL $\leq$ 1.5V. Input rise and fall times are driven at 1ns/V.
2. Reference Table 3 for maximum limit.
3. Both transitions of the signal apply to parameters with asterisks (**).
4. $\overline{BCLK}$ generates $\overline{BPRO}$ from arbiter #1 wherein subsequent $\overline{BPRO}$ changes lower in the chain are generated from $\overline{BPRO}$ of the next higher priority arbiter.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. 82C89/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	f = 1MHz, all measurements are reference to device GND, VCC = Open	1	$T_A = +25^oC$	-	10	pF
Output Capacitance	COUT		1	$T_A = +25^oC$	-	10	pF
I/O Capacitance	CIO		1	$T_A = +25^oC$	-	15	pF
Status Active Setup Time	(4)TSVCH		1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	TCLCL -10	ns
Status Inactive Setup Time	(5)TSHCL		1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	TCLCL -10	ns
$\overline{BCLK}$ High Time	(11)TBHCL		1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	0.65 TBLBL	ns
$\overline{BCLK}$ to $\overline{BUSY}$ Float Time	(22)TBLBYH		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	35	ns
$\overline{BCLK}$ to $\overline{CBRQ}$ Float Time	(26)TBLCBH		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
Input Rise Time	(29)TILIH		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	20	ns
Input Fall Time	(30)TIHIL		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	20	ns

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. VCC = 4.5V and 5.5V
3. Reference Table 2 for minimum limit.

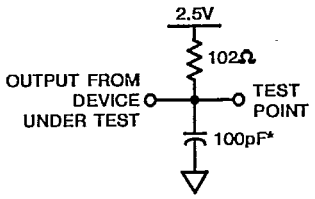
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

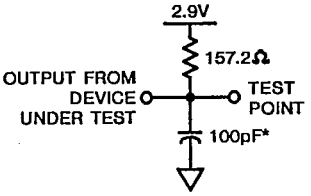
5 CMOS PERIPHERALS

A.C. Test Load Circuits

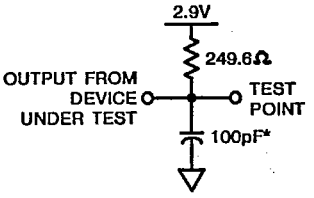
$\overline{BUSY}$, $\overline{CBRQ}$ LOAD CIRCUIT



$\overline{AEN}$ LOAD CIRCUIT



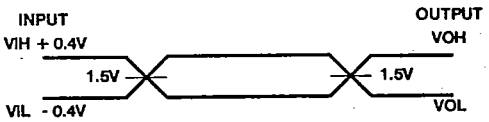
$\overline{BPRQ}$, $\overline{BREQ}$ LOAD CIRCUIT



* Includes Stray and Jig Capacitance

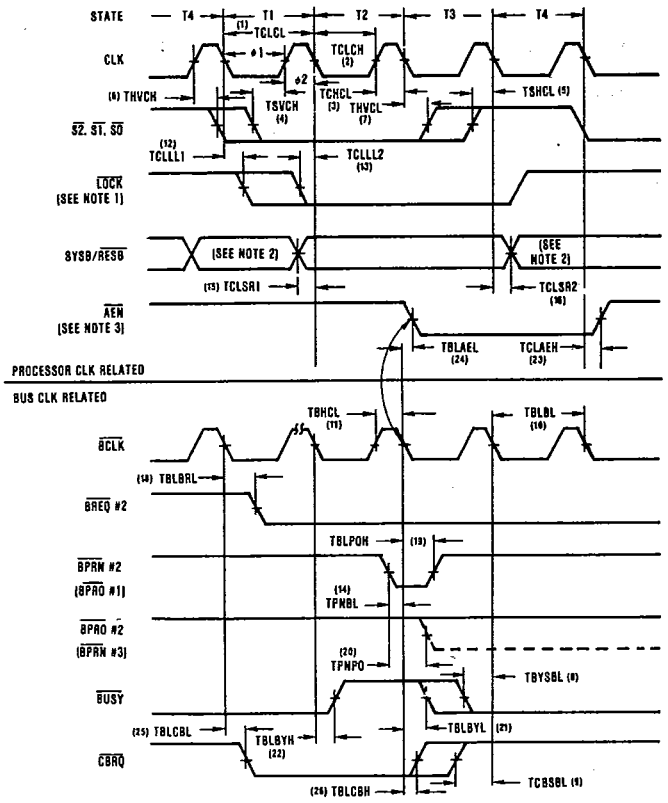
CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

A.C. Testing Input, Output Waveform



A.C. Testing: Inputs are driven at VIH +0.4V for a logic "1" and VIL -0.4V for a logic "0". The clock is driven at VCC -0.4V and 0.4V. Timing measurements are made at 1.5V for both a logic "1" and "0".

Timing Waveform



NOTES:

1. $\overline{LOCK}$ active can occur during any state, as long as the relationships shown above with respect to the CLK are maintained. $\overline{LOCK}$ inactive has no critical time and can be asynchronous. $\overline{CRQLCK}$ has no critical timing and is considered an asynchronous input signal.
2. Glitching of SYSB/$\overline{RESB}$ is permitted during this time. After Φ2 of T1, and before Φ1 of T4, SYSB/$\overline{RESB}$ should be stable to maintain system efficiency.
3. $\overline{AEN}$ leading edge is related to $\overline{BCLK}$, trailing edge to CLK. The trailing edge of $\overline{AEN}$ occurs after bus priority is lost.

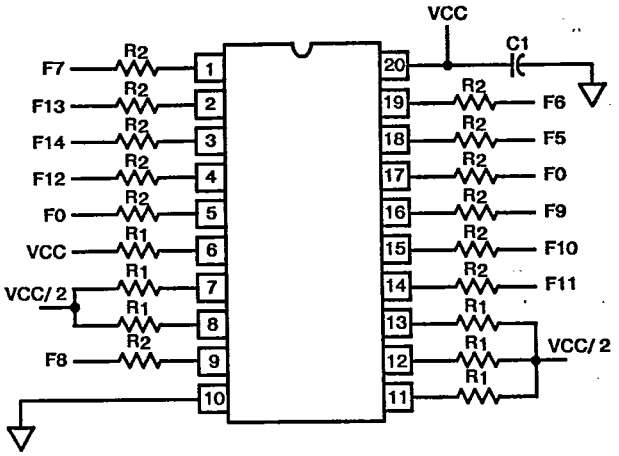
ADDITIONAL NOTES:

The signals related to CLK are typical processor signals, and do not relate to the depicted sequence of events of the signals referenced to $\overline{BCLK}$. The signals shown related to the $\overline{BCLK}$ represent a hypothetical sequence of events for illustration. Assume 3 bus arbiters of priorities 1, 2 and 3 configured in serial priority resolving scheme (as shown in Design Information Figure 3). Assume arbiter 1 has the bus and is holding $\overline{BUSY}$ low. Arbiter #2 detects its processor wants the bus and pulls low $\overline{BREQ}$ #2. If $\overline{BPRN}$ #2 is high (as shown), arbiter #2 will pull low $\overline{CBRQ}$ line. $\overline{CBRQ}$ signals to the higher priority arbiter #1 that a lower priority arbiter wants the bus. (A higher priority arbiter would be granted $\overline{BPRN}$ when it makes the bus request rather than having to wait for another arbiter to release the bus through $\overline{CBRQ}$). *Arbiter #1 will relinquish the multi-master system bus when it enters a state not requiring it (see Design Information Table A), by lowering its $\overline{BPRO}$ #1 (tied to $\overline{BPRN}$ #2) and releasing $\overline{BUSY}$. Arbiter #2 now sees that is has priority from $\overline{BPRN}$ #2 being low and releases $\overline{CBRQ}$. As soon as $\overline{BUSY}$ signifies the bus is available (high), arbiter #2 pulls $\overline{BUSY}$ low on next falling edge of $\overline{BCLK}$. Note that if arbiter #2 didn't want the bus at the time it received priority, it would pass priority to the next lower priority arbiter by lowering its $\overline{BPRO}$ #2 (TPNPO).

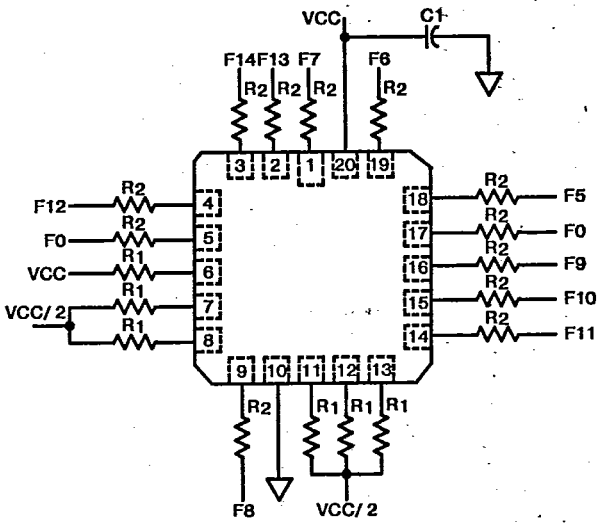
*Note that even a higher priority arbiter which is acquiring the bus through $\overline{BPRN}$ will momentarily drop $\overline{CBRQ}$ until it has acquired the bus.

Burn-In Circuits

82C89/883 CERAMIC DIP



82C89/883 CERAMIC LCC



NOTES:
1. VCC = 5.5V ± 0.5V, GND = 0V
2. VIH = 4.5V ± 10%, VIL = -0.2V to +0.4V
3. Components Values:
   R1 = 1.2kΩ, 1/4W, 5%
   R2 = 47kΩ, 1/4W, 5%
   C1 = 0.01μF minimum
   F0 = 100kHz ± 10%
   F1 = F0/2
   F2 = F1/2 . . .
   F14 = F13/2

Metallization Topology

DIE DIMENSIONS:
92.9 x 95.7 x 19 ± 1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 2kÅ

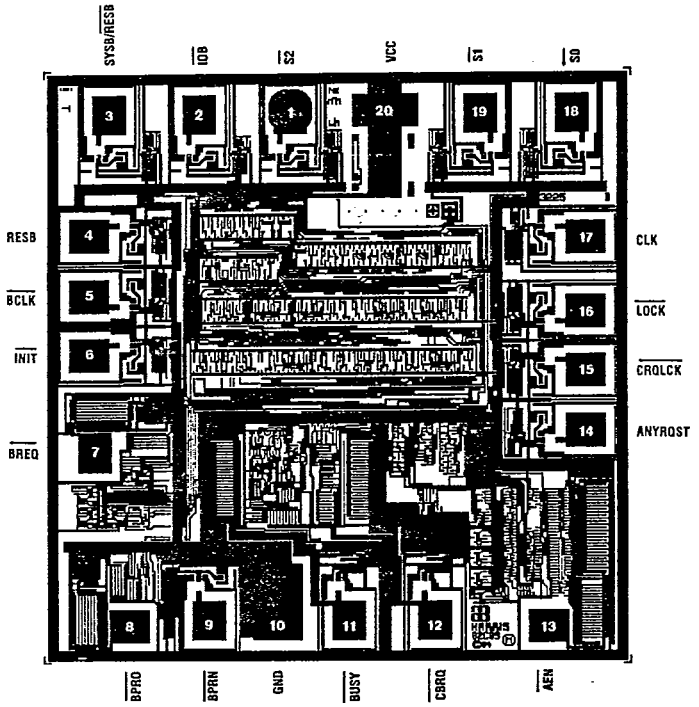
GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ ± 2kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.8×10^5 A/cm^2

Metallization Mask Layout

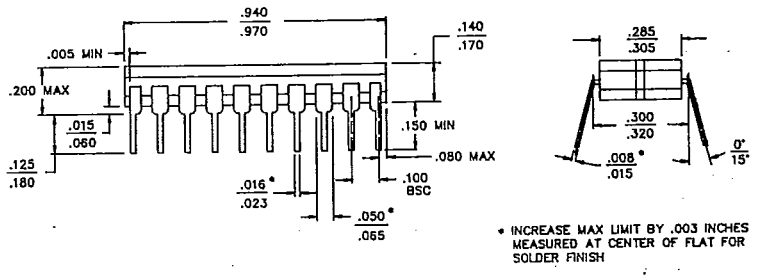
82C89/883



Packaging†

T-52-33-03

20 PIN CERAMIC DIP



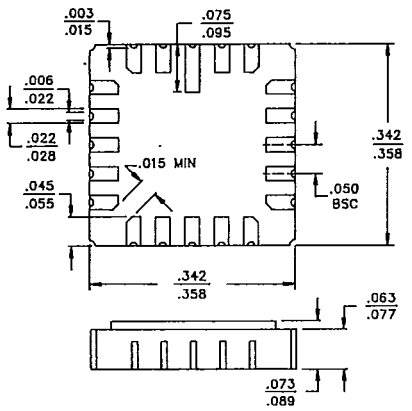
* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-8

20 PAD CERAMIC LCC

BOTTOM VIEW



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

82C89

T-52-33-03

DESIGN INFORMATION

CMOS Bus Arbiter

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Functional Description

The 82C89 Bus Arbiter operates in conjunction with the 82C88 Bus Controller to interface 80C86, 80C88 processors to a multi-master system bus (both the 80C86 and 80C88 are configured in their max mode). The processor is unaware of the arbiter's existence and issues commands as though it has exclusive use of the system bus. If the processor does not have the use of the multi-master system bus, the arbiter prevents the Bus Controller (82C88), the data transceivers and the address latches from accessing the system bus (e.g. all bus driver outputs are forced into the high impedance state). Since the command sequence was not issued by the 82C88, the system bus will appear as "Not Ready" and the processor will enter wait states. The processor will remain in Wait until the Bus Arbiter acquires the use of the multi-master system bus whereupon the arbiter will allow the bus controller, the data transceivers, and the address latches to access the system. Typically, once the command has been issued and a data transfer has taken place, a transfer acknowledge (XACK) is returned to the processor to indicate "READY" from the accessed slave device. The processor then completes its transfer cycle. Thus the arbiter serves to multiplex a processor (or bus master) onto a multi-master system bus and avoid contention problems between bus masters.

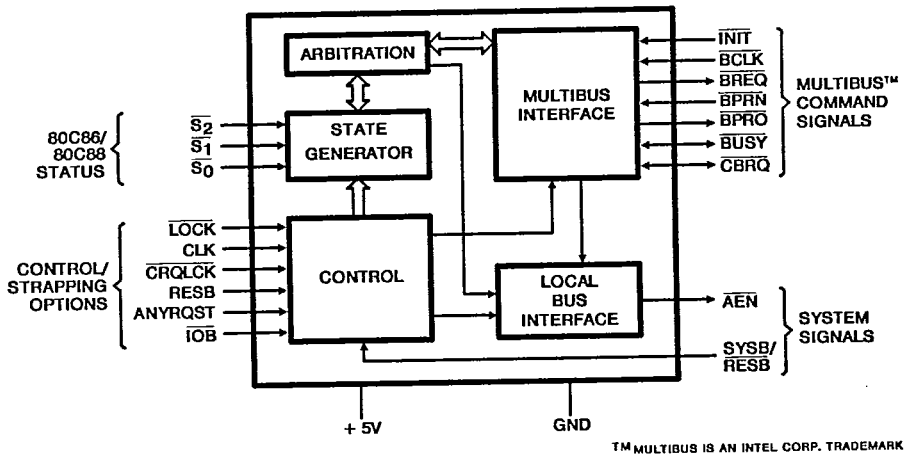
Arbitration Between Bus Masters

In general, higher priority masters obtain the bus when a lower priority master completes its present transfer cycle. Lower priority bus masters obtain the bus when a higher priority master is not accessing the system bus. A strapping option (ANYRQST) is provided to allow the arbiter to surrender the bus to a lower priority master as though it were a master of higher priority. If there are no other bus masters requesting the bus, the arbiter maintains the bus so long as its processor has not entered the HALT State. The arbiter will not voluntarily surrender the system bus and has to be forced off by another master's bus request, the HALT State being the only exception. Additional strapping options permit other modes of operation wherein the multi-master system bus is surrendered or requested under different sets of conditions.

Priority Resolving Techniques

Since there can be many bus masters on a multi-master system bus, some means of resolving priority between bus masters simultaneously requesting the bus must be provided. The 82C89 Bus Arbiter provides several resolving techniques. All the techniques are based on a priority concept that at a given time one bus master will have priority above all the rest. There are provisions for using parallel priority resolving techniques, serial priority resolving techniques, and rotating priority techniques.

Functional Diagram



TM MULTIBUS IS AN INTEL CORP. TRADEMARK

DESIGN INFORMATION (Continued)

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Parallel Priority Resolving

The parallel priority resolving technique uses a separate bus request line $\overline{BREQ}$ for each arbiter on the multi-master system bus, see Figure 1. Each $\overline{BREQ}$ line enters into a priority encoder which generates the binary address of the highest priority $\overline{BREQ}$ line which is active. The binary address is decoded by a decoder to select the corresponding $\overline{BPRN}$ (Bus Priority In) line to be returned to the highest priority requesting arbiter. The arbiter receiving priority ($\overline{BPRN}$ true) then allows its associated bus master onto the multi-master system bus as soon as it becomes available (i.e., the bus is no longer busy). When one bus arbiter gains priority over another arbiter it cannot immediately seize the bus, it must wait until the present bus transaction is complete. Upon completing its transaction the present bus occupant recognizes that it no longer has priority and surrenders the bus by releasing $\overline{BUSY}$. $\overline{BUSY}$ is an active low "OR" tied signal line which goes to every bus arbiter on the system bus. When $\overline{BUSY}$ goes inactive (high), the arbiter which presently has bus priority ($\overline{BPRN}$ true) then seizes the bus and pulls $\overline{BUSY}$ low to keep other arbiters off of the bus. See waveform timing diagram, Figure 2. Note that all multi-master system bus transactions are synchronized to the bus clock ($\overline{BCLK}$). This allows the parallel priority resolving circuitry or any other priority resolving scheme employed to settle.

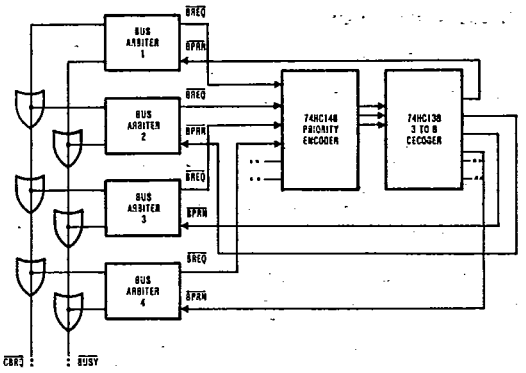
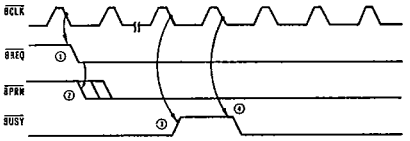


FIGURE 1. PARALLEL PRIORITY RESOLVING TECHNIQUE



NOTES:
1. Higher priority bus arbiter requests the Multi-Master system bus.
2. Attains priority.
3. Lower priority bus arbiter releases $\overline{BUSY}$.
4. Higher priority bus arbiter then acquires the bus and pulls $\overline{BUSY}$ down.

FIGURE 2. HIGHER PRIORITY ARBITER OBTAINING THE BUS FROM A LOWER PRIORITY ARBITER

Serial Priority Resolving

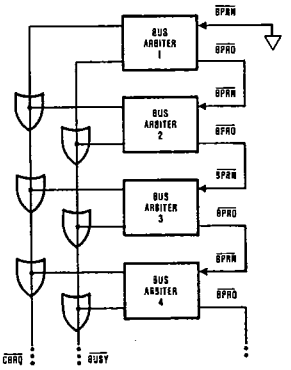
The serial priority resolving technique eliminates the need for the priority encoder-decoder arrangement by daisy-chaining the bus arbiters together, connecting the higher priority bus arbiter's $\overline{BPRO}$ (Bus Priority Out) output to the $\overline{BPRN}$ of the next lower priority. See Figure 3.

Rotating Priority Resolving

The rotating priority resolving technique is similar to that of the parallel priority resolving technique except that priority is dynamically re-assigned. The priority encoder is replaced by a more complex circuit which rotates priority between requesting arbiters thus allowing each arbiter an equal chance to use the multi-master system bus, over time.

Which Priority Resolving Technique To Use

There are advantages and disadvantages for each of the techniques described above. The rotating priority resolving technique requires substantial external logic to implement while the serial technique uses no external logic but can accommodate only a limited number of bus arbiters before the daisy-chain propagation delay exceeds the multi-master's system bus clock ($\overline{BCLK}$). The parallel priority resolving technique is in general a good compromise between the other two techniques. It allows for many arbiters to be present on the bus while not requiring too much logic to implement.



NOTE:
The number of arbiters that may be daisy-chained together in the serial priority resolving scheme is a function of $\overline{BCLK}$ and the propagation delay from arbiter to arbiter. Normally, at 10MHz only 3 arbiters may be daisychained.

FIGURE 3. SERIAL PRIORITY RESOLVING

DESIGN INFORMATION (Continued)

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82C89 Modes Of Operation

There are two types of processors for which the 82C89 will provide support: An Input/Output processor (i.e. an NMOS 8089 IOP) and the 80C86, 80C88. Consequently, there are two basic operating modes in the 82C89 bus arbiter. One, the IOB (I/O Peripheral Bus) mode, permits the processor access to both an I/O Peripheral Bus and a multi-master system bus. The second, the RESB (Resident Bus mode), permits the processor to communicate over both a Resident Bus and a multi-master system bus. An I/O Peripheral Bus is a bus where all devices on that bus, including memory, are treated as I/O devices and are addressed by I/O commands. All memory commands are directed to another bus, the multi-master system bus. A Resident Bus can issue both memory and I/O commands, but it is a distinct and separate bus from the multi-master system bus. The distinction is that the Resident Bus has only one master, providing full availability and being dedicated to that one master.

The $\overline{IOB}$ strapping option configures the 82C89 Bus Arbiter into the $\overline{IOB}$ mode and the strapping option RESB configures it into the RESB mode. It might be noted at this point that if both strapping options are strapped false, the arbiter interfaces the processor to a multi-master system bus only (see Figure 4). With both options strapped true, the arbiter interfaces the processor to a multi-master system bus, a Resident Bus, and an I/O Bus.

In the $\overline{IOB}$ mode, the processor communicates and controls a host of peripherals over the Peripheral Bus. When the I/O Processor needs to communicate with system memory, it does so over the system memory bus. Figure 5 shows a possible I/O Processor system configuration.

The 80C86 and 80C88 processors can communicate with a Resident Bus and a multi-master system bus. Two bus controllers and only one Bus Arbiter would be needed in such a configuration as shown in Figure 6. In such a system configuration the processor would have access to memory and peripherals of both busses. Memory mapping techniques are applied to select which bus is to be

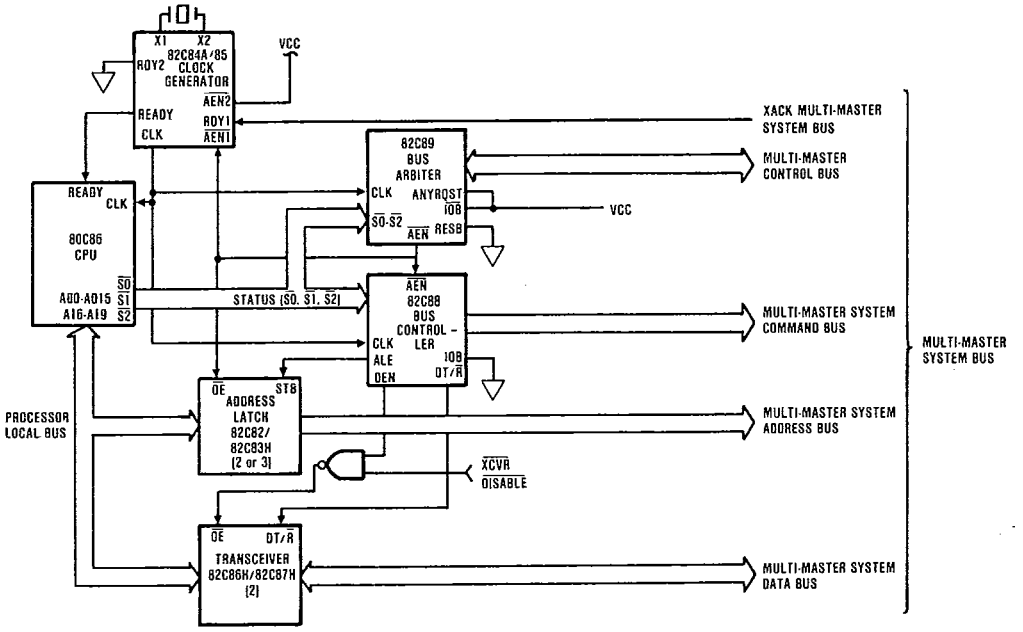

FIGURE 4. TYPICAL MEDIUM COMPLEXITY CPU SYSTEM

DESIGN INFORMATION (Continued)

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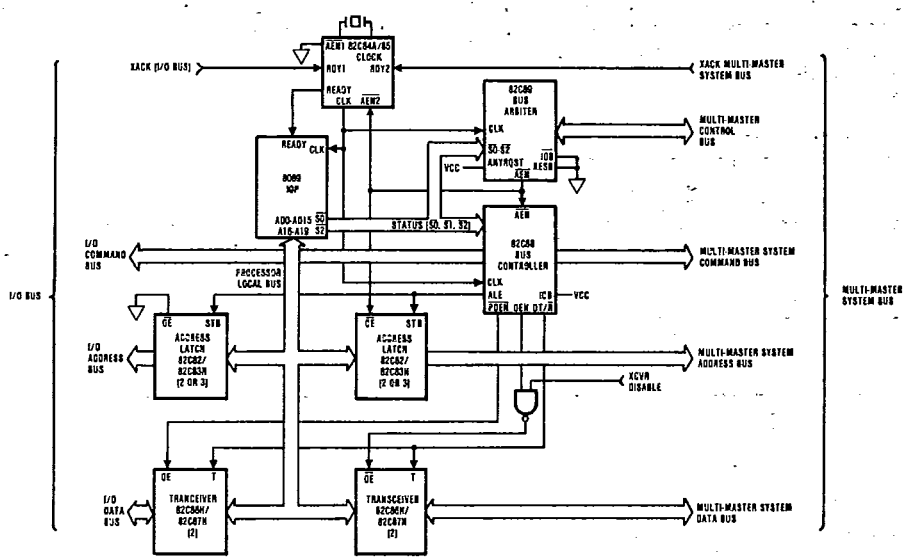

FIGURE 5. TYPICAL MEDIUM COMPLEXITY IOB SYSTEM

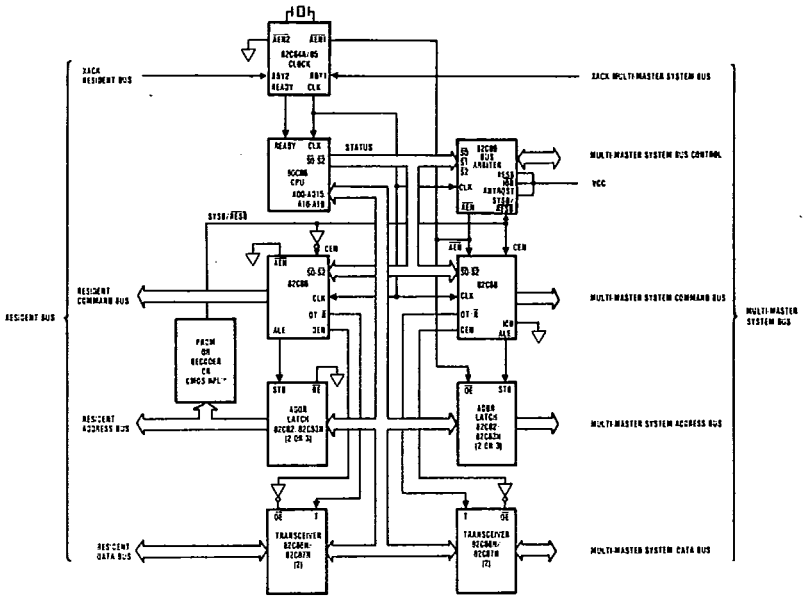

FIGURE 6. 82C89 BUS ARBITER SHOWN IN SYSTEM - RESIDENT BUS CONFIGURATION

* By adding another 82C89 arbiter and connecting its $\overline{AEN}$ to the 82C88 whose $\overline{AEN}$ is presently grounded, the processor could have access to two multi-master buses.

5 CMOS PERIPHERALS

DESIGN INFORMATION (Continued)

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accessed. The SYSB/$\overline{RESB}$ input on the arbiter serves to instruct the arbiter as to whether or not the system bus is to be accessed. The signal connected to SYSB/$\overline{RESB}$ also enables or disables commands from one of the bus controllers.

A summary of the modes that the 82C89 has, along with its response to its status lines inputs, is shown in Table A.

TABLE A. SUMMARY OF 82C89 MODES, REQUESTING AND RELINQUISHING THE MULTI-MASTER SYSTEM BUS

STATUS LINES FROM 80C86 OR 80C88 OR 8088				IOB MODE ONLY $\overline{IOB}$ = LOW RESB = LOW	RESB MODE ONLY $\overline{IOB}$ = HIGH, RESB = HIGH		IOB MODE RESB MODE $\overline{IOB}$ = LOW, RESB = HIGH		SINGLE BUS MODE $\overline{IOB}$ = HIGH RESB = LOW
	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$		SYSB/$\overline{RESB}$ = HIGH	SYSB/$\overline{RESB}$ = LOW	SYSB/$\overline{RESB}$ = HIGH	SYSB/$\overline{RESB}$ = LOW	
I/O Commands	0	0	0	X	✓	X	X	X	✓
	0	0	1	X	✓	X	X	X	✓
	0	1	0	X	✓	X	X	X	✓
Halt	0	1	1	X	X	X	X	X	X
Memory Commands	1	0	0	✓	✓	X	✓	X	✓
	1	0	1	✓	✓	X	✓	X	✓
	1	1	0	✓	✓	X	✓	X	✓
Idle	1	1	1	X	X	X	X	X	X

NOTES: 1. X = Multi-Master System Bus is allowed to be Surrendered.
2. ✓ = Multi-Master System Bus is Requested.

MODE	PIN STRAPPING	MULTI-MASTER SYSTEM BUS	
		REQUESTED**	SURRENDERED*
Single Bus Multi-Master Mode	$\overline{IOB}$ = High RESB = Low	Whenever the processor's status lines go active	HLT + TI • $\overline{CBRQ}$ + HPBRQ †
RESB Mode Only	$\overline{IOB}$ = High RESB = High	SYSB/$\overline{RESB}$ + High • ACTIVE STATUS	(SYSB/$\overline{RESB}$ = Low + TI) • $\overline{CBRQ}$ + HLT + HPBRQ
IOB Mode Only	$\overline{IOB}$ = Low RESB = Low	Memory Commands	(I/O Status + TI) • $\overline{CBRQ}$ + HLT + HPBRQ
IOB Mode RESB Mode	$\overline{IOB}$ = Low RESB = High	(Memory Command) • (SYSB/$\overline{RESB}$ = High)	((I/O Status Commands) + SYSB/$\overline{RESB}$ = Low) • $\overline{CBRQ}$ +HPBRQ † + HLT

NOTES: * $\overline{LOCK}$ prevents surrender of Bus to any other arbiter, $\overline{CRQLCK}$ prevents surrender of Bus to any lower priority arbiter.
**Except for HALT and Passive or IDLE Status.
† HPBRQ, Higher priority Bus request or $\overline{BPRN}$ = 1.
1. $\overline{IOB}$ Active Low.
2. RESB Active High.
3. + is read as "OR" and • as "AND"
4. TI = Processor Idle Status $\overline{S2}$, $\overline{S1}$, $\overline{S0}$ = 111
5. HLT = Processor Halt Status $\overline{S2}$, $\overline{S1}$, $\overline{S0}$ = 011

Packaging Techniques

T-90-20

Harris Semiconductor offers Leadless Chip Carriers (LCC) as a packaging option on various Digital integrated circuits. An LCC is a square or rectangular package for an Integrated Circuit (IC) that is manufactured in the same manner as a conventional side-braze dual-in-line package (DIP). The LCC is comprised of the cavity and seal ring section of a standard DIP and offers the user a means of achieving high density system configurations while retaining the reliability benefits of hermetic IC Packaging. Figure 1 provides a comparison of the construction of an LCC and a conventional side-braze DIP.

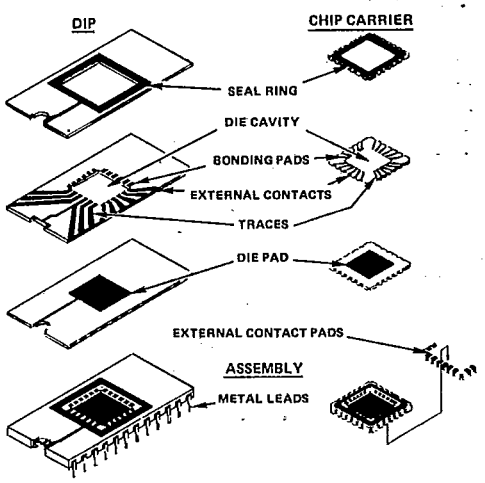


FIGURE 1. EXPLODED VIEW OF CHIP CARRIER AND DIP

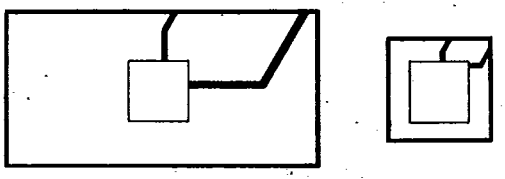
The LCC's two principle advantages over conventional side-braze DIPs are packaging density and electrical performance. Packaging density is the number one advantage to an LCC over a side-braze DIP. The size of a DIP is governed primarily by the number of leads required and not by the size of the IC. As pin count increases, more and more of the DIP package is used only to provide an electrical trace path to the external leads. The size of an LCC is dependent on the size of the die not on the number of leads. As pin count increases, overall size increases but at a much slower rate. Table 1 provides a comparison between the areas of 18, 28 and 48 lead LCCs to 18, 28 and 48 lead side-braze DIPs.

TABLE 1.

LEAD COUNT	LCC AREA	DIP AREA	DIP AREA vs. LCC AREA
18	0.10	0.22	220%
28	0.20	0.84	420%
48	0.31	1.68	542%

(All Units in Square Inches)

The chart indicates a 220% improvement in packaging area for the 18 lead LCC, and 542% improvement for the 48 lead LCC. Obviously, sizeable savings in circuit board area can be achieved with this packaging option. The second major advantage of the LCC is in electrical performance. The package size and geometry also dictates trace length and uniformity. Figure 2 provides a comparison between the trace lengths for various LCCs and side-braze DIPs. As pin count goes up, trace lengths get longer, adding resistance and capacitance unequally around the package. As ICs get faster and more complex these factors start to become a limiting factor on performance. LCCs minimize this effect by maintaining, as close as possible, uniform trace length so that the package is a significantly smaller determinant of system performance.



LEAD COUNT	LONGEST TRACE DIP LONGEST TRACE LCC	LONGEST TRACE SHORTEST TRACE	
		LCC	DIP
18	2:1	1.5:1	6:1
24	4:1	1.5:1	3:1
40	5:1	1.5:1	6:1
54	6:1	1.5:1	7:1

FIGURE 2. ELECTRICAL PERFORMANCE (RESISTANCE AND SPEED)

The LCC also offers environmental advantages over "chip-and-wire" manufacturing techniques used in high density hybrid circuits. An IC can be fully tested, burned-in and processed in an LCC, thereby guaranteeing its performance.

The IC is further protected by a small hermetic package in which internal vapor content can be carefully controlled during production.

Harris Semiconductor Leadless Chip Carriers in both Ceramic and Epoxy provide reliable, high density, high performance packaging options for today's systems.

Consult the factory or your Harris sales representative for pricing and availability.