Ordering number : EN*A0337

Preliminary

SANYO Semiconductors
DATA SHEET

Bi-CMOS IC

LV2258PV — 315MHz and 434MHz Band Wireless System Receiver IC

Overview

The LV2258PV is an FSK/ASK receiver IC that is optimal for keyless entry and other short-range wireless systems and that integrates RF amplifier, mixer, PLL, FM detector, RSSI, data filter, and data shaper circuits on the same IC. The LV2258PV reduces the number of external components required by integrating the VCO circuit and the FM detection phase shifter on the same chip, and thus supports compact end product designs.

Functions and Features

- Supports both the 315 and the 434MHz bands
- RF amplifier
- Mixer
- PLL circuit
- Built-in local VCO
- Built-in phase shifter for FM detection
- Data filter
- Data shaper
- Power saving mode control pin
- Miniature package: SSOP24 (0.65mm lead pitch)

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		6	V
Allowable power dissipation	Pd max	≤ 85°C, Mounted on a circuit board*	150	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-40 to +125	°C
Recommended operating supply voltage range	V_{CC}		4.5 to 5.5	V

* Mounted on a specified board: 114.3mm×76.1mm×1.6mm glass epoxy

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

DC Characteristics at Ta = +25°C, V_{CC} = 5.0V, 315MHz mode

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain 1	$I_{CC}1$	All circuits operating ON		8		mA
Current drain 2	$I_{CC}2$	All circuits operating OFF		0.1	1.0	μA
Logic input low-level input voltage	$V_{IN}L$				0.5	V
Logic input high-level input voltage	$V_{IN}H$		V_{CC}×0.8			V

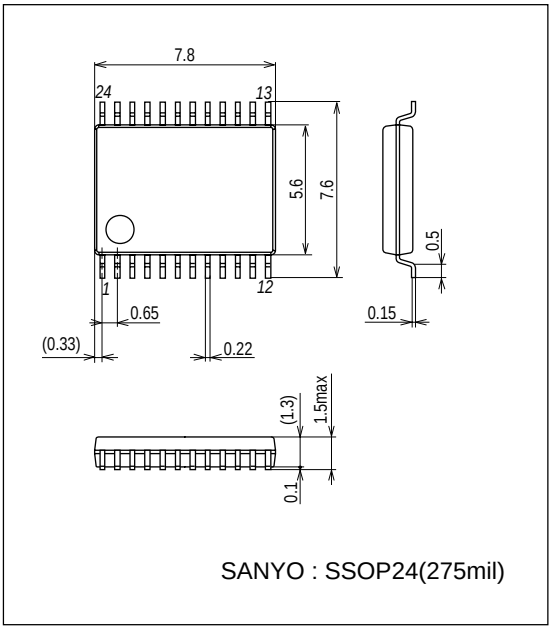
AC Characteristics at Ta = +25°C, V_{CC} = 5.0V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
RF Amplifier (Frfin = 315MHz)						
Gain	Grf	Matching input		15		dB
Input dynamic range	1dB CP1	Matching input		-40		dBm
Mixer (Frfin = 315MHz)						
Conversion gain	Gmix			20		dB
Input dynamic range	1dB CP2			-25		dBm
PLL						
Crystal input operating frequency	F X tal	V X tal = -6dBm	7		15	MHz
Charge pump current	Icp	Vcp = 2.5V		±200		μA
Charge pump off state leakage current	Icpoff	Vcp = 2.5V	-100		100	nA
FM detector (Frfin = 315MHz, Fdev = ±30kHz, Fmod = 1kHz sine wave)						
12dB SINAD sensitivity	12dB SINAD	Matching input		-115		dBm
AF modulation level	V_O	V_I = -50dBm		220		mVrms
Signal-to-noise ratio	S/N	V_I = -50dBm		65		dB
AM rejection ratio	AMR	V_I = -50dBm, AM 30% mod.		50		dB
RSSI (Frfin = 315MHz)						
RSSI1	RSSI1	V_I = -120dBm		0.3		V
RSSI2	RSSI2	V_I = -110dBm		0.5		V
RSSI3	RSSI3	V_I = -80dBm		1.5		V
RSSI4	RSSI4	V_I = -50dBm		2.5		V
Data Shaper Duty 1 (Frfin = 315MHz, Fdev = ±30kHz, Fmod = 1kHz square wave, FSK mode)						
Duty	Dty	V_I = -50dBm	45	50	55	%
Low-level output voltage	V_OLo	V_I = -50dBm			0.3	V
Data Shaper Duty 2 (Frfin = 315MHz, AM90%mod, Fmod = 1kHz square wave, ASK mode)						
Duty	Dty	V_I = -50dBm	45	50	55	%
Low-level output voltage	V_OLo	V_I = -50dBm			0.3	V

Package Dimensions

unit : mm (typ)

3175C



SANYO : SSOP24(275mil)

Pin Functions

Pin No.	Pin	Function
1	F/A	FSK/ASK mode switching. Low: FSK, high: ASK
2	FSEL	Frequency switch. Low: 315 MHz, high: 434 MHz
3	XIN	Crystal oscillator connection
4	AFGND	AF system ground
5	VREG	Regulator capacitor connection
6	QC	Quick charge capacitor connection
7	DSOUT	Data output
8	PS	Power saving mode control. Low: normal operation, high: power saving mode
9	DSREF	Data shaper reference
10	LPFOUT	Data filter output
11	C2	Data filter cutoff frequency adjustment capacitor connection
12	C1	Data filter cutoff frequency adjustment capacitor connection
13	LPFIN	Data filter input
14	AFOUT	FSK/ASK detection output
15	RSSI	RSSI output
16	TUNE	IF tuning circuit capacitor connection
17	IFREF	IF amplifier reference
18	IFIN	IF amplifier input
19	IFV_{CC}	IF system power supply (V_{CC})
20	IFOUT	Mixer output
21	RFGND	RF system ground
22	RFOUT	RF amplifier output
23	RFV_{CC}	RF system power supply (V_{CC})
24	RFIN	RF amplifier input

Block Diagram