40160B

SYNCHRONOUS PROGRAMMABLE 4-BIT COUNTERS

40160B - DECADE WITH ASYNCHRONOUS CLEAR
40161B - BINARY WITH ASYNCHRONOUS CLEAR
40162B - DECADE WITH SYNCHRONOUS CLEAR
40163B - BINARY WITH SYNCHRONOUS CLEAR

- INTERNAL LOOK-AHEAD FOR FAST COUNTING
- CARRY OUTPUT FOR CASCADING
- SYNCHRONOUSLY PROGRAMMABLE
- SYNCHRONOUS LOAD CONTROL INPUT
- LOW-POWER TTL COMPATIBILITY
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 40160B, 40161B, 40162B, 40163B** (extended temperature range) and **HCF 40160, 40161. 40162, 40163** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. **HCC/HCF 40160B, 40161B, 40162B,** and **40163B** are 4-bit synchronous programmable counters. The $\overline{\text{CLEAR}}$ function of the **HCC/HCF 40162B** and **40163B** is synchronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low on the next positive CLOCK edge. The $\overline{\text{CLEAR}}$ function of the **HCC/HCF 40160B** and **40161B** is asynchronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low regardless of the state of the CLOCK, $\overline{\text{LOAD}}$, or ENABLE inputs. A low level at the $\overline{\text{LOAD}}$ input disables the counter and causes the output to agree with the setup data after the next CLOCK pulse regardless of the conditions of the ENABLE inputs. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output (C_{OUT}). Counting is enable when both PE and TE inputs are high. The TE input is fed forward to enable C_{OUT}. This enabled output produces a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages. Logic transitions at the PE or TE inputs may occur when the clock is either high or low.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_i	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

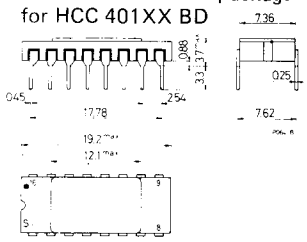
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

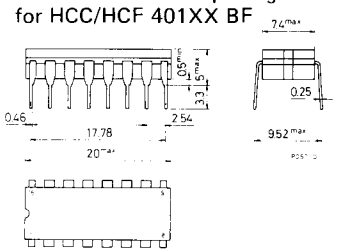
HCC 401XX BD for dual in-line ceramic package
HCC 401XX BF for dual in-line ceramic package, frit seal
HCC 401XX BK for ceramic flat package
HCF 401XX BE for dual in-line plastic package
HCF 401XX BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

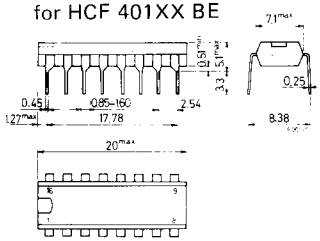
Dual in-line ceramic package for HCC 401XX BD



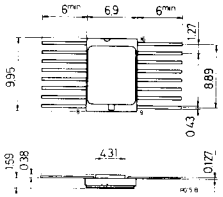
Dual in-line ceramic package for HCC/HCF 401XX BF



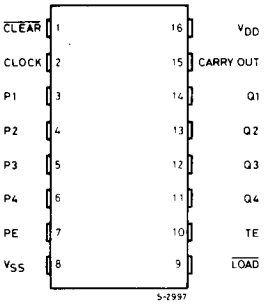
Dual in-line plastic package for HCF 401XX BE



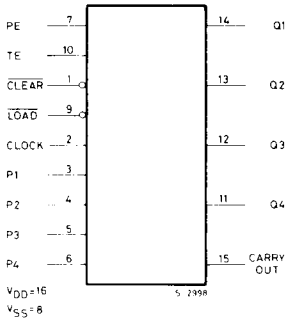
Ceramic flat package for HCC 401XX BK



PIN CONNECTIONS



FUNCTIONAL DIAGRAM

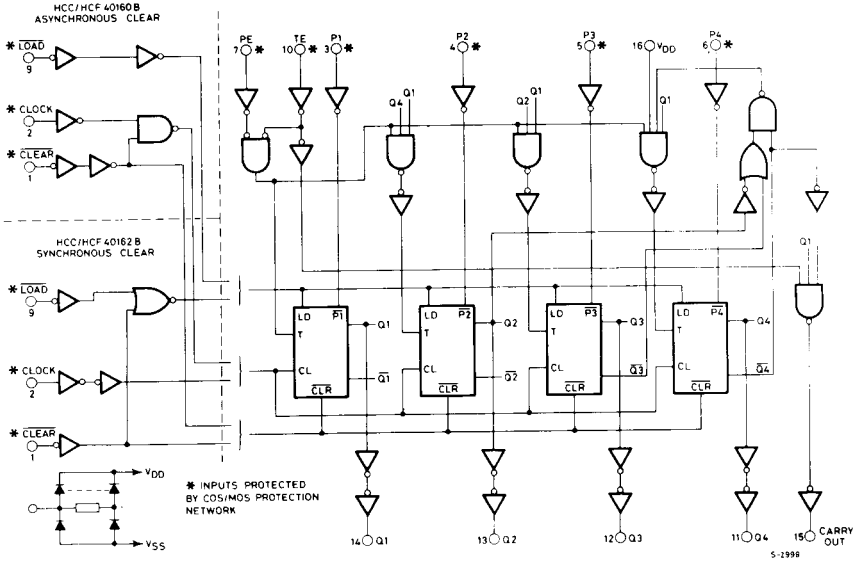


RECOMMENDED OPERATING CONDITIONS

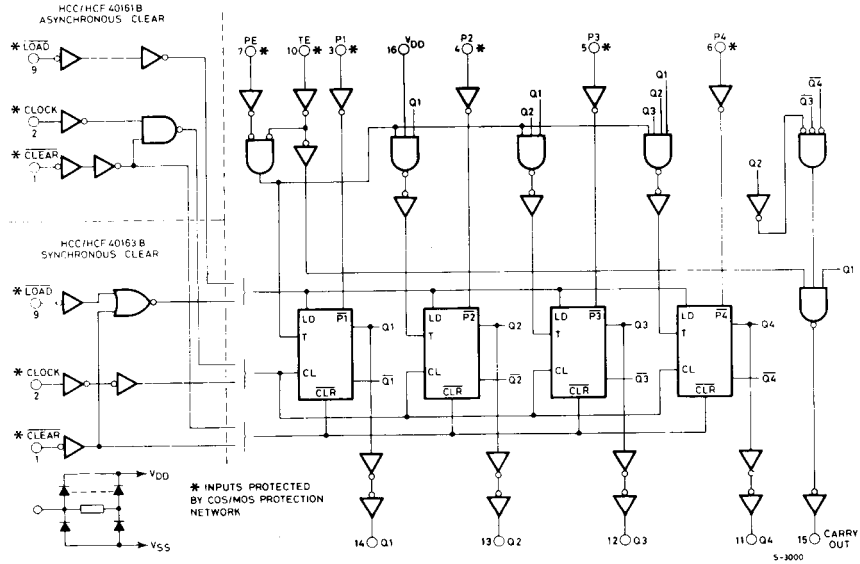
V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

LOGIC DIAGRAMS

For **40160B** and **40162B** BCD decade counters.

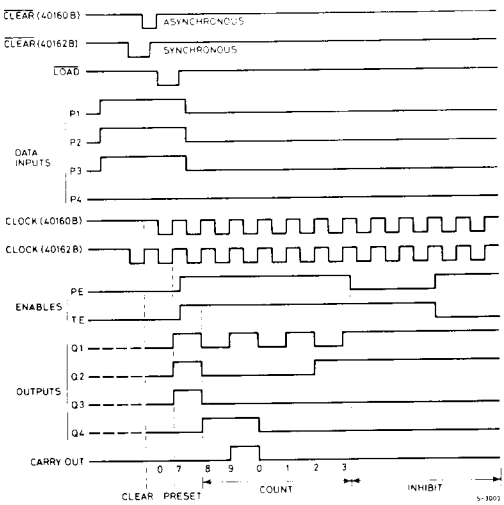


For **40161B** and **40163B** binary counters.

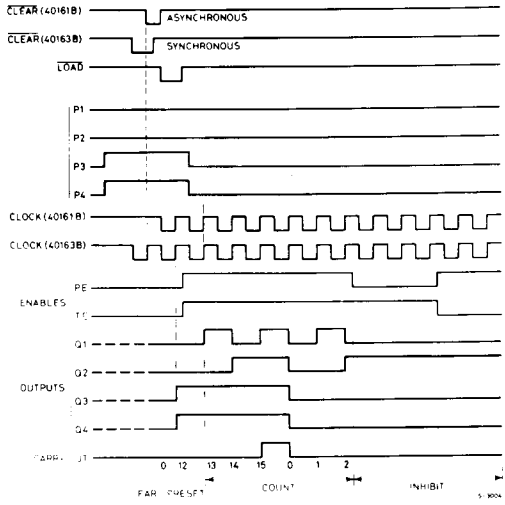


TIMING DIAGRAMS

for **40160B** and **40162B**



for **40161B** and **40163B**



TRUTH TABLE

CLOCK	$\overline{CLR}$	$\overline{LOAD}$	PE	TE	OPERATION
⌐¯	1	0	X	X	PRESET
⌐¯	1	1	0	X	NC
⌐¯	1	1	X	0	NC
⌐¯	1	1	1	1	COUNT
X	0	X	X	X	RESET (HCC/HCF 40160B, HCC/HCF 40161B)
⌐¯	0	X	X	X	RESET (HCC/HCF 40162B, HCC/HCF 40163B)
¯⌐	1	X	X	X	NC (HCC/HCF 40162B, HCC/HCF 40163B)

1 = HIGH LEVEL
0 = LOW LEVEL
X = DON'T CARE
NC= NO CHANGE

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		±0.1		$±10^{-5}$	±0.1		± 1	μA
		HCF types	0/15			15		±0.3		$±10^{-5}$	±0.3		± 1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device: -40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns)

Parameter			Test conditions	Values			Unit
			V_{DD}(V)	Min.	Typ.	Max.	
CLOCK OPERATION							
t_{PHL}, t_{PLH}	Propagation delay time	Clock to Q	5		200	400	ns
			10		30	160	
			15		60	120	
		Clock to C_{OUT}	5		225	450	ns
			10		95	190	
			15		70	140	
		TE to C_{OUT}	5		125	250	ns
			10		55	110	
			15		40	80	
t_{setup}	Setup time	Data to Clock	5	240	120		ns
			10	90	45		
			15	60	30		
		$\overline{Load}$ to Clock	5	240	120		ns
			10	90	45		
			15	60	30		
		PE to TE to Clock	5	340	170		ns
			10	140	70		
			15	100	50		
t_{hold}	Hold time		5	0			ns
			10	0			
			15	0			
t_{THL} t_{TLH}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
t_W	Clock input pulse width		5	170	85		ns
			10	70	35		
			15	50	25		
f_{CL}	Maximum clock input frequency		5	2	3		MHz
			10	5.5	8.5		
			15	8	12		
t_r, t_f	Clock input rise or fall time*		5			200	μs
			10			70	
			15			15	

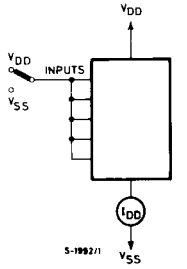
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Values			Unit
		V_{DD}(V)	Min.	Typ.	Max.	
CLEAR OPERATION						
t_{PHL}	Propagation delay time (HCC/HCF 40160B, 40161B) Clear to Q	5		250	500	ns
		10		110	220	
		15		80	160	
t_{setup}	Setup time (HCC/HCF 40162B, 40163B) Clear to clock	5	340	170		ns
		10	140	70		
		15	100	50		
t_{hold}	Hold time (HCC/HCF 40162B, 40163B) Clear to clock	5	0			ns
		10	0			
		15	0			
t_{rem}	Clear removal time (HCC/HCF 40160B, 40161B)	5	200	100		ns
		10	100	50		
		15	70	35		
t_W	Clear input pulse width Low level (HCC/HCF 40160B, 40161B)		170	85		ns
			70	35		
			50	25		

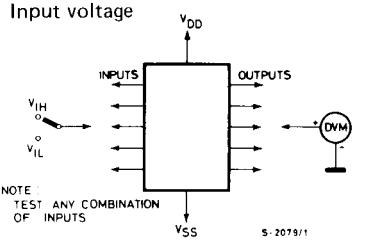
* If more than one unit is cascaded in the parallel clocked application, t_r should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the carry output driving stage for the estimated capacitive load.

TEST CIRCUITS

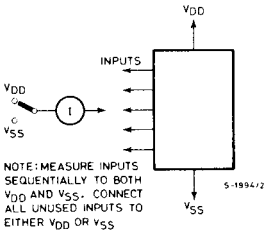
Quiescent device current



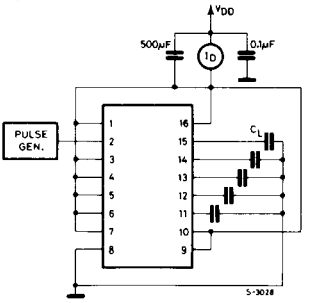
Input voltage



Input leakage current

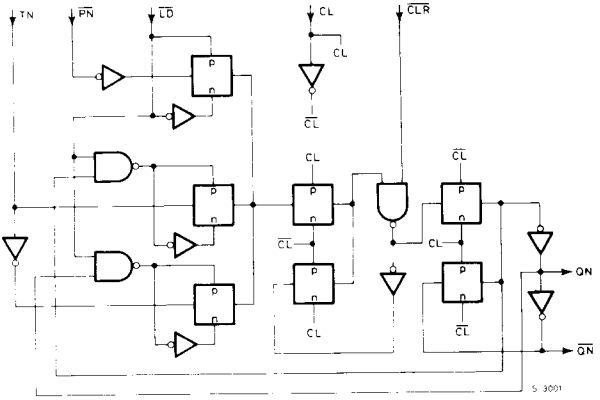


Dynamic power dissipation

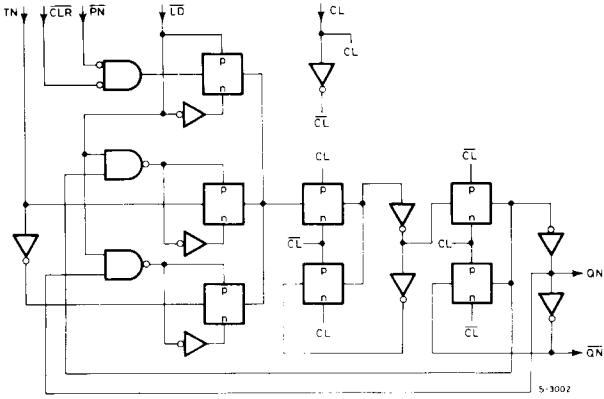


TYPICAL APPLICATIONS

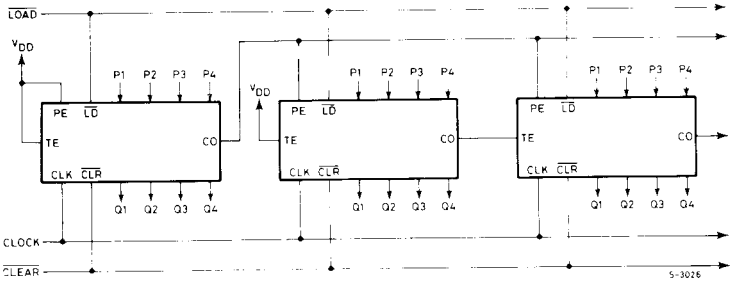
Detail of flip-flops for **40160B** and **40161B** (asynchronous clear)



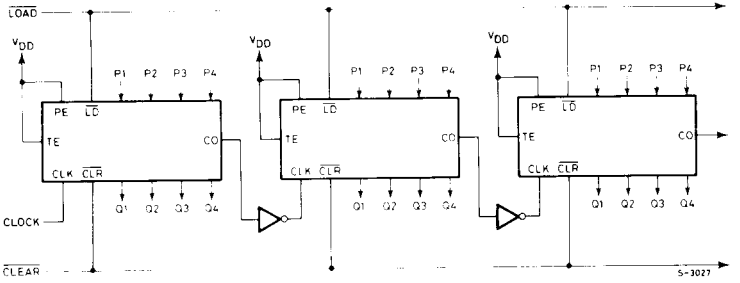
Detail of flip-flops for **40162B** and **40163B** (synchronous clear)



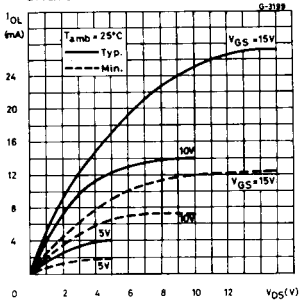
Cascaded counter packages in the parallel-clocked mode.



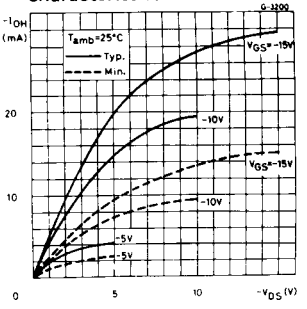
Cascaded counter packages in the ripple-clocked mode.



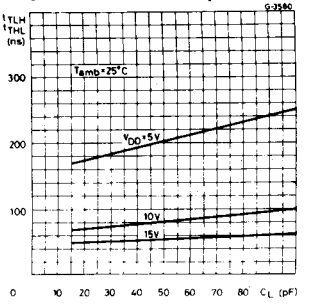
Output low (sink) current characteristics



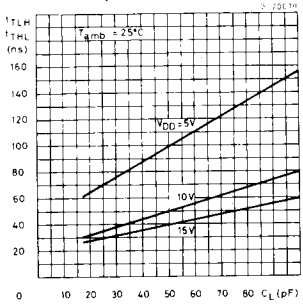
Output high (source) current characteristics



Typical propagation delay time vs. load capacitance



Typical transition time vs. load capacitance



Typical dynamic power dissipation vs. clock frequency