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SSI 32P541C
Pulse Detector

Preliminary Data

December 1993

DESCRIPTION

The SSI 32P541C is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals.

In Read mode the SSI 32P541C provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

In Write mode the circuitry is disabled and the AGC gain stage input impedance is switched to a lower level to allow fast settling of the input coupling capacitors during a write to read transition. The SSI 32P541C requires a +5V power supply and is available in a 28-pin PLCC package.

FEATURES

- **Level qualification supports high resolution MFM and RLL encoded data retrieval**
- **Wide bandwidth AGC input amplifier**
- **Standard +5V ±10% supplies**
- **Write to read transient suppression**
- **Fast and slow AGC attack regions for fast transient recovery**
- **≤1.0 ns pulse pairing**
- **32 Mbit/s operation**
- **Low power**

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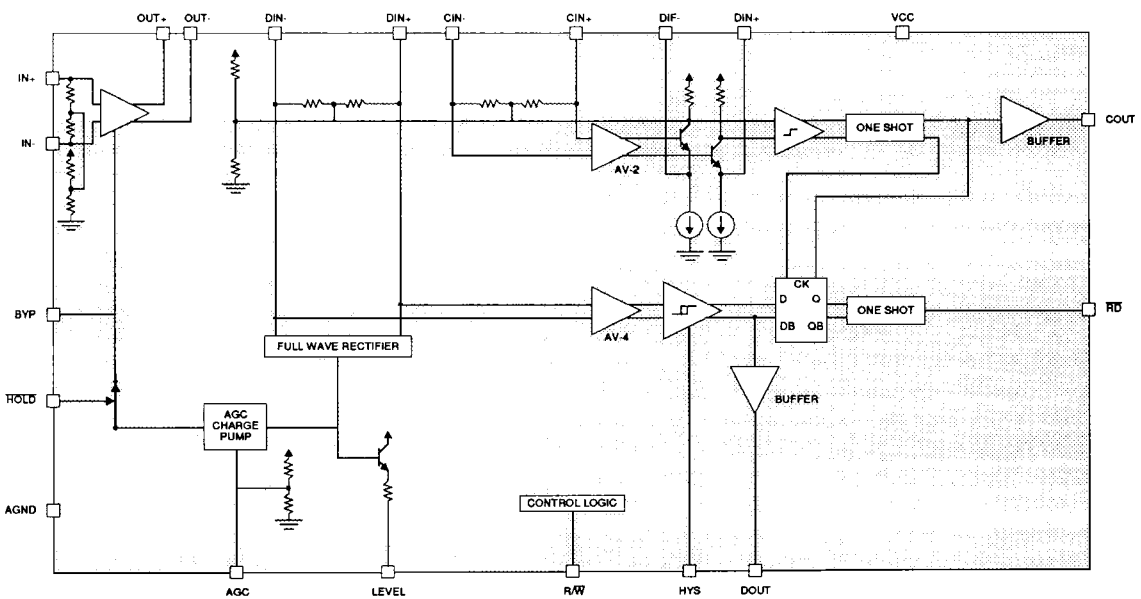
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

READ MODE

In Read mode (R/$\overline{W}$ input high or open) the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+)-(DIN-)] voltage level and comparing it to a reference voltage level at the AGC pin.

The 32P541C contains a dual rate attack charge pump. The value of the attack current is dependent on the instantaneous level at DIN±. For signal levels above 125% of the desired level a Fast Attack mode is invoked that supplies a 1.2 mA charge current to the network on the BYP pin. Between 125% and 100% of the desired level the circuit enters a Slow Attack mode and supplies 0.17 mA of charge current to the BYP pin.

Two Decay modes are available and are automatically controlled within the device.

Upon a switch to Write mode, the device will hold the gain at its previous value. When the device is then switched back to Read mode the AGC holds the gain and stays in a low impedance state for 0.9 µs. It then switches into a Fast/Slow Attack mode if the new gain required is less than the previously held gain or a Fast Decay mode if the gain required is more than its previous value. The fast decay current is 0.10 mA and stays on for 0.9 µs. After the 0.9 µs time period the device stays in a steady state slow attack, Slow Decay mode. The slow decay discharge current is 4.5 µA.

The AGC pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vpp under nominal conditions. The voltage on this pin can be modified by tying a resistor between AGC and GND or VPA. A resistor to GND decreases the voltage level, while a resistor to VPA increases it. The resulting AGC voltage level is shown in Figure 1; where:

V = Voltage at AGC w/pin open (2.2V, nom)

Rint = AGC pin input impedance (3.9 kΩ, typ)

Rext = External resistor

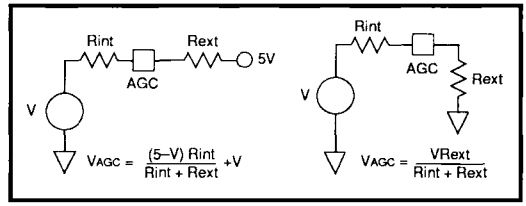


FIGURE 1: AGC Voltage

The new DIN± input target level is nominally: 0.45 Vpp/V • V_{AGC}.

The maximum AGC amplifier output swing is 3.0 Vpp at OUT±, which allows for up to 6 dB loss in any external filter between OUT± and DIN±.

AGC gain is a linear function of the BYP-pin voltage (VBYP) as shown in Figure 2.

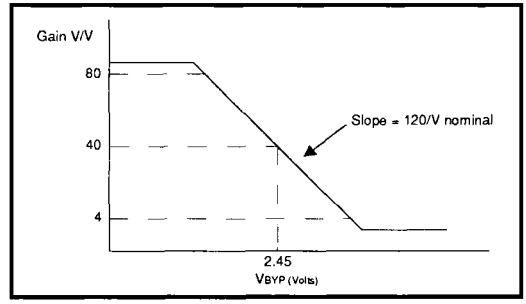


FIGURE 2: AGC Gain

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be a fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 Vpp at DIN± results in 1.0 V0-pk nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example,

if DIN± is 1.0 Vpp, then using an equal valued resistor divider will result in 0.5 Vpk at the HYS pin. This will result in a nominal ±0.18V threshold or a 36% threshold of a ±0.500V DIN± input. The capacitor is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin is a comparator output signal for testing purposes only.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$Av = \frac{-3536Cs}{LCs^2 + C(R+52)s + 1}$$

where: C, L, R are external passive components
$15\ pF < C < 125\ pF$
$s = j\omega = j2\pi f$

OFF-CHIP DIFFERENTIATION

For constant density recording applications, a differentiation function with a low pass bandwidth tracking data rate can maximize the signal-to-noise ratio performance. A time differentiated input can be applied at the CIN± pins, separated from the DIN± pins. A 2.0 kΩ resistor should be placed across the DIF± pins. This function can best be supported by the Silicon Systems programmable filters, such as the SSI 32F8020A and the SSI 32F8120A. The filters feature both a normal low pass output and a differentiated low pass output. The low pass bandwidth is programmable by the user to track the data rate. The signal delays of the two signal paths are well matched.

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched.

WRITE MODE

In Write Mode the SSI 32P541C Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P541C and a head preamplifier such as the SSI 32R2020R. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

MODE CONTROL

The SSI 32P541C Circuit mode is controlled by the $\overline{PDWN}$, $\overline{HOLD}$, and R/$\overline{W}$ pins as shown in Table 1.

TABLE 1: Mode Control

R/$\overline{W}$	$\overline{HOLD}$	
1	1	Read mode, AGC Active
1	0	Read mode AGC gain held constant*
0	X	Write mode AGC gain held constant* Input impedance reduced

* AGC gain will drift at a rate determined by BYP and Hold mode discharge current.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCC	I	+5V power supply for pulse detector
AGND	I	Analog ground pin for pulse detector block
DGND	I	Digital ground pin
IN+, IN–	I	Analog signal input pins to AGC amplifier
OUT+, OUT–	O	Read path AGC Amplifier output pins
DIN+, DIN–	I	Analog input to the hysteresis comparator
CIN+, CIN–	I	Analog input to the differentiator
DIF+, DIF–	I/O	Pins for external differentiating network
COUT	O	Test point for monitoring the flip-flop clock input. 5 kΩ resistor to GND is needed to use this pin as a test point. Leave it open in normal operation to save power dissipation.
DOUT	O	Test point for monitoring the flip-flop D-input. 5 kΩ resistor to GND is needed to use this pin as a test point. Leave it open in normal operation to save power dissipation.
$\overline{RD}$	O	TTL compatible read output
BYP	I/O	An AGC timing capacitor or network is tied between this pin and AGND1
AGC	I	Reference input voltage for the read data AGC loop
LEVEL	O	Output from fullwave rectifier that may be used for input to the hysteresis comparator
HYS	I	Hysteresis level setting input to the hysteresis comparator
$\overline{HOLD}$	I	TTL compatible pin that holds the AGC gain when pulled low
R/$\overline{W}$	I	Selects Read or Write mode

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
5V Supply Voltage, VCC	6.0V
Pin Voltage	-0.3 to VCC, + 0.3V
Storage Temperature	65 to 150°C
Lead Temperature (Soldering 10 sec.)	260°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage, VCC		4.5	5.0	5.5	V
Junction Temperature, Tj		25		135	°C
Ambient Temperature, Ta		0		70	°C

POWER SUPPLY

IVCC	Supply Current	Outputs unloaded; $\overline{PDWN}$ = high or open	19	34	42	mA
PD	Power dissipation	Ta = 25°C, outputs unloaded		170	230	mW

LOGIC SIGNALS

VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		2.0		VCC+0.3	V
IIL	Input Low Current	VIL = 0.4V	-0.4			mA
IIH	Input High Current	VIH = 2.4V			100	µA
VOL	Output Low Voltage	IOL = 4.0 mA			0.5	V
VOH	Output High Voltage	IOH = -400 µA	2.4			V

ELECTRICAL SPECIFICATIONS (continued)

MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Read to Write Transition Time	R/$\overline{W}$ pin high to low			1.0	µs
Write to Read Transition Time	R/$\overline{W}$ pin low to high AGC settling not included	0.5	0.9	1.3	µs
$\overline{HOLD}$ Off to $\overline{HOLD}$ On Transition Time	$\overline{HOLD}$ pin transitions from high to low			1.0	µs

READ MODE (R/$\overline{W}$ is high)

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN± and amplitude is between 25 mVpp & 250 mVpp differential. OUT± are loaded differentially with >600Ω, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 2000 pF capacitor is connected between BYP and AGND. AGC pin is open.

Gain Range	1.0 Vpp ≤ OUT± ≤ 3.0 Vpp	4		80	V/V
Output Offset Voltage	Over entire gain range	-200	0	+200	mV
Maximum Output	Set by BYP pin	3.0			Vpp
Voltage Swing	THD ≤ 5%				
Differential Input Resistance	IN± = 100 mVpp @ 2.5 MHz		5.0		kΩ
Differential Input Capacitance	IN± = 100 mVpp @ 2.5 MHz			10	pF
Common Mode Input	R/$\overline{W}$ = high		1.5		kΩ
Impedance	R/$\overline{W}$ = low		250		Ω
Input Noise Voltage	Gain set to maximum		5.5	15	nV/$\sqrt{Hz}$
Bandwidth	-3 dB bandwidth at maximum gain	32			MHz
OUT+ & OUT- Pin Current	No DC path to AGND		3		mA
CMRR (Input Referred)	IN± = 0 VDC + 100 mVpp @ 2.5 MHz, gain set to max	40	63		dB
PSRR (Input Referred)	100 mVpp @ 2.5 MHz on VCC, gain set to max	30	66		dB

AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DIN± Input Swing vs. AGC Input	25 mVpp ≤ IN± ≤ 250 mVpp, $\overline{HOLD}$ = high, 0.5 Vpp ≤ DIN± ≤ 1.5 Vpp	0.38	0.45	0.56	Vpp/V
DIN± Input Voltage Swing Variation	25 mVpp ≤ IN± ≤ 250 mVpp			6.0	%
AGC Voltage	AGC open	1.8	2.2	2.6	V
AGC Pin Input Impedance		3.5	3.9	5.5	kΩ
Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V	3.5	4.3	6	µA
Fast AGC Discharge Current	Starts at 0.9 µs after R/$\overline{W}$ goes high, stops at 1.8 µs after R/$\overline{W}$ goes high	70	102	150	µA
AGC Leakage Current	$\overline{HOLD}$ = low	-0.2	0	+0.2	µA
Slow AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, vary AGC until slow charge begins	-0.12	-0.17	-0.24	mA
Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, V_{AGC} = 3.0V	-0.9	-1.2	-1.7	mA
Fast to Slow Attack Switchover Point	$\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$		125		%
Gain Decay Time (Td)	IN± = 250 mVpp to 125 mVpp @ 2.5 MHz, OUT± to 90% final value		20		µs
	IN± = 50 mVpp to 25 mVpp at 2.5 MHz OUT± to 90% final value		70		µs
Gain Attack Time	R/$\overline{W}$ = low to high IN± = 250 mVpp @ 2.5 MHz, OUT± to 110% final value		2		µs

WRITE MODE (R/$\overline{W}$ is low)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Common Mode Input Impedance			250		Ω

ELECTRICAL SPECIFICATIONS (continued)

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vpp, 2.5 MHz sine wave. 0.5 VDC is applied to the HYS pin. R/$\overline{W}$ pin is high.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range		0.6	1.0	1.5	Vpp
Differential Input Resistance	DIN± = 100 mVpp @ 2.5 MHz	17.5	20	22.5	kΩ
Differential Input Capacitance	DIN± = 100 mVpp @ 2.5 MHz			5.0	pF
Common Mode Input Impedance (Both Sides)		3	4.8	5.5	kΩ
Level Pin Output Voltage vs. DIN±	0.6 Vpp < DIN± < 1.5 Vpp, 10 kΩ between LEVEL pin and AGND		1		V/Vpp
Level Pin Output Offset Voltage	10 kΩ between LEVEL pin and AGND	120	170	250	mV
Level Pin Output Impedance	I_{LEVEL} = 0.2 mA		330		Ω
Level pin Maximum Output Current		2.0			mA
Hysteresis Voltage at DIN± vs. HYS Pin Voltage	0.3 V < HYS < 1.0V		0.19		V/V
HYS Pin Input Current	0.5 V < HYS < 1.5V	-10.0		0	µA
Comparator Offset Voltage	HYS pin at AGND ≤1.5 kΩ across DIN±			5.0	mV
DOUT Pin Output Low Voltage	5 kΩ from DOUT to GND		VPA -2.8		V
DOUT Pin Output High Voltage	5 kΩ from DOUT to GND		VPA -2.4		V

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input CIN± is an AC-coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range		0.6	1.0	1.5	Vpp
Differential Input Resistance	CIN± = 100 mVpp @ 2.5 MHz	17.5	20	22.5	kΩ
Differential Input Capacitance	CIN± = 100 mVpp @ 2.5 MHz			5.0	pF
Common Mode Input Impedance	Both sides	3.5	4.5	5.5	kΩ
Voltage Gain From CIN± to DIF±	Resistor across DIF± is 2 kΩ		1		V/V
DIF+ to DIF- PIn Current	Differentiator impedance must be set so as to not clip the the signal for this current level	-0.7		0.7	mA
COUT Pin Output Low Voltage	5 kΩ from COUT to GND		VPA -2.8		V
COUT Pin Output High Voltage	5 kΩ from COUT to GND		VPA -2.4		V
COUT Pin Output Pulse Width			47		ns

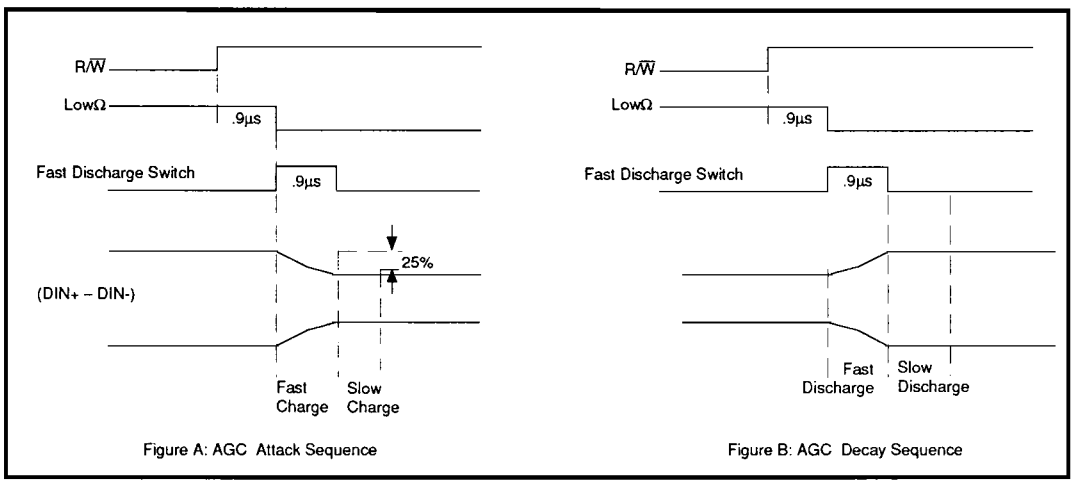


Figure A: AGC Attack Sequence

Figure B: AGC Decay Sequence

FIGURE 7: AGC Timing Diagram

ELECTRICAL SPECIFICATIONS (continued)

QUALIFIER TIMING

Unless otherwise specified, recommended operating conditions apply. Inputs CIN± and DIN± are in-place as a coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. COUT and DOUT each have a 5 kΩ pull-down resistor (for test purposes only.) R/$\overline{W}$ pin is high.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysterisis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay	From positive peak to $\overline{RD}$ output pulse		28		ns
Td4	Propagation Delay	From negative peak to $\overline{RD}$ output pulse		28		ns
|Td3-Td4|	Pulse Pairing			1.0		ns
Td5	$\overline{RD}$ Output Pulse Width	$\overline{RD}$ pin open	8		14	ns

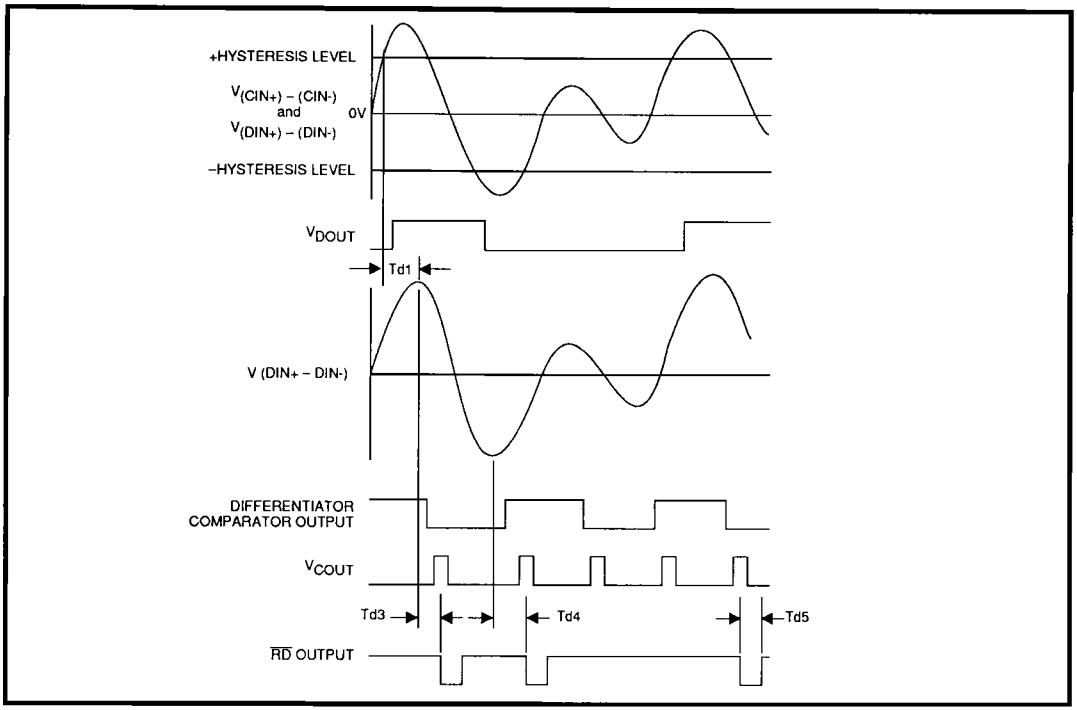
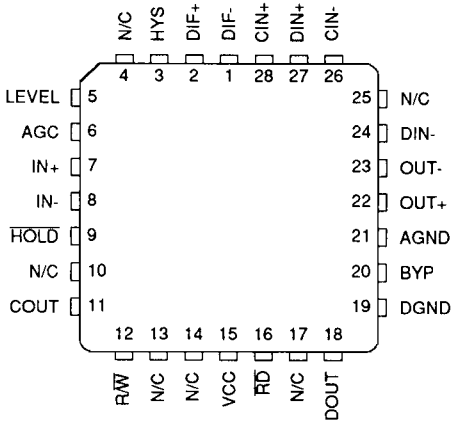


FIGURE 8: Read Mode Digital Section Timing Diagram

PACKAGE PIN DESIGNATIONS

(Top View)



28-Pin PLCC

THERMAL CHARACTERISTICS: θja

28-Pin PLCC	65°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32P541C		
28-Pin PLCC	32P541C-CH	32P541C-CH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

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Notes: