SUN MICROELECTRONICS

STP3020

July 1997

SMC

DATA SHEET — System Memory Controller

DESCRIPTION

The STP3020 System Memory controller (SMC) interfaces to an array of DRAM and VRAM SIMMs. It accelerates graphics and imaging to main memory and frame buffers. It also provides the interface for video I/O transfers to the STP3021 Memory Display Interface (MDI), STP3022 Video Buffer, DAC and Programmable Clock Generator (PCG) devices.

The STP3020 consists of two major sections: an integer vector processor and a memory controller. The integer vector processor portion takes in commands from the CPU via the MBus and can load or store to memory or manipulate data using its two ALU's and multipliers.

Features	*Benefits*
• Implements the full level-2 Mbus protocol	
• Supports a 40 or 50 MHz Mbus system	
• 128-bit memory data bus plus 16 ECC check bits for double word DRAM	• Optimum memory bandwidth
• Sustained 32B, including Mbus Arbitration and Refresh overhead, DRAM transfers of 86 MB/s	• System performance
• Interfaces to VSIMMs of various frame buffer sizes (2/4/8/16 MB) and display resolutions	• Local bus, true color graphics capable
• Supports several VRAM addressing modes for efficient pixel manipulations	• Multiple resolutions/pixel depths
• DRAM capacity ranges from 4 to 512MB using from 1Mbit to 16Mbit DRAM parts	• Flexibility
• Two can share an Mbus for a combined DRAM capacity of 1024MB	
• JTAG boundary and internal scan	• Chip fault grading and board testing

BLOCK, LOGIC AND TYPICAL APPLICATION DIAGRAMS

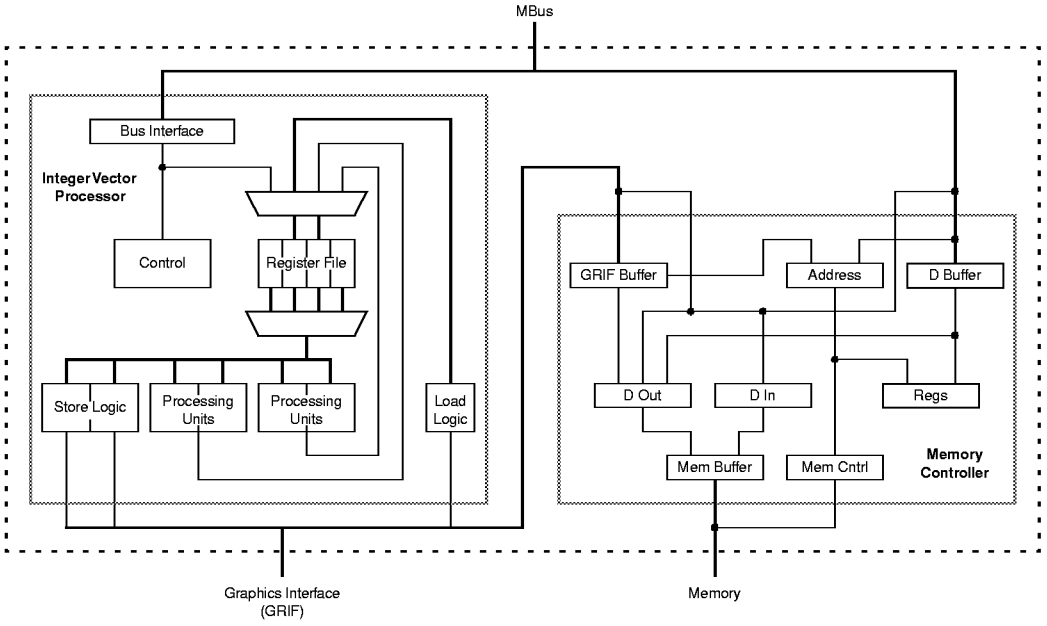


Figure 1. STP3020 Block Diagram

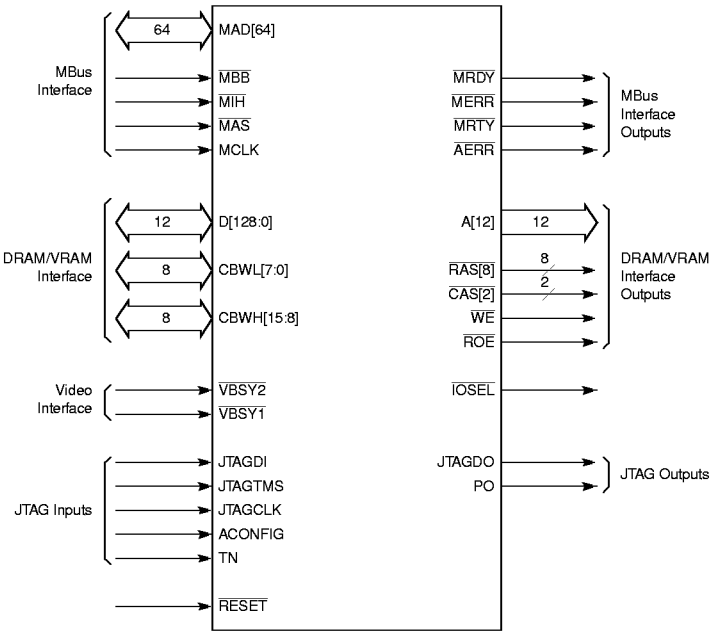


Figure 2. STP3020 Logic Symbol

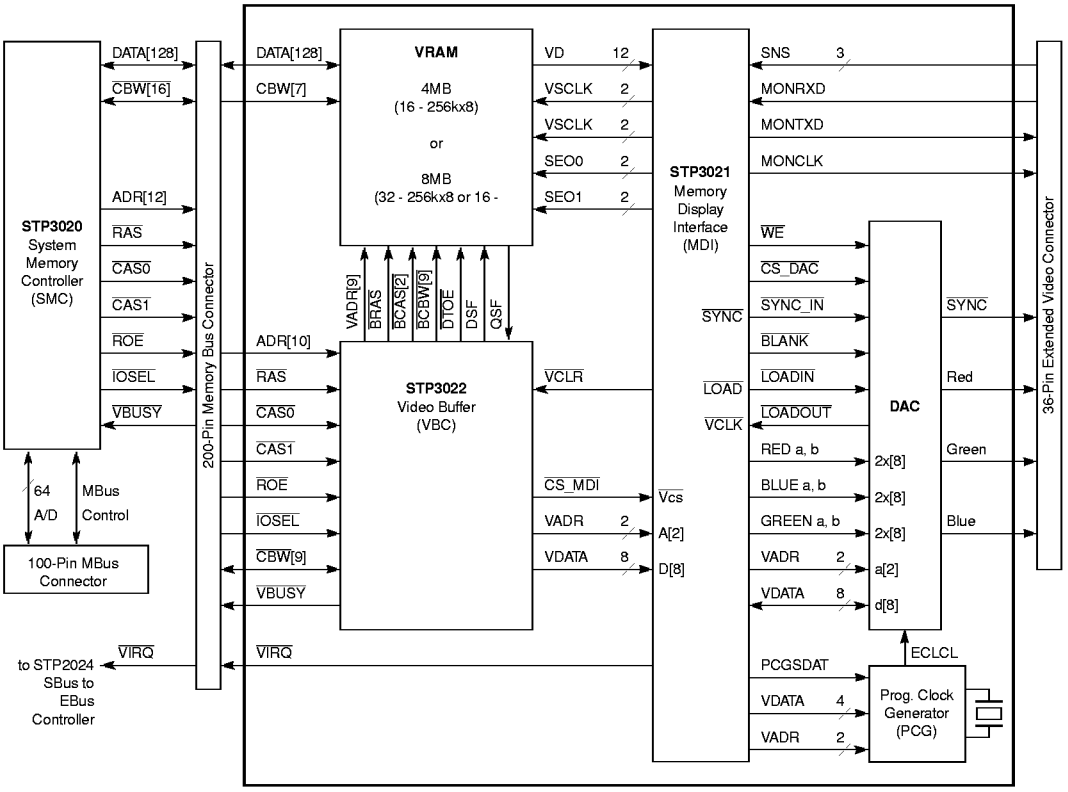


Figure 3. STP3020 Typical Application

SIGNAL DESCRIPTIONS

MBUS Interface

Signal	Type	Description
MAD[63:0]	I/O	MBus address/data bus
$\overline{\text{MAS}}$	Input	MBus address strobe
$\overline{\text{MRDY}}$	Output	MBus acknowledge
$\overline{\text{MERR}}$	Output	MBus error
$\overline{\text{MRTY}}$	Output	MBus retry
$\overline{\text{MBB}}$	Input	MBus busy
$\overline{\text{MIH}}$	Input	MBus inhibit
$\overline{\text{MCLK}}$	Input	System clock
$\overline{\text{AERR}}$	Output	Asynchronous error

Video Interface

Signal	Type	Description
$\overline{\text{VBSY0}}$	Input	Video busy from VRAM SIMMs [RAS 0,2,4,6]
$\overline{\text{VBSY1}}$	Input	Video busy from VRAM SIMMs [RAS 1,3,5,7]
$\overline{\text{IOSEL}}$	Output	VIO space qualifier

DRAM/VRAM Interface

Signal	Type	Description
D[127:0]	I/O	Memory Data.
CBWL[7:0]	I/O	Check bits for VRAM VIO Address/Data
CBWH[15:8]	I/O	Check bits for VRAM VIO Read/Write Qualifier
$\overline{\text{CAS0}}$	Output	CAS
$\overline{\text{CAS1}}$	Output	CAS
A[11:0]	Output	Muxed row/col address (4MB) address range).
$\overline{\text{RAS}}$[7:0]	Output	RAS
$\overline{\text{ROE}}$	Output	RAM Output Enable
$\overline{\text{WE}}$	Output	DRAM Write Enable

Miscellaneous

Signal	Type	Description
JTAGDI	Input	JTAG boundary scan data in
JTAGTMS	Input	JTAG boundary scan mode select
JTAGCLK	Input	JTAG clock
JTAGDO	Output	JTAG boundary scan data out
ACONFIG	Input	Address configuration
TN	Input	Test mode three-state disable
PO	Output	Parametric test output/procmon output
RESET	Input	Master reset pin

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage	5.25	V
V_I	Input voltage (any pin)	$0 \le V_{IN} \le V_{CC}$	V
P_D	Continuous power dissipation		W
T_J	Operating junction temperature	75	°C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground.

Recommended Operating Conditions

Symbol	Parameter	CPGA Package			TAB Package			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
T_A	Ambient temperature	0	–	40	0	–	60	°C
f_{OSC}	Frequency of operation	–	–	40	–	–	50	MHz
I_{CC}	Operating Current	–	0.9	–	–	1.5	–	A

DC Characteristics

Symbol	Description	Condition	Min	Max	Units
V_{IH}	High Level Input Voltage		3.32	–	V
V_{IL}	Low Level Input Voltage		–	1.57	V
V_{OH}	High Level Output Voltage	2 mA Buffer, I_{OH} = -2 mA [1]	2.4	–	V
		4 mA Buffer, I_{OH} = -4 mA [2]	2.4	–	V
		6mA Buffer, I_{OH} = -6 mA	2.4	–	V
		12 mA Buffer, I_{OH} = -12 mA	2.4	–	V
V_{OL}	Low Level Output Voltage	2 mA Buffer, I_{OL} = 2 mA [1]	–	0.4	V
		4 mA Buffer, I_{OL} = 4 mA [2]	–	0.4	V
		8 mA Buffer, I_{OL} = 8 mA [3]	–	0.4	V
I_{IL}	Input Leakage Current		–	10	µA
I_{OL}	Output Leakage Current		–	10	µA
C_{OUT}	Output Capacitance		–	45	pF
C_{IN}	Input Capacitance		–	45	pF

1. 2 mA Output Buffer Signals - D[127:0], JTAGDO, PO.
2. 4 mA Output Buffer Signals - MAD[63:0], $\overline{AERR}$, CBWL[7:0], CBWH[15;8].
3. 8 mA Output Buffer Signals - $\overline{MRDY}$, $\overline{MERR}$, $\overline{MRTY}$, A[11:0], $\overline{RAS}$[7:0], $\overline{CAS}$[1,0], $\overline{WE}$, $\overline{ROE}$, $\overline{IOSEL}$.

AC Characteristics: Input Timing (with Respect to Rising Edge of MCLK)

Parameter	Setup Time (Ts)	Hold Time (Th)	Units
$\overline{\text{MAS}}$	5.0	1.0	ns
MIH	5.0	1.0	ns
MAD Bus	5.0	1.0	ns
Memory Data Bus (DRAM reads)	0.0	0.0	ns
Memory Data Bus (VRAM reads)	0.0	0.0	ns
CBW[L/H] (DRAM reads)	0.0	0.0	ns
CBW[L/H] (VRAM reads)	0.0	0.0	ns
$\overline{\text{VBUSY0}}$	3.0	2.0	ns
$\overline{\text{VBUSY1}}$	3.0	2.0	ns
$\overline{\text{RESET}}$	2.0	2.0	ns

AC Characteristics: Output Timing (with Respect to Rising Edge of MCLK)

Parameter	Low-to- High	High-to-Low	Units
$\overline{\text{MRDY}}$	10.5	12.5	ns
$\overline{\text{MERR}}$	10.5	12.5	ns
$\overline{\text{MRTY}}$	10.5	12.5	ns
MAD Bus	17.5	17.5	ns
Memory Data Bus	24.0	24.0	ns
CBWL	20.0	24.0	ns
CBWH	20.5	21.5	ns
Memory Address Bus	18.0	21.0	ns
$\overline{\text{CAS}}$[0..1]	13.0	12.5	ns
$\overline{\text{RAS}}$[0. .7]	19.0	13.0	ns
IOSEL	10.5	12.0	ns
$\overline{\text{WE}}$	11.5	13.5	ns
$\overline{\text{ROE}}$	12.0	14.0	ns
$\overline{\text{AERR}}$	-	15.0	ns

TIMING WAVEFORMS

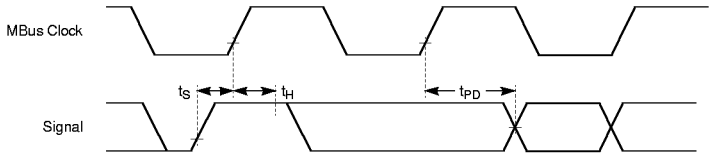


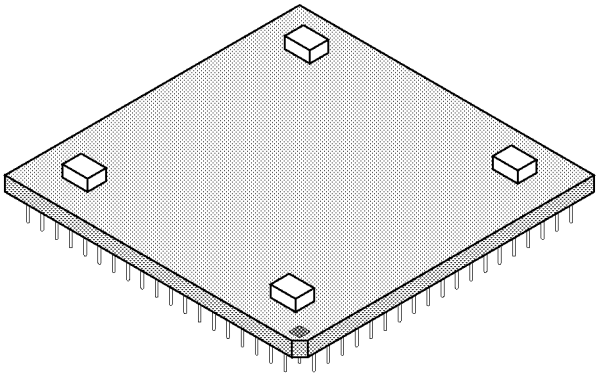
Figure 4. Timing Relationship Between MBus Clock and Signal

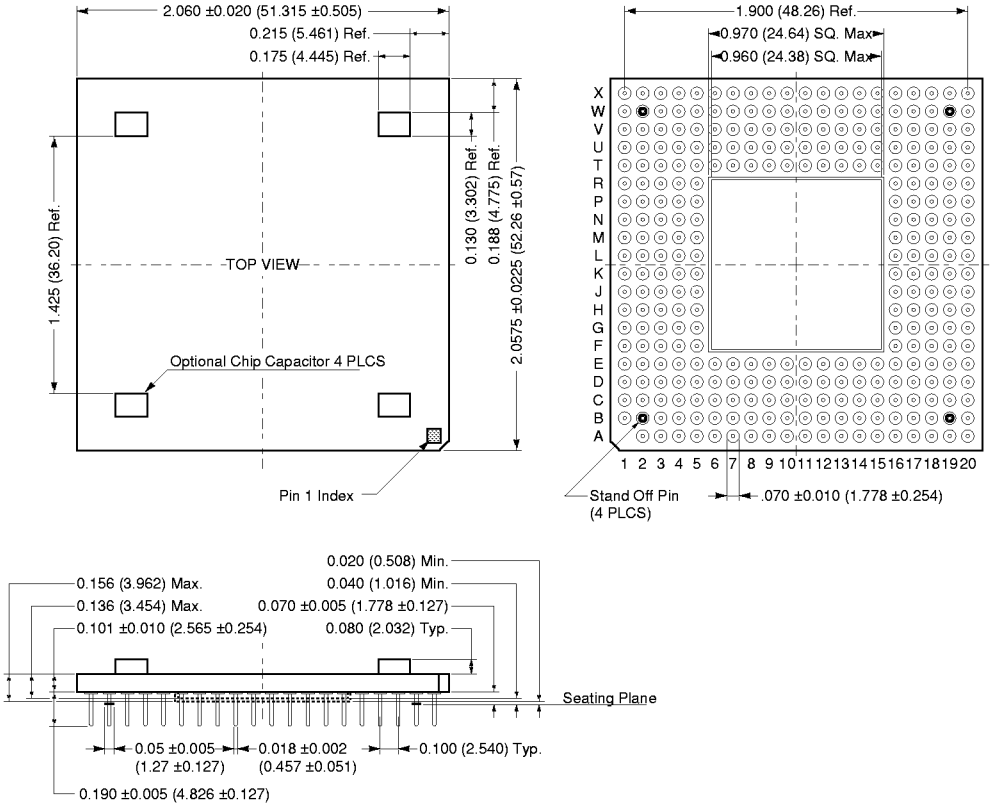
PACKAGE INFORMATION

299-Pin CPGA Package Pin Assignment

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A2	GND	C12	D<4>	F2	A<10>	L2	D<127>	T2	CBWH<14>	V12	MAD<43>
A3	VCC	C13	D<11>	F3	A<8>	L3	D<106>	T3	$\overline{\text{RAS}}$<7>	V13	MAD<57>
A4	GND	C14	D<43>	F4	CBWL<6>	L4	$\overline{\text{WE}}$	T4	$\overline{\text{RAS}}$<6>	V14	MAD<36>
A5	D<61>	C15	D<19>	F5	D<62>	L5	D<96>	T5	MAD<8>	V15	MAD<46>
A6	D<52>	C16	$\overline{\text{CAS}}$<1>	F16	D<26>	L16	D<24>	T6	MAD<10>	V16	MAD<54>
A7	D<22>	C17	D<56>	F17	CBWL<1>	L17	$\overline{\text{MBB}}$	T7	MAD<16>	V17	MAD<56>
A8	D<12>	C18	GND	F18	$\overline{\text{MRDY}}$	L18	D<77>	T8	MAD<19>	V18	GND
A9	VCC	C19	D<66>	F19	A<5>	L19	JTAGCLK	T9	MAD<27>	V19	$\overline{\text{RAS}}$<5>
A10	GND	C20	VCC	F20	D<75>	L20	VCC	T10	MAD<35>	V20	VCC
A11	VCC	D1	VCC	G1	D<117>	M1	VCC	T11	MAD<33>	W1	VCC
A12	GND	D2	VBSY0	G2	D<119>	M2	D<115>	T12	MAD<41>	W2	MAD<1>
A13	VCC	D3	CBWL<7>	G3	A<11>	M3	D<110>	T13	MAD<49>	W3	MAD<5>
A14	D<42>	D4	JTAGDI	G4	A<0>	M4	D<97>	T14	MAD<38>	W4	MAD<9>
A15	D<18>	D5	D<28>	G5	$\overline{\text{VBSY1}}$	M5	D<98>	T15	MAD<44>	W5	MAD<13>
A16	D<49>	D6	D<53>	G16	CBWL<3>	M16	D<59>	T16	MAD<50>	W6	MAD<17>
A17	D<69>	D7	D<45>	G17	A<3>	M17	D<80>	T17	CBWH<11>	W7	MAD<21>
A18	VCC	D8	D<47>	G18	A<9>	M18	D<81>	T18	CBWH<8>	W8	MAD<25>
A19	GND	D9	D<15>	G19	D<72>	M19	D<85>	T19	D<90>	W9	MAD<29>
A20	VCC	D10	D<32>	G20	D<95>	M20	GND	T20	D<92>	W10	MAD<30>
B1	VCC	D11	D<0>	H1	D<122>	N1	GND	U1	CBWH<15>	W11	MAD<32>
B2	D<108>	D12	D<1>	H2	D<118>	N2	D<120>	U2	$\overline{\text{RAS}}$<3>	W12	JTAGDO
B3	D<112>	D13	D<9>	H3	D<111>	N3	D<109>	U3	ACONFIG	W13	MAD<61>
B4	D<101>	D14	D<40>	H4	D<104>	N4	D<105>	U4	GND	W14	MAD<34>
B5	D<63>	D15	D<17>	H5	D<29>	N5	D<21>	U5	MAD<4>	W15	MAD<48>
B6	D<31>	D16	D<51>	H16	A<7>	N16	D<82>	U6	MAD<12>	W16	MAD<58>
B7	D<23>	D17	$\overline{\text{RESET}}$	H17	$\overline{\text{IOSEL}}$	N17	D<71>	U7	MAD<18>	W17	MAD<63>
B8	D<14>	D18	CBWL<0>	H18	D<78>	N18	D<76>	U8	MAD<23>	W18	MAD<60>
B9	D<7>	D19	A<1>	H19	D<73>	N19	D<83>	U9	MAD<31>	W19	MAD<62>
B10	D<38>	D20	$\overline{\text{MAS}}$	H20	GND	N20	D<88>	U10	MAD<26>	W20	GND
B11	MCLK	E1	A<6>	J1	GND	P1	D<125>	U11	MAD<37>	X1	GND
B12	D<3>	E2	A<4>	J2	D<114>	P2	D<121>	U12	MAD<45>	X2	VCC
B13	D<8>	E3	A<2>	J3	D<113>	P3	D<126>	U13	MAD<53>	X3	GND
B14	D<41>	E4	CBWL<4>	J4	D<103>	P4	D<99>	U14	MAD<40>	X4	MAD<3>
B15	D<50>	E5	D<30>	J5	D<54>	P5	$\overline{\text{RAS}}$<2>	U15	MAD<42>	X5	MAD<7>
B16	D<48>	E6	D<20>	J16	D<25>	P16	$\overline{\text{RAS}}$<0>	U16	MAD<52>	X6	MAD<11>
B17	D<70>	E7	D<46>	J17	D<58>	P17	CBWH<10>	U17	GND	X7	MAD<15>
B18	D<65>	E8	D<37>	J18	D<79>	P18	$\overline{\text{AERR}}$	U18	$\overline{\text{RAS}}$<4>	X8	VCC
B19	D<67>	E9	D<5>	J19	D<74>	P19	D<89>	U19	CBWH<9>	X9	GND
B20	GND	E10	D<2>	J20	VCC	P20	D<84>	U20	D<91>	X10	VCC
C1	GND	E11	D<34>	K1	VCC	R1	D<123>	V1	GND	X11	GND
C2	CBWL<5>	E12	D<33>	K2	D<116>	R2	D<124>	V2	$\overline{\text{ROE}}$	X12	VCC
C3	GND	E13	D<35>	K3	D<107>	R3	CBWH<13>	V3	GND	X13	MAD<47>
C4	D<102>	E14	D<10>	K4	D<100>	R4	TN	V4	MAD<0>	X14	MAD<51>
C5	D<60>	E15	D<16>	K5	D<55>	R5	MAD<6>	V5	MAD<2>	X15	MAD<55>
C6	$\overline{\text{CAS}}$<0>	E16	D<57>	K16	D<27>	R16	JTAGTMS	V6	MAD<14>	X16	MAD<59>
C7	D<44>	E17	CBWL<2>	K17	D<64>	R17	$\overline{\text{RAS}}$<1>	V7	MAD<20>	X17	GND
C8	D<36>	E18	$\overline{\text{MRTY}}$	K18	D<68>	R18	D<87>	V8	MAD<22>	X18	VCC
C9	D<13>	E19	$\overline{\text{MERR}}$	K19	D<86>	R19	D<94>	V9	MAD<24>	X19	GND
C10	D<39>	E20	$\overline{\text{MIH}}$	K20	GND	R20	D<93>	V10	MAD<28>	X20	VCC
C11	D<6>	F1	PO	L1	GND	T1	CBWH<12>	V11	MAD<39>		

299-Pin CPGA Package Dimensions



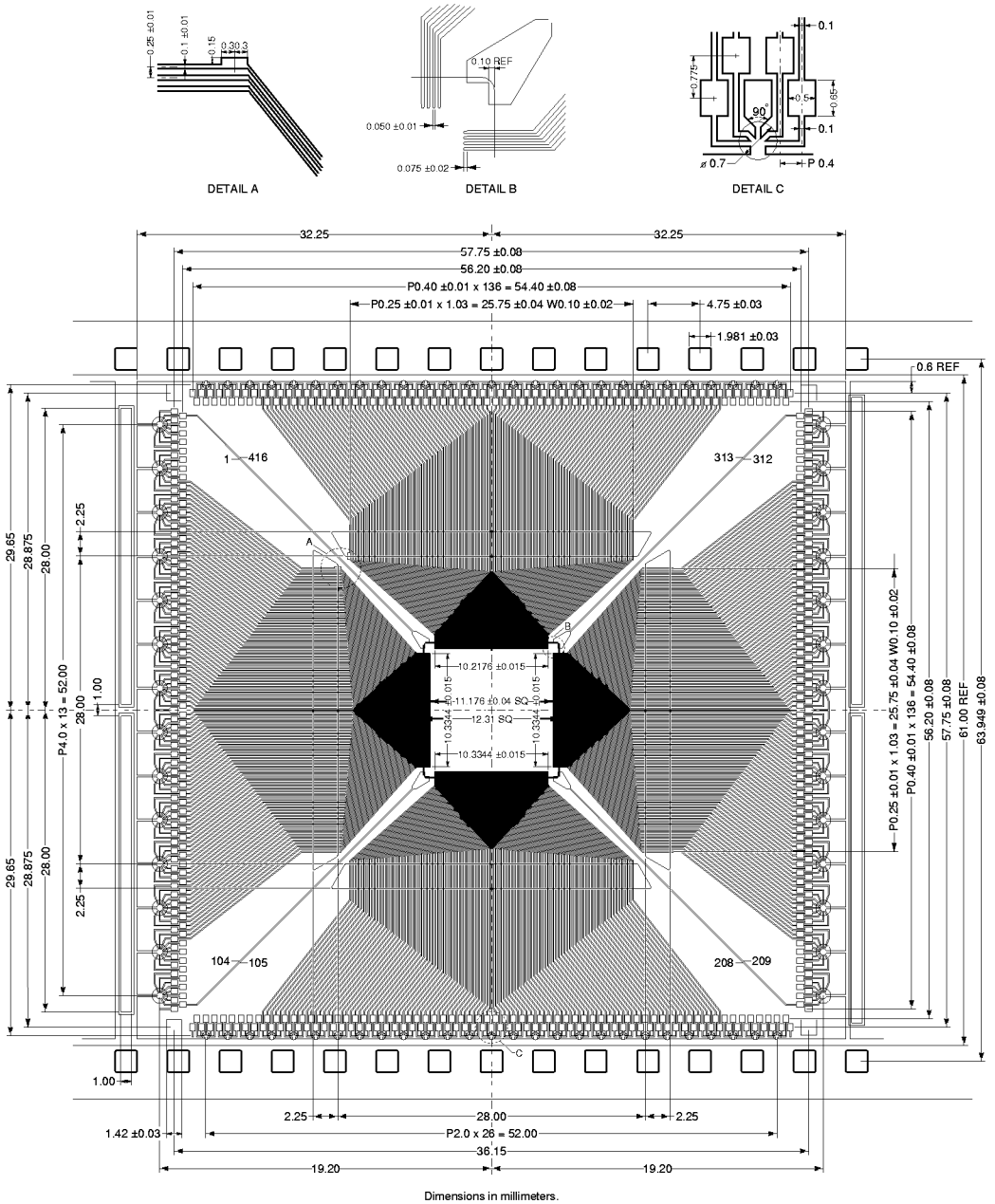


Dimensions in inches, dimensions in brackets in (millimeters).

416-Lead TAB Package Pin Assignment

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	VCC	64	D4	127	$\overline{\text{MRDY}}$	185	GND	248	MAD43	311	GND	374	D114
2	GND	66	D11	128	GND	186	D87	249	MAD57	312	VCC	375	D107
3	D30	67	D1	129	$\overline{\text{MIH}}$	187	GND	250	MAD39	313	VCC	376	D122
4	D112	68	D41	130	GND	188	D90	252	MAD61	314	GND	377	D113
5	D20	69	D33	131	A3	190	GND	253	MAD33	316	MAD8	379	D118
6	D102	70	D18	132	VCC	191	D91	254	MAD47	317	MAD1	380	D103
7	D53	71	D9	133	VCC	192	GND	255	MAD37	318	MAD6	381	D111
8	D28	72	D43	134	A5	193	CBWH8	256	JTAGD0	319	$\overline{\text{ROE}}$	382	D54
9	D46	73	D35	135	A7	196	GND	257	GND	320	TN	383	D117
10	D101	75	D50	136	A9	197	CBWH9	260	GND	321	ACONFIG	384	D104
12	GND	76	VCC	137	$\overline{\text{IOSEL}}$	198	CBWH10	261	GND	322	RAS2	385	D119
14	D60	77	VCC	139	D75	199	CBWH11	263	VCC	323	RAS6	386	D29
15	GND	78	D49	140	D25	200	$\overline{\text{RAS0}}$	265	MAD26	325	GND	387	A11
16	D63	79	GND	141	D72	202	$\overline{\text{RAS4}}$	266	MAD32	326	RAS3	388	VCC
17	GND	80	D19	142	D58	203	$\overline{\text{RAS1}}$	267	MAD35	327	GND	389	VCC
18	D61	81	GND	143	D78	204	$\overline{\text{RAS5}}$	268	MAD30	328	RAS7	390	PO
20	GND	82	D48	144	D79	205	JTAGTMS	270	MAD28	329	GND	391	GND
21	$\overline{\text{CAS\_UT0}}$	83	GND	145	D95	207	GND	271	MAD29	330	CBWH15	393	A10
22	GND	84	D69	146	D68	208	VCC	272	MAD24	333	GND	394	GND
23	D31	87	GND	147	D73	209	VCC	273	MAD25	334	CBWH14	395	A8
25	GND	88	$\overline{\text{CAS\_UT1}}$	148	D27	210	GND	274	MAD31	335	GND	396	GND
26	D45	89	GND	149	D74	211	MAD50	275	MAD15	336	CBWH13	397	A6
28	GND	90	D70	150	D64	212	MAD62	276	MAD27	337	GND	399	GND
29	D52	91	GND	151	D86	213	MAD44	277	MAD22	338	CBWH12	400	A4
30	VCC	92	D51	152	GND	215	MAD60	278	MAD23	340	GND	401	GND
31	D44	93	D40	156	GND	216	MAD42	279	MAD21	341	D99	402	A2
32	D37	95	D56	157	GND	217	MAD56	280	MAD19	342	VCC	403	A0
33	D23	96	D10	158	GND	218	MAD38	281	MAD11	343	VCC	405	$\overline{\text{VBSY0}}$
34	D47	97	D65	159	VCC	220	MAD52	282	VCC	344	D124	406	$\overline{\text{VBSY1}}$
36	D22	99	D17	160	$\overline{\text{MBB}}$	221	GND	283	VCC	345	D21	407	CBWL7
37	D5	100	D67	161	JTAGCLK	222	MAD63	284	MAD20	346	D126	408	CBWL6
38	D36	102	D16	162	D24	223	GND	285	GND	347	D105	410	CBWL5
39	D15	103	$\overline{\text{RESET}}$	163	D85	224	MAD54	287	MAD17	349	D123	411	CBWL4
40	D14	104	VCC	165	D77	225	GND	288	GND	350	D98	412	D108
41	D13	105	VCC	166	D88	228	MAD58	289	MAD7	351	D121	413	D62
42	D12	106	VCC	167	D81	229	GND	290	GND	352	D97	415	JTAGDI
43	D39	107	GND	168	D83	230	MAD59	291	MAD14	353	D109	416	VCC
45	D7	109	D57	169	D80	231	GND	292	GND	354	D110		
46	D2	110	D66	170	D84	232	MAD46	293	MAD13	355	D125		
47	D38	111	D26	171	D59	234	GND	295	GND	356	D106		
48	D32	112	CBWL0	172	D76	235	MAD48	296	MAD3	357	D120		
50	VCC	113	CBWL1	174	D71	236	VCC	297	GND	358	D96		
52	GND	114	CBWL2	175	D89	237	VCC	298	MAD2	359	D115		
53	GND	115	CBWL3	176	D82	238	MAD40	299	GND	360	$\overline{\text{WE}}$		
55	GND	116	A1	177	D93	239	MAD49	300	MAD9	362	VCC		
56	MCLKSMC	118	GND	178	VCC	240	MAD55	301	MAD18	363	GND		
57	D0	119	$\overline{\text{MRTY}}$	179	VCC	241	MAD53	302	MAD4	364	GND		
58	D3	120	GND	180	$\overline{\text{AERR}}$	242	MAD36	303	MAD16	365	GND		
59	D34	121	$\overline{\text{MAS}}$	181	GND	243	MAD41	306	MAD0	370	D127		
61	D8	123	GND	182	D94	244	MAD34	307	MAD12	371	D100		
62	D6	125	$\overline{\text{MERR}}$	183	GND	245	MAD45	308	MAD5	372	D116		
63	D42	126	GND	184	D92	247	MAD51	309	MAD10	373	D55		

416-Lead TAB Package Dimensions



ORDERING INFORMATION

Part Number	Description
STP3020PGA	299-Pin Pin Grid Array (PGA)
STP3020TAB	416-Lead Chip on Tape (TAB)

Document Part Number: STP3020