

54F/74F195

4-Bit Parallel Access Shift Register

Description

The functional characteristics of the 'F195 4-Bit Parallel Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

The 'F195 operates on two primary modes: shift right (Q_0 - Q_1) and parallel load, which are controlled by the state of the Parallel Enable (\overline{PE}) input. Serial data enters the first flip-flop (Q_0) via the J and \overline{K} inputs when the \overline{PE} input is HIGH, and is shifted 1 bit in the direction Q_0 - Q_1 - Q_2 - Q_3 following each LOW-to-HIGH clock transition. The J and \overline{K} inputs provide the flexibility of the JK type input for special applications and, by tying the two pins together, the simple D-type input for general applications. The device appears as four common clocked D flip-flops when the \overline{PE} input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (D_0 - D_3) is transferred to the respective Q_0 - Q_3 outputs. Shift left operation (Q_3 - Q_2) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the \overline{PE} input LOW.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The 'F195 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, \overline{K} , D_n , and \overline{PE} inputs for logic operation, other than the setup and release time requirements.

A LOW on the asynchronous Master Reset (\overline{MR}) input sets all Q outputs LOW, independent of any other input condition.

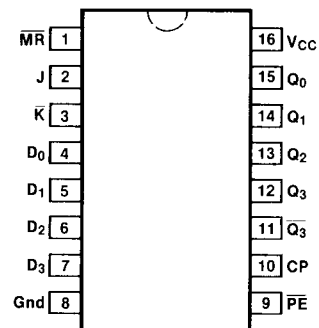
- Shift Right and Parallel Load Capability
- J- \overline{K} (D-Type) Inputs to First Stage
- Complement Output from Last Stage
- Asynchronous Master Reset

Ordering Code: See Section 5

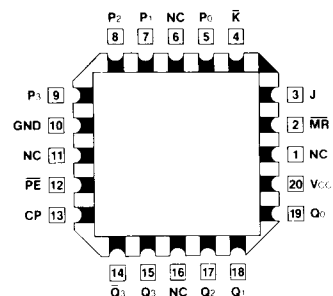
Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
D_0 - D_3	Parallel Data Inputs	0.5/0.375
\overline{PE}	Parallel Enable Input	0.5/0.375
\overline{MR}	Asynchronous Master Reset	0.5/0.375
J, \overline{K}	J- \overline{K} or D Type Serial Inputs	0.5/0.375
Q_0 - Q_3 , \overline{Q}_3	Outputs	25/0.375

Connection Diagrams

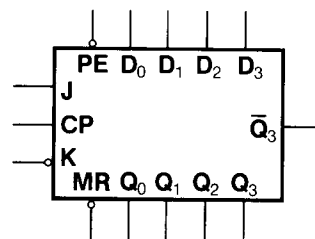


**Pin Assignment
for DIP and SOIC**



**Pin Assignment
for LCC and PCC**

Logic Symbol



Mode Select-Function Table

Operating Modes	Inputs						Outputs				
	MR	CP	PE	J	\bar{K}	D_n	Q ₀	Q ₁	Q ₂	Q ₃	\bar{Q}_3
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	↑	h	h	h	X	H	q ₀	q ₁	q ₂	\bar{q}_2
Shift, Reset First Stage	H	↑	h	l	l	X	L	q ₀	q ₁	q ₂	\bar{q}_2
Shift, Toggle First Stage	H	↑	h	h	l	X	\bar{q}_0	q ₀	q ₁	q ₂	\bar{q}_2
Shift, Retain First Stage	H	↑	h	l	h	X	q ₀	q ₀	q ₁	q ₂	\bar{q}_2
Parallel Load	H	↑	l	X	X	d_n	d ₀	d ₁	d ₂	d ₃	\bar{d}_3

H = HIGH Voltage Level

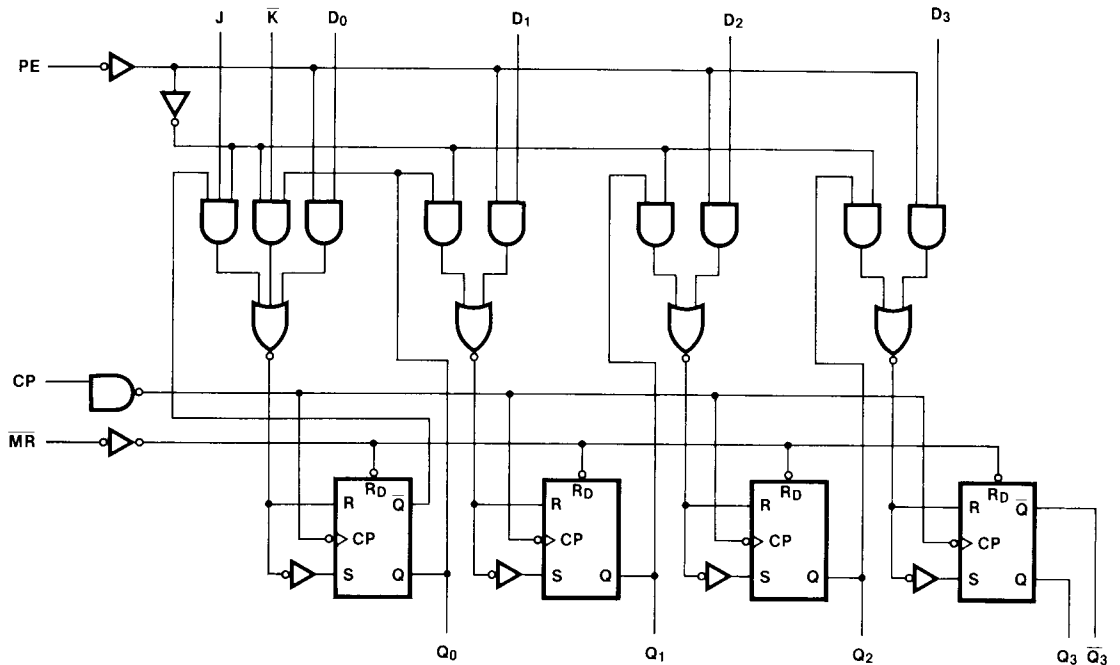
L = LOW Voltage Level

X = Immaterial

Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.

↑ = LOW-to-HIGH clock transition.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current				mA	$V_{CC} = \text{Max}$

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	105	150					MHz	3-1	
t_{PLH} t_{PHL}	Propagation Delay Clock to Output			7.0				ns	3-1 3-7	
t_{PHL}	Propagation Delay $\overline{\text{MR}}$ to Output			12.0				ns	3-1 3-11	

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$			$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{\text{s(H)}}$ $t_{\text{s(L)}}$	Setup Time, HIGH or LOW J, $\overline{\text{K}}$ and D_n to CP	4.0		4.0				ns	3-5	
$t_{\text{h(H)}}$ $t_{\text{h(L)}}$	Hold Time, HIGH or LOW J, $\overline{\text{K}}$ or D_n to CP	0		0				ns	3-5	
$t_{\text{s(H)}}$ $t_{\text{s(L)}}$	Setup Time, HIGH or LOW $\overline{\text{PE}}$ to CP	8.0		8.0				ns	3-14	
$t_{\text{h(H)}}$ $t_{\text{h(L)}}$	Hold Time, HIGH or LOW $\overline{\text{PE}}$ to CP	0		0				ns	3-14	
$t_{\text{w(H)}}$	Clock Pulse Width, HIGH	5.0						ns	3-7	
$t_{\text{w(L)}}$	$\overline{\text{MR}}$ Pulse Width, LOW	5.0						ns	3-11	
t_{rec}	Recovery Time, $\overline{\text{MR}}$ to CP	7.0						ns	3-11	