ISI IDEAL SEMICONDUCTOR INC.
"Your Best Defense Against Obsolescence"

373
54HCTLS
74HCTLS

OBJECTIVE SPECIFICATIONS

Octal D-Type Transparent Latches with 3-State Outputs

Features

- 8 latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compatability with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industial and military temperature ranges:

  74HCTLS: -40°C to +85°C
  54HCTLS: -55°C to +125°C

Description

The '373 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

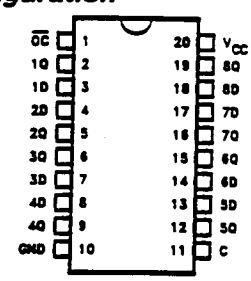
The latches are transparent: when the enable (C) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal ($\overline{OC}$) which places the outputs at a high-impedance state when it is taken high. The $\overline{OC}$ signal does not effect the internal operations of the latches. Old data can be retrained or new data can be entered while outputs are off.

Fabrication using ISI proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Configuration



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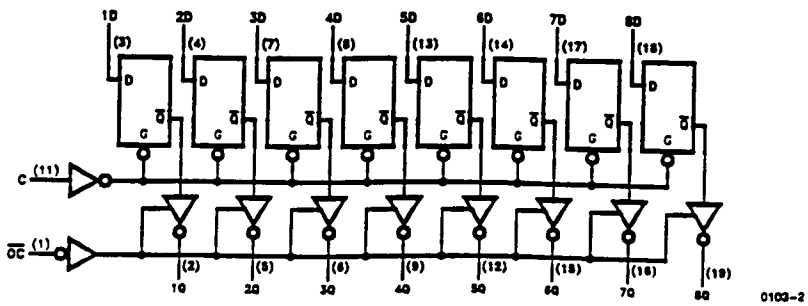
Function Table

(Each Latch)

Inputs			Output
$\overline{OC}$	Enable C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Logic Diagram



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Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} .....-0.5V to 7V
DC Input Diode Current, I_{IK}
(V_I<-0.5V or V_I>V_{CC} + 0.5V).....±20 mA
DC Output Diode Current, I_{OK}
(V_O<-0.5V or V_O>V_{CC} + 0.5V).....±20 mA
Continuous Output Current Per Pin, I_O
(-0.5V<V_O<V_{CC} + 0.5V).....±70 mA
Continuous Current Through
V_{CC} or GND pins.....±250 mA
Storage Temperature Range, T_{STG} .....-65°C to +150°C
Power Dissipation Per Package, P_D .....500 mW

*Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Power Dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} .....4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} .....0V to V_{CC}

Operating Temperature

Range 74HCTLS: -40°C to +85°C
54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f .....Max 500 ns

*Unused inputs must always to tied to an appropriate logic voltage level (either V_{CC} or GND)

DC Electrical Characteristics (V_{CC} = 5V ±10% Unless Otherwise Specified)

Sym	Parameter	Test Conditions	T_A = 25°C	74HCTLS T_A = -40°C to +85°C	54HCTLS T_A = -55°C to +125°C	Unit
			Typ	Guaranteed Limits		
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_O = -20 µA I_O = -6 uA	V_{CC} 4.2	V_{CC} -0.1 3.98	V_{CC} -0.1 3.84	V_{CC} -0.1 3.7	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}= V_{IH} or V_{IL} I_O = 20 µA I_O = 12 mA I_O = 24 mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	µA
I_{OZ}	Maximum 3-State Leakage Current	Output Enable = V_{IH} V_{OUT} = V_{CC} or GND		±0.5	±5.0	±10.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 µA		8.0	80.0	160.0	µA

AC Electrical Characteristics (Input t_r, $t_f \leq 6$ ns), HCTLS373

Sym	Parameter	Conditions •	T_A = 25°C VCC - 5.0V	74HCTLS T_A = -40°C to +85°C V_{CC} = 5.0V ±10%	54HCTLS T_A = -55°C to +125°C V_{CC} = 5.0V ±10%	Unit
			Typ	Guaranteed Limits		
t_{PLH}	Maximum Propagation Delay, D to Q	C_L = 50 pF	14	18	23 / 27	ns
		C_L = 150 pF	20	25	32 / 38	
t_{PHL}		C_L = 50 pF	14	18	23 / 27	
		C_L = 150pF	20	25	32 / 38	
t_{PLH}	Maximum Propagation Delay, C to any Q	C_L = 50 pF	22	30	37 / 45	ns
		C_L = 150 pF	28	37	46 / 56	
t_{PHL}		C_L = 50 pF	22	30	37 / 45	
		C_L = 150 pF	28	37	46 / 56	
t_{PZH}	Maximum Output Enable Time, $\overline{OC}$ to any Q	R_L = 1kΩ, C_L = 50 pF	24	32	40 / 48	ns
		C_L = 150 pF	30	39	49 / 59	
t_{PZL}		C_L = 50 pF	24	32	40 / 48	
		C_L = 150 pF	30	39	49 / 59	
t_{PHZ}	Maximum Output Disable Time, $\overline{OC}$ to any Q	R_L = 1kΩ	19	25	31 / 37	ns
t_{PLZ}		C_L = 50 pF	19	25	31 / 37	
t_w	Minimum Pulse Width, C High		6	10	12 / 15	ns
t_{su}	Minimum Setup Time, D before C↓		2	3	4 / 5	ns
t_h	Minimum Hold Time, D after C↓		6	10	12 / 15	ns
C_{IN}	Maximum Input Capacitance		5			pF
C_{OUT}	Maximum Output Capacitance	Output Disabled	10			pF
C_{PD}	Power Dissipation Capacitance* (per stage)	$\overline{OC}$ = V_{CC}	5			pF
		$\overline{OC}$ = GND	30			

*C_{PD} determines the no-load dynamic power consumption: $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$
•For AC switching test circuits and timing waveforms see section 2.