POWER LOGIC CMOS QUAD DRIVERS

FEATURES

- Tough CMOS™ Construction
- Latchproof! Withstands 500 mA Inductive Kickback
- 3 Input Logic Choices
  - — AND/NAND/AND+Inv
- 4 Output Structures
  - — Pull-Up/Pull-Down/Totem Pole/ Pull-Down with Clamp Diode
- Inverting or Non-Inverting Outputs
- Symmetrical Rise and Fall Times .....25 ns
- Short, Equal Delay Times .....75 ns
- High Peak Output Current 1.2A
- Wide Operating Range .....4.5 to 18V
- Inputs = Logic 1 for Any Input From 2.4V to V_{DD}
- 2 kV ESD Protection on All Pins

APPLICATIONS

- General-Purpose CMOS Logic Buffer
- Driving All Four MOSFETs in an H-Bridge
- Direct Small Motor Driver
- Relay or Peripheral Drivers
- Dual Differential Output Power Drivers
- CCD Driver
- Pin-Switching Network Driver
- LED Driver
- High Side Switch

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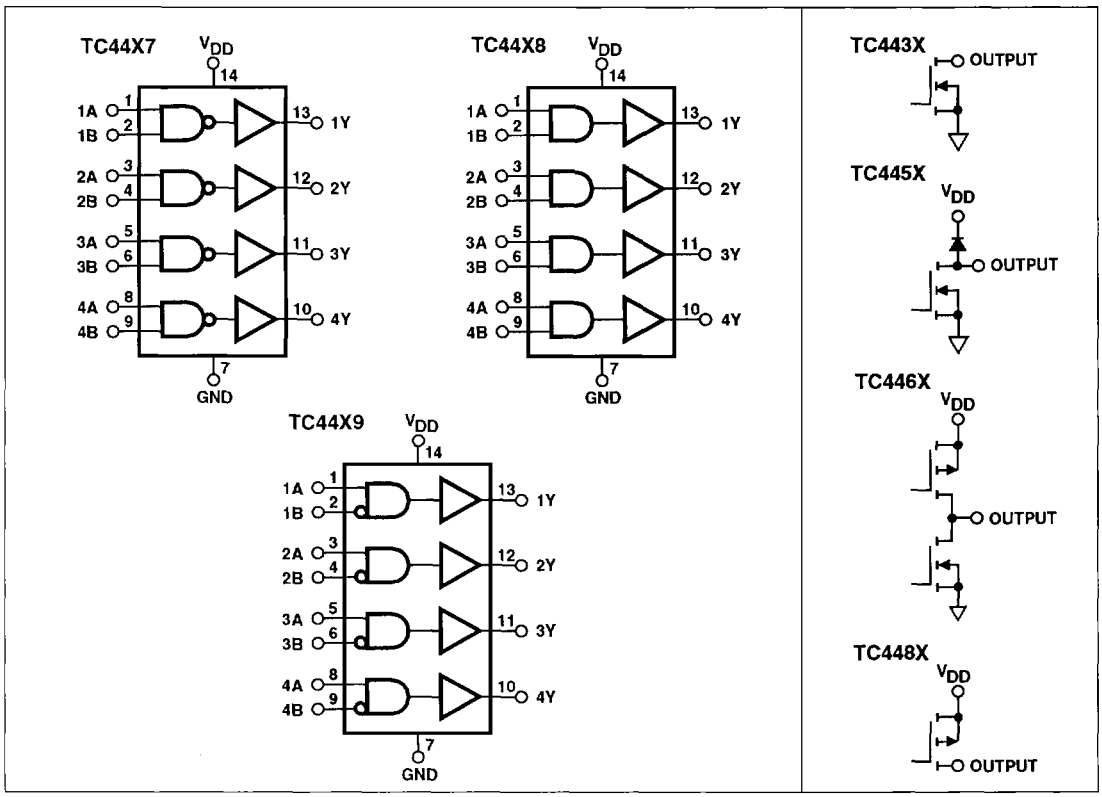
LOGIC DIAGRAMS



TC4437/8/9 TC4467/8/9
TC4457/8/9 TC4487/8/9

GENERAL DESCRIPTION

The TC44XX family of four-output CMOS buffer/drivers are an expansion from our earlier single- and dual-output drivers. Each driver has been equipped with a two-input logic gate for added flexibility. Four output configurations have also been provided, so high-efficiency CMOS drivers can be used whether the application requires a totem-pole output or pull-up/pull-down output, or pull-down with a clamp diode. These different input and output combinations make these Power Logic™ drivers well suited for a wide range of applications.

Although commonly used for driving power MOSFETs and similar highly capacitive loads, these drivers are equally well suited to driving any other load (capacitive, resistive, or inductive) which requires a high efficiency, low-impedance driver capable of high peak currents, rail-to-rail voltage swings, and fast switching times. For example, relays and solenoids can be driven with the 445X driver which contains an internal clamp diode which will shunt inductive flybacks back to the supply. The 443X driver provides a fast, low impedance path to ground for devices referenced to the upper supply rail like indicators, sounders or pin drivers. The 448X driver can source up to 250 mA into loads referenced to ground. Heavily loaded clock lines, coaxial cables, and piezoelectric transducers can all be driven easily with the 44XX series drivers. The only limitation on loading is that total power dissipation in the IC must be kept within the power dissipation limits of the package.

The TC44XX series drivers are built using Teledyne Component's new Tough CMOS process, which makes them easy and forgiving parts to use; capable of giving reliable service in very demanding operating environments. They will not latch under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (either polarity) occurs on the ground line. They can accept up to half an amp of inductive kickback current (either polarity) into their outputs without damage or logic upset. In addition, all terminals are protected against ESD to at least 2000V. Even the molding epoxy used on our plastic packages has been custom developed to contain less sodium and chlorine contamination than standard commercial molding compounds. In tests, it demonstrated zero device failures after 10,000 hours in an 85°C, 85% relative humidity environment.

ORDERING INFORMATION

Part No.	Package	Temp. Range
TC44**CPD	14-Pin Plastic DIP	0° to +70°C
TC44**COE	16-Pin Wide SOIC	0° to +70°C
TC44**EPD	14-Pin Plastic DIP	–40° to +85°C
TC44**EOE	16-Pin Wide SOIC	–40° to +85°C
TC44**EJD	14-Pin CerDIP	–40° to +85°C
TC44**MJD	14-Pin CerDIP	–55° to +125°C

**Two digits must be added in this position to define the device input and output configuration: TC44XX

3 Pull-Down	7 NAND
5 Pull-Down with Clamp Diode	8 AND
6 Pull-Up and Down	9 AND with INV
8 Pull-Up	

The first digit represents output structure. The second digit represents input logic. *Example:* TC4487 has a pull-up output and a NAND input.

TRUTH TABLE

Part No.	Inputs A	Inputs B	Outputs 443X	Outputs 445X	Outputs 446X	Outputs 448X
TC44*7	H	H	L	L	L	F
NAND	H	L	F	F	H	H
	L	H	F	F	H	H
	L	L	F	F	H	H
TC44*8	H	H	F	F	H	H
AND	H	L	L	L	L	F
	L	H	L	L	L	F
	L	L	L	L	L	F
TC44*9	H	H	L	L	L	F
AND/	H	L	F	F	H	H
INV	L	H	L	L	L	F
	L	L	L	L	L	F

H = High L = Low F = Floating

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +20V
Input Voltage ..... (GND – 5V) to (V_{DD} + 0.3V)
Maximum Chip Temperature
  Operating ..... +150°C
  Storage ..... –65° to +150°C
Maximum Lead Temperature
  (Soldering, 10 sec) ..... +300°C
Operating Ambient Temperature Range
  C Device ..... 0° to +70°C
  E Device ..... –40° to +85°C
  M Device ..... –55° to +125°C
Power Dissipation
  JD Package (14-Pin CerDIP) 1.25W
  PD Package (14-Pin Plastic DIP) 1.5W
  OE Package (16-Pin Wide SOIC) 1W

Package Thermal Resistance

JD Package (14-Pin CerDIP)	$R_{\theta J-A}$	10 mW/°C
	$R_{\theta J-C}$	45 mW/°C
PD Package (14-Pin Plastic DIP)	$R_{\theta J-A}$	12 mW/°C
	$R_{\theta J-C}$	20 mW/°C
OE Package (16-Pin Wide SOIC)	$R_{\theta J-A}$	8 mW/°C
	$R_{\theta J-C}$	31 mW/°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

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ELECTRICAL CHARACTERISTICS: Measured at T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage	Note 3	2.4		V_{DD}	V
V_{IL}	Logic 0, Low Input Voltage	Note 3	0		0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–1		1	µA
Output						
V_{OH}	High Output Voltage	I_{LOAD} = 10 mA (Note 1)	V_{DD} –0.15			V
V_{OL}	Low Output Voltage	I_{LOAD} = 10 mA (Note 1)			0.15	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V		10	15	Ω
I_{PK}	Peak Output Current			1.2		A
I_{DC}	Continuous Output Current	Single Output Total Package			300 500	mA mA
I	Latch-Up Protection Withstand Reverse Current	4.5V ≤ V_{DD} ≤ 16V	500			mA
Switching Time						
t_R	Rise Time	Figure 1		15	25	ns
t_F	Fall Time	Figure 1		15	25	ns
t_{D1}	Delay Time	Figure 1		40	75	ns
t_{D2}	Delay Time	Figure 1		40	75	ns
Power Supply						
I_S	Power Supply Current			1.5	4	mA
V_{DD}	Power Supply Voltage	Note 2	4.5		18	V

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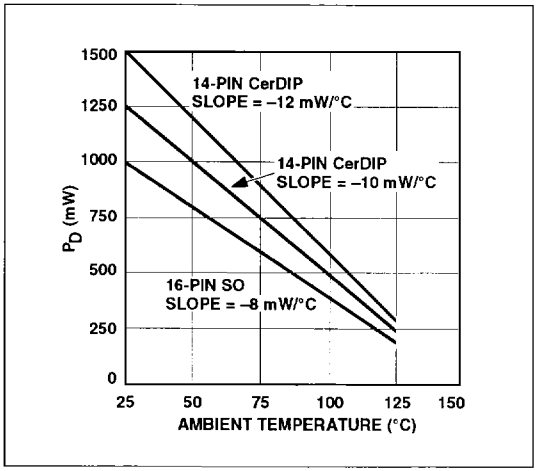
ELECTRICAL CHARACTERISTICS:

Measured throughout operating temperature range with $4.5V \leq V_{DD} \leq 18V$, unless otherwise specified.

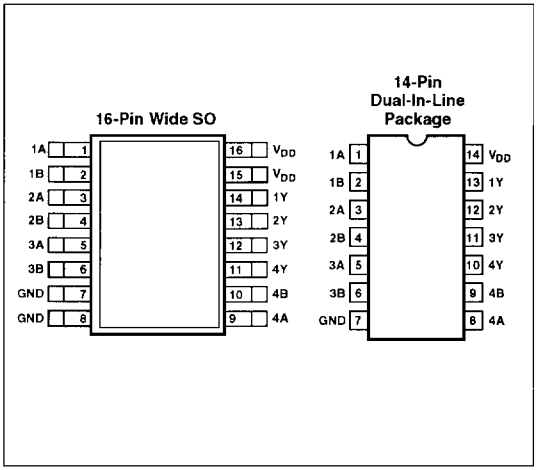
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage	(Note 3)	2.4			V
V_{IL}	Logic 0, Low Input Voltage	(Note 3)			0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	−1		1	µA
Output						
V_{OH}	High Output Voltage	I_{LOAD} = 10 mA (Note 1)	V_{DD} −0.30			V
V_{OL}	Low Output Voltage	I_{LOAD} = 10 mA (Note 1)			0.30	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V		20	30	Ω
I_{PK}	Peak Output Current			1.2		A
I	Latch-Up Protection Withstand Reverse Current	$4.5V \leq V_{DD} \leq 16V$	500			mA
Switching Time						
t_R	Rise Time	Figure 1			50	ns
t_F	Fall Time	Figure 1			50	ns
t_{D1}	Delay Time	Figure 1			100	ns
t_{D2}	Delay Time	Figure 1			100	ns
Power Supply						
I_S	Power Supply Current				8	mA
I_S	Power Supply Voltage	Note 2	4.5		18	V

NOTES:
1. Totem-pole outputs should not be paralleled because the propagation delay differences from one to the other could cause one driver to drive high a few nanoseconds before another. The resulting current spike, although short, may decrease the life of the device.
2. When driving all four outputs simultaneously in the same direction, V_{DD} shall be limited to 16V. This reduces the chance that internal dv/dt will cause high-power dissipation in the device.
3. The input threshold has about 50 mV of hysteresis centered at approximately 1.5V. Slow moving inputs will force the device to dissipate high peak currents as the input transitions through this band. Input rise times should be kept below 5 µs to avoid high internal peak currents during input transitions. Static input levels should also be maintained above the maximum or below the minimum input levels specified in the "Electrical Characteristics" to avoid increased power dissipation in the device.

PACKAGE POWER DISSIPATION



PIN CONFIGURATIONS



Supply Bypassing

Large currents are required to charge and discharge large capacitive loads quickly. For example, charging a 1000 pF load 18V in 25 ns requires a 0.8A current from the device's power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (<0.5 in.) should be used. A 1 µF film capacitor in parallel with one or two 0.1 µF ceramic disk capacitors normally provides adequate bypassing.

Grounding

The TC44X7 and TC44X9 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for input and output circuits or a ground plane should be used.

Input Stage

The input voltage level changes the no load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. With logic "0" outputs, maximum quiescent supply current is 4 mA. Logic "1" output level signals reduce quiescent current to 1.4 mA maximum. Unused driver inputs must be connected to V_{DD} or V_{SS}. Minimum power dissipation occurs for logic "1" outputs.

The drivers are designed with 50 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V, making Logic 1 input any voltage greater than 1.5V up to V_{DD}. Input current is less than 1 µA over this range.

Power Dissipation

The supply current versus frequency and supply current versus capacitive load characteristic curves will aid in determining power dissipation calculations.

Teledyne Components' CMOS drivers have greatly reduced quiescent DC power consumption. Maximum quiescent current is 4 mA, compared to the D469's 20 mA specification.

Input signal duty cycle, power supply voltage, and load type influence package power dissipation. Given power dissipation and package thermal resistance, the maximum ambient operation temperature is easily calculated. The 14-pin plastic package junction-to-ambient thermal resistance is 83.3°C/W. At +25°C, the package is rated at 1500 mW maximum dissipation. Maximum allowable chip temperature is +150°C.

Three components make up total package power dissipation:

(1) Load caused dissipation (P_L)
(2) Quiescent power (P_Q)
(3) Transition power (P_T).

A capacitive-load-caused dissipation (driving MOSFET gates), is a direct function of frequency, capacitive load, and supply voltage. The power dissipation is:

$$P_L = f\,C\,V_S^2,$$

where: f = Switching frequency
C = Capacitive load
V_S = Supply voltage.

A resistive-load-caused dissipation for ground-referenced loads is a function of duty cycle, load current, and load voltage. The power dissipation is:

$$P_L = D\,(V_S - V_L)\,I_L,$$

where: D = Duty cycle
V_S = Supply voltage
V_L = Load voltage
I_L = Load current.

A resistive-load-caused dissipation for supply-referenced loads is a function of duty cycle, load current, and output voltage. The power dissipation is:

$$P_L = D\,V_O\,I_L,$$

where: f = Switching frequency
V_O = Device output voltage
I_L = Load current.

Quiescent power dissipation depends on input signal duty cycle. Logic high outputs result in a lower power dissipation mode with only 0.6 mA total current drain (all devices driven). Logic low outputs raise the current to 4 mA maximum. The quiescent power dissipation is:

$$P_Q = V_S\,(D(I_H) + (1-D)I_L),$$

where: I_H = Quiescent current with all outputs low (4 mA max)
I_L = Quiescent current with all outputs high (0.6 mA max)
D = Duty cycle
V_S = Supply voltage.

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Transition power dissipation arises in the totem-pole configuration (TC446X) because the output stage N-channel and P-channel MOS transistors are ON simultaneously for a very short period when the output changes. The transition power dissipation is approximately:

$P_T = f\ V_S\ (10 \times 10^{-9})$.

Package power dissipation is the sum of load, quiescent and transition power dissipations. An example shows the relative magnitude for each term:

C = 1000 pF capacitive load
V_S = 15V
D = 50%
f = 200 kHz
P_D = Package Power Dissipation = $P_L + P_Q + P_T$
= 45 mW + 35 mW + 30 mW = 110 mW.

Maximum operating temperature:

$T_J - \theta_{JA}\ (P_D) = 141°C$,

where: T_J = Maximum allowable junction temperature (+150°C)
θ_{JA} = Junction-to-ambient thermal resistance (83.3°C/W) 14-pin plastic package.

NOTE: Ambient operating temperature should not exceed +85°C for "EJD" device or +125°C for "MJD" device.

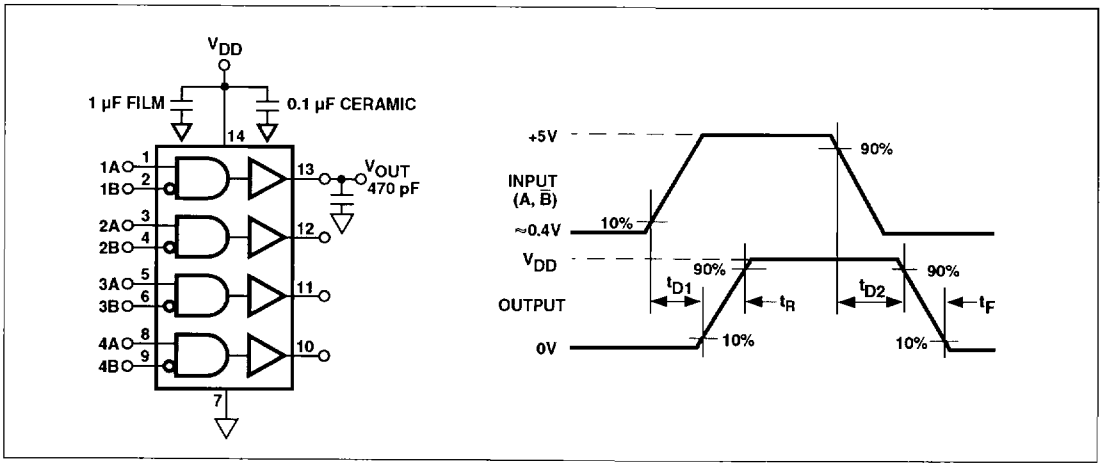
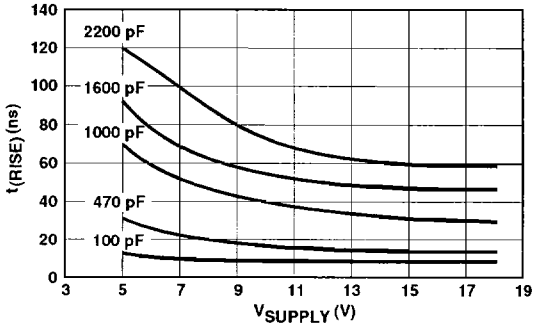


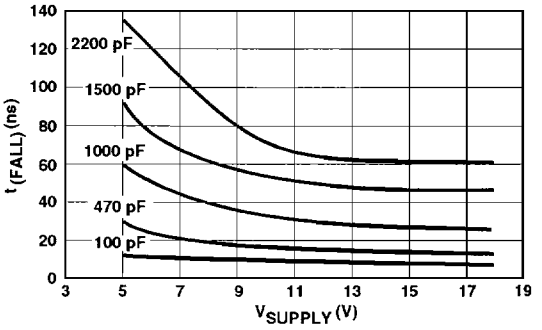
Figure 1 Switching Time Test Circuit

CHARACTERISTICS CURVES

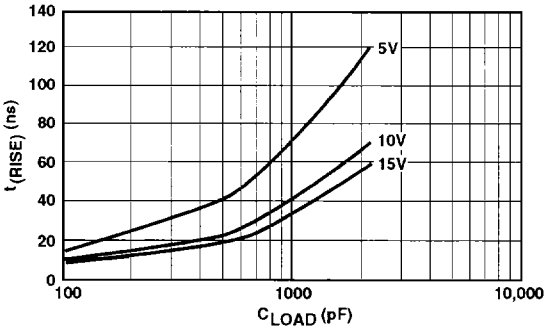
Rise Time vs Supply Voltage
(TC446X, TC448X)



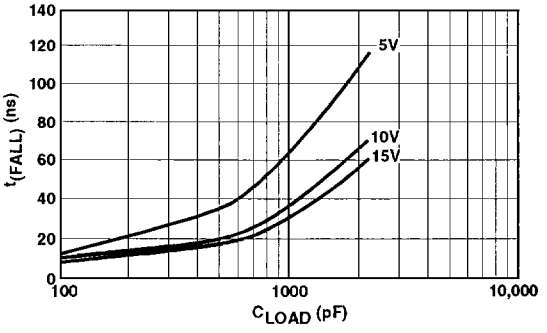
Fall Time vs Supply Voltage
(TC443X, TC445X, TC446X)



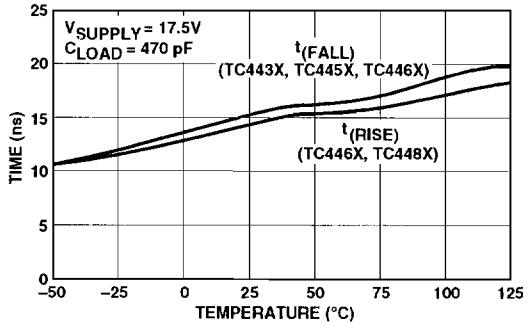
Rise Time vs Capacitive Load
(TC446X, TC448X)



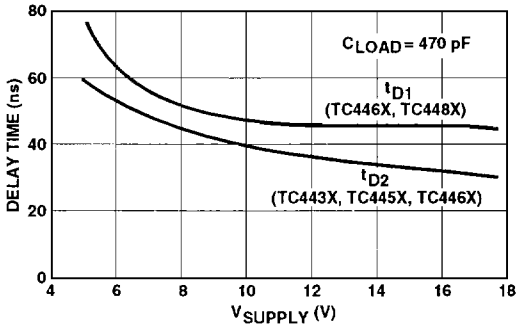
Fall Time vs Capacitive Load
(TC443X, TC445X, TC446X)



Rise/Fall Times vs Temperature



Propagation Delay Time vs Supply Voltage



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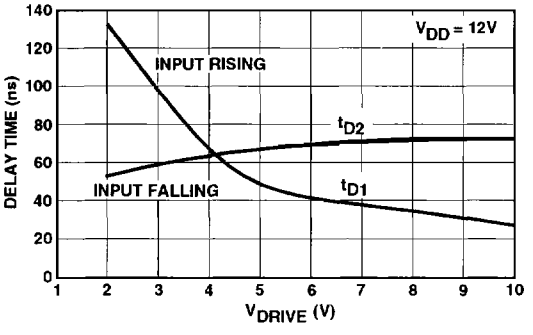
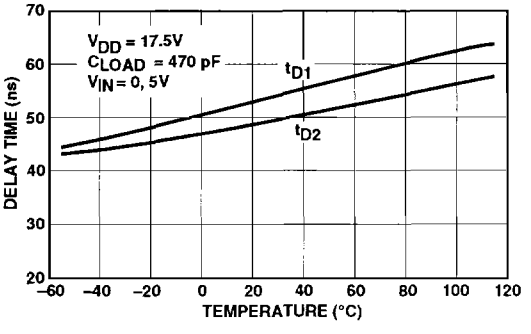
CHARACTERISTICS CURVES (Cont.)

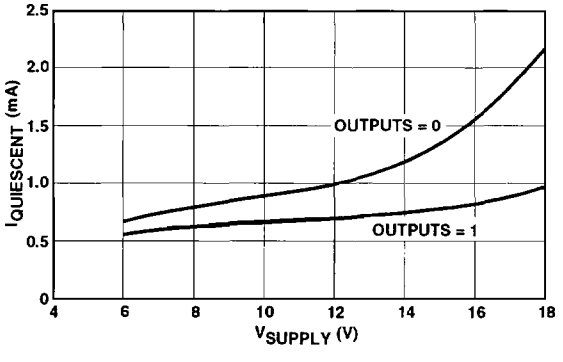
Input Amplitude vs Delay Times



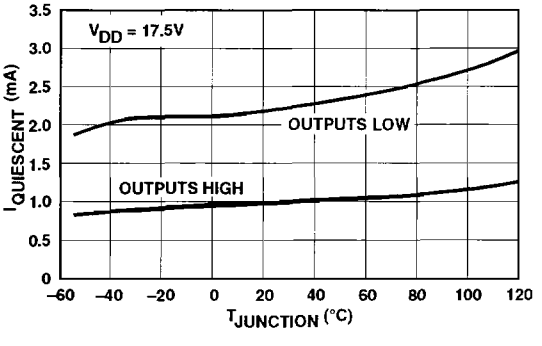
Propagation Delay Times vs Temperature



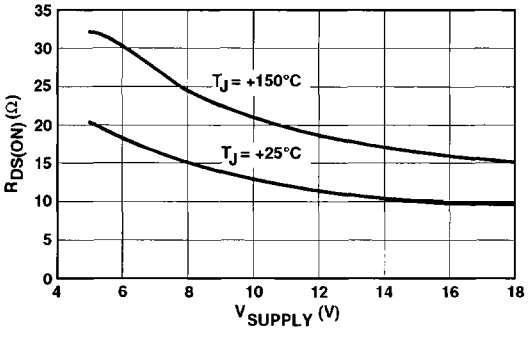
Quiescent Supply Current vs Supply Voltage



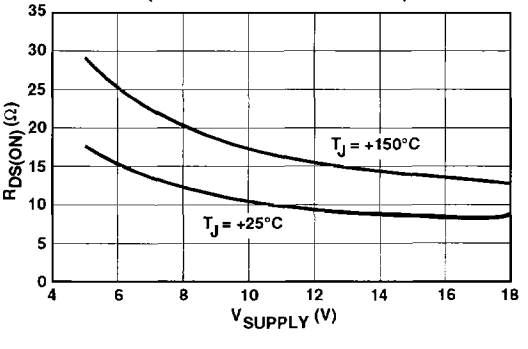
Quiescent Supply Current vs Temperature



High-State Output Resistance
(TC446X, TC448X)

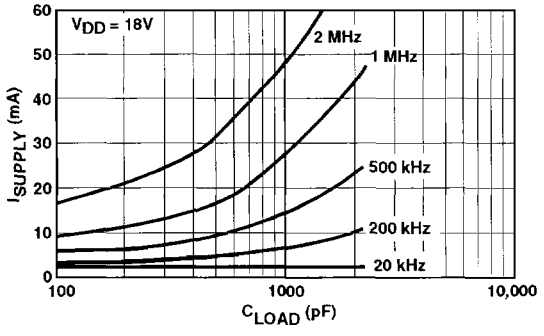


Low-State Output Resistance
(TC443X, TC445X, TC446X)

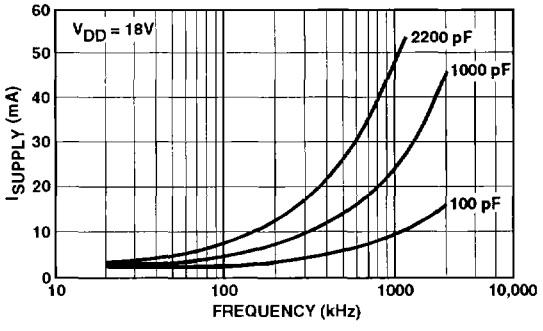


SUPPLY CURRENT CHARACTERISTICS (Load on Single Output Only)

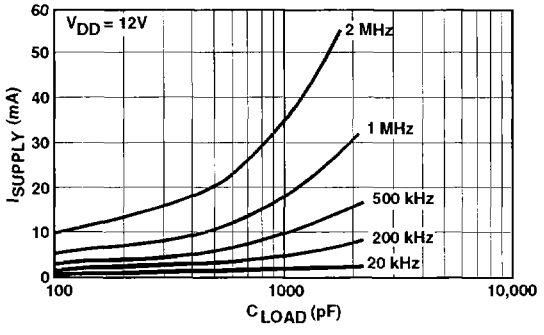
Supply Current vs Capacitive Load
(TC446X)



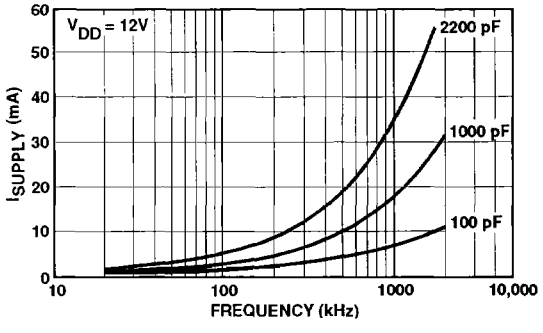
Supply Current vs Frequency
(TC446X)



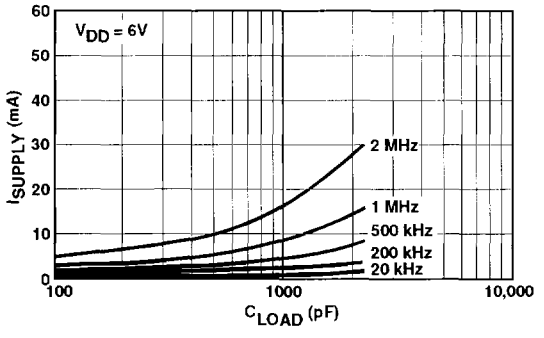
Supply Current vs Capacitive Load
(TC446X)



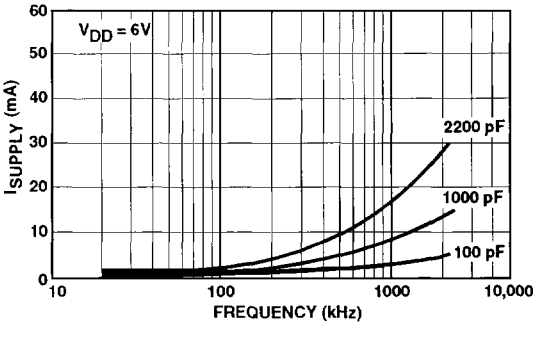
Supply Current vs Frequency
(TC446X)



Supply Current vs Capacitive Load
(TC446X)



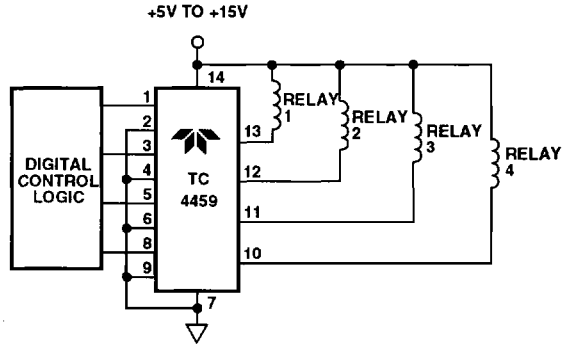
Supply Current vs Frequency
(TC446X)



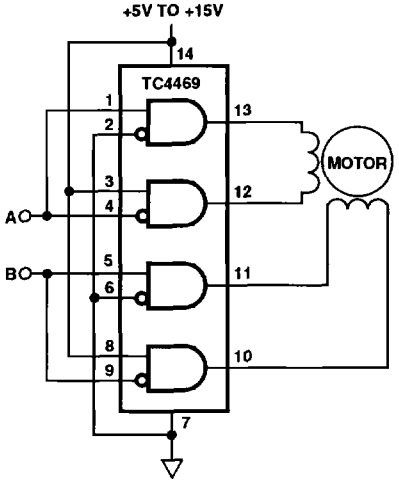
TC4437/8/9 TC4467/8/9
TC4457/8/9 TC4487/8/9

TYPICAL APPLICATIONS

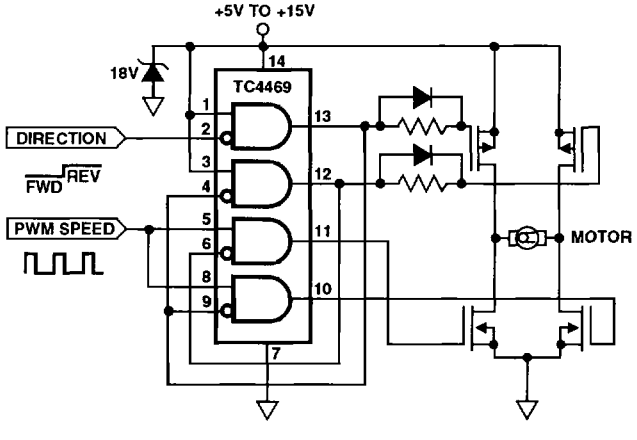
Quad Relay Driver Interface



Stepper Motor Drive



Quad Driver for H-Bridge Motor Control



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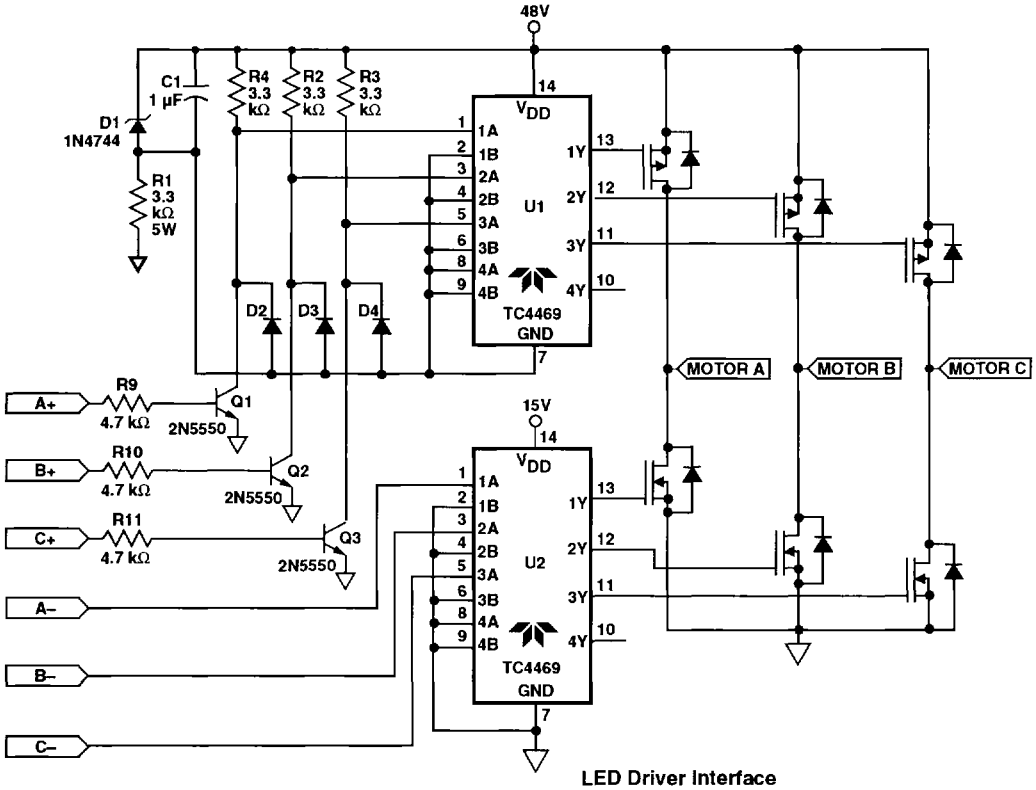
TYPICAL APPLICATIONS (Cont.)

48-Volt, 3-Phase Brushless Output Stage



LED Driver Interface