

D-1454/155

R-1454/155

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SN54180, SN74180 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54180		SN74180		UNIT
		MIN	TYP‡	MAX	MIN	
V _{IH} High-level input voltage		2			2	V
V _{IL} Low-level input voltage			0.8		0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA		-1.5		-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 µA	2.4	3.3	2.4	3.3	V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2 0.4		0.2 0.4	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		1		1	mA
I _{IH} High-level input current	Any data input		40		40	µA
	Even or odd input	V _{CC} = MAX, V _I = 2.4 V		80		
I _{IL} Low-level input current	Any data input		-1.6		-1.6	mA
	Even or odd input	V _{CC} = MAX, V _I = 0.4 V		-3.2		
I _{OS} Short-circuit output current‡	V _{CC} = MAX	-20	-55	-18	-55	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 2	34	49	34	56	mA

NOTE 2: I_{CC} is measured with even and odd inputs at 4.5 V, all other inputs and outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

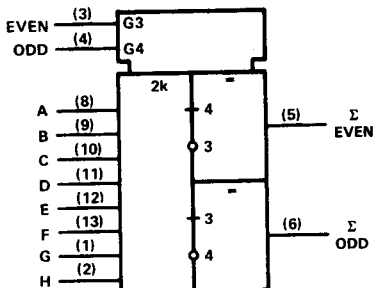
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Data	Σ Even	C _L = 15 pF, R _L = 400 Ω, Odd input grounded, See Note 3	40	60	ns	
				45	68		
t _{PHL}	Data	Σ Odd		32	48	ns	
				25	38		
t _{PLH}	Data	Σ Even		C _L = 15 pF, R _L = 400 Ω, Even input grounded, See Note 3	32	48	ns
					25	38	
t _{PHL}	Data	Σ Odd	40		60	ns	
			45		68		
t _{PLH}	Even or Odd	Σ Even or Σ Odd	C _L = 15 pF, R _L = 400 Ω, See Note 3		13	20	ns
					7	10	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

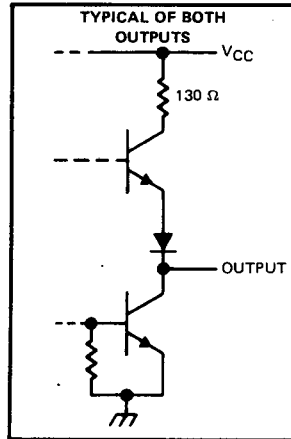
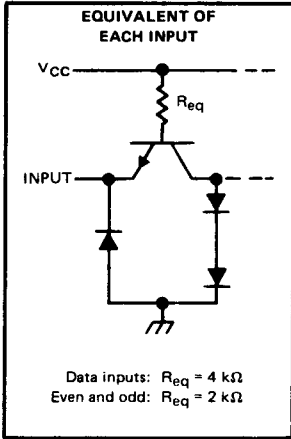
logic symbol†



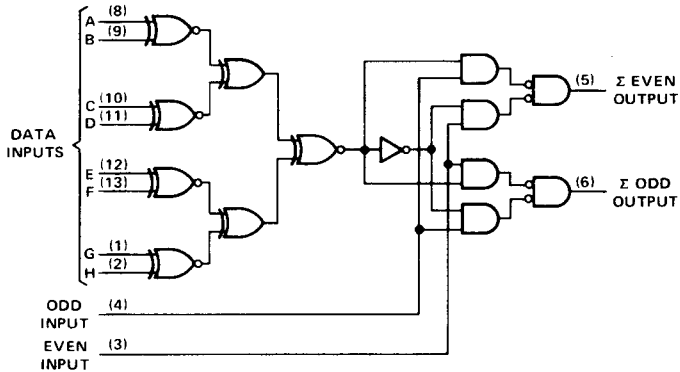
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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schematics of inputs and outputs



logic diagram (positive logic)



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TTL Devices