

CA3260, CA3260A

4MHz, BiMOS Operational Amplifier with MOSFET Input/CMOS Output

FN1266
Rev.7.00
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CA3260A and CA3260 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA3260 series circuits are dual versions of the popular CA3160 series.

Gate protected P-Channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute in single supply applications.

A complementary symmetry MOS (CMOS) transistor pair, capable of swinging the output voltage to within 10mV of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3260 Series circuits operate at supply voltages ranging from 4V to 16V, or $\pm 2V$ to $\pm 8V$ when using split supplies. The CA3260A offers superior input characteristics over those of the CA3260.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
CA3260E	CA3260E	-55 to +125	8 Ld PDIP	E8.3
CA3260EZ (Note)	CA3260EZ	-55 to +125	8 Ld PDIP* (Pb-free)	E8.3
CA3260AE	CA3260AE	-55 to +125	8 Ld PDIP	E8.3
CA3260AEZ (Note)	3260AEZ	-55 to +125	8 Ld PDIP* (Pb-free)	E8.3

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

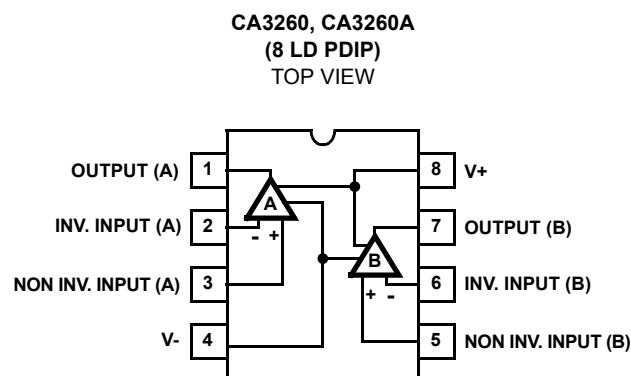
Features

- MOSFET Input Stage provides
 - Very High $Z_i = 1.5T\Omega$ ($1.5 \times 10^{12}\Omega$) (Typ)
 - Very Low I_i 5pA (Typ) at 15V Operation
..... 2pA (Typ) at 5V Operation
- Ideal for Single Supply Applications
- Common Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (Or Both) Supply Rails
- Pb-Free Available (RoHS Compliant)

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- Ideal Interface with Digital CMOS
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to 0V)
- Wien Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers

Pinout



Absolute Maximum Ratings

DC Supply Voltage (V+ to V-) 16V
 DC Input Voltage (V+ +8V) to (V- -0.5V)
 Differential Input Voltage 8V
 Input Terminal Current 1mA
 Output Short Circuit Duration (Note 1)..... Indefinite

Operating Conditions

Temperature Range -55°C to +125°C

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W) θ_{JC} (°C/W)
 PDIP Package* 100 N/A
 Maximum Junction Temperature (Plastic Package) +150°C
 Maximum Storage Temperature Range -65°C to +150°C
 Pb-Free Reflow Profile see link below

<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = +25^\circ\text{C}$, Typical Values Intended Only for Design Guidance.

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUES		UNITS
			CA3260A	CA3260	
Input Resistance	R_I	$V_S = \pm 7.5\text{V}$	1.5	1.5	$T\Omega$
Input Capacitance	C_I	$f = 1\text{MHz}$, $V_S = \pm 7.5\text{V}$	4.3	4.3	pF
Unity Gain Crossover Frequency	f_T	$V_S = \pm 7.5\text{V}$	4	4	MHz
Slew Rate	SR	$V_S = \pm 7.5\text{V}$	10	10	V/ μs
Transient Response	Rise Time	$C_L = 25\text{pF}$, $R_L = 2\text{k}\Omega$, $A_V = +1$, $V_S = \pm 7.5\text{V}$	0.09	0.09	μs
	Overshoot		10	10	%
Settling Time (to <0.1%, $V_{IN} = 4V_{P-P}$)	t_S	$C_L = 25\text{pF}$, $R_L = 2\text{k}\Omega$, $A_V = +1$, $V_S = \pm 7.5\text{V}$	1.8	1.8	μs
Input Offset Voltage	V_{IO}	$V_+ = 5\text{V}$, $V_- = 0\text{V}$	2	6	mV
Input Offset Current	I_{IO}	$V_+ = 5\text{V}$, $V_- = 0\text{V}$	0.1	0.1	pA
Input Current	I_I	$V_+ = 5\text{V}$, $V_- = 0\text{V}$	2	2	pA
Common Mode Rejection Ratio	CMRR	$V_+ = 5\text{V}$, $V_- = 0\text{V}$	70	60	dB
Large Signal Voltage Gain	A_{OL}	$V_O = 4V_{P-P}$, $R_L = 20\text{k}\Omega$, $V_+ = 5\text{V}$, $V_- = 0\text{V}$	100	100	kV/V
			100	100	dB
Common Mode Input Voltage Range	V_{ICR}	$V_+ = 5\text{V}$, $V_- = 0\text{V}$	0 to 2.5	0 to 2.5	V
Supply Current	I_+	$V_O = 5\text{V}$, $R_L = \infty$, $V_+ = 5\text{V}$, $V_- = 0\text{V}$	1	1	mA
		$V_O = 2.5\text{V}$, $R_L = \infty$, $V_+ = 5\text{V}$, $V_- = 0\text{V}$	1.2	1.2	mA
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V_+$, $V_+ = 5\text{V}$, $V_- = 0\text{V}$	200	200	$\mu\text{V/V}$

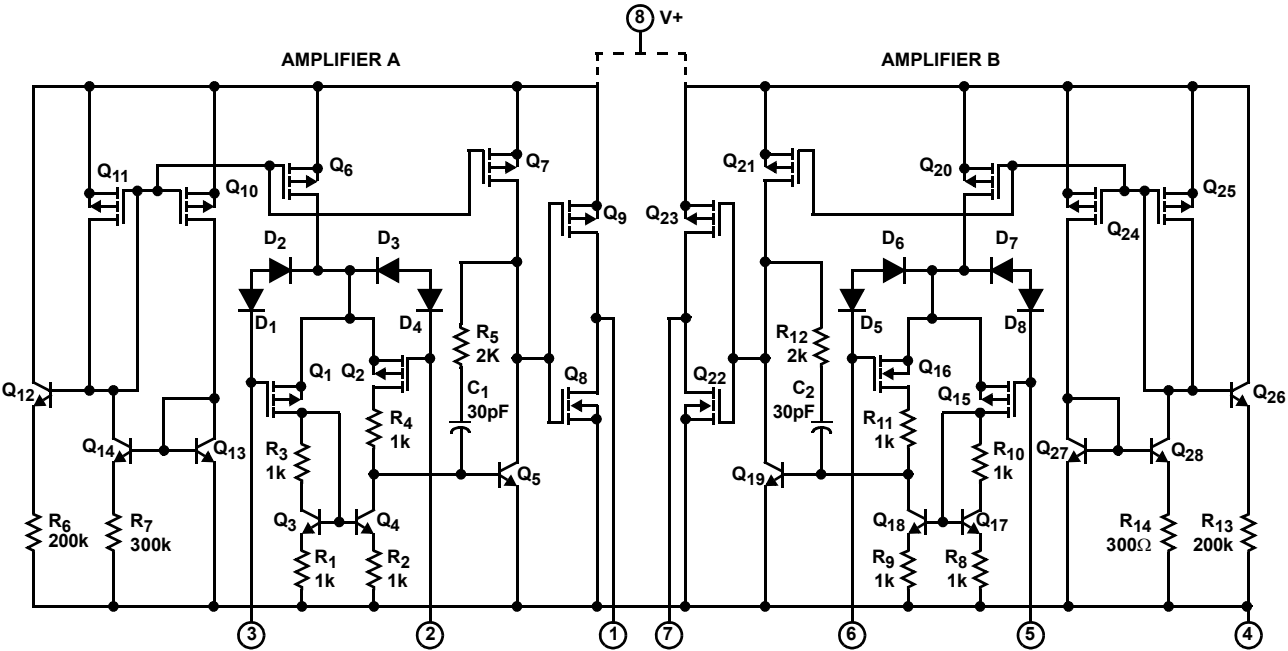
Electrical Specifications For Each Amplifier at $T_A = +25^\circ\text{C}$, $V_+ = 15\text{V}$, $V_- = 0\text{V}$, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	CA3260A			CA3260			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$ V_{IO} $	$V_S = \pm 7.5\text{V}$	-	2	5	-	6	15	mV
Input Offset Current	$ I_{IO} $	$V_S = \pm 7.5\text{V}$	-	0.5	20	-	0.5	30	pA
Input Current	I_I	$V_S = \pm 7.5\text{V}$	-	5	30	-	5	50	pA
Large Signal Voltage Gain	A_{OL}	$V_O = 10V_{P-P}$, $R_L = 10\text{k}\Omega$	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common Mode Rejection Ratio	CMRR		80	95	-	70	90	-	dB

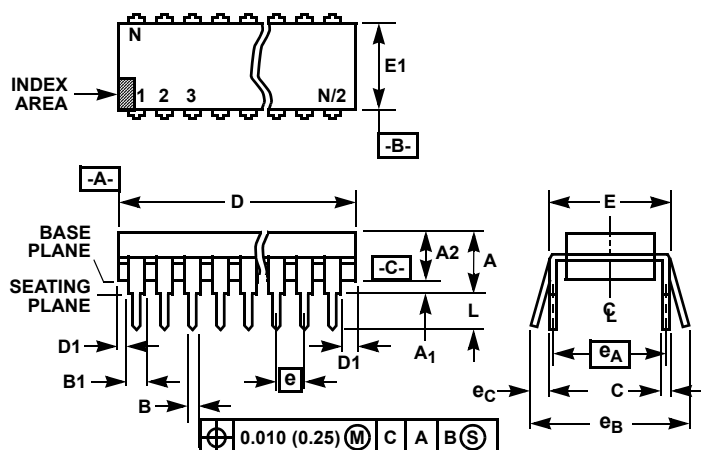
Electrical Specifications For Each Amplifier at T_A = +25°C, V₊ = 15V, V₋ = 0V, Unless Otherwise Specified. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	CA3260A			CA3260			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Common Mode Input Voltage Range	V _{ICR}		0	-0.5 to 12	10	0	-0.5 to 12	10	V
Power Supply Rejection Ratio	PSRR	$\Delta V_{IO}/\Delta V_+$ V ₊ = 17.5V	-	32	150	-	32	320	μV/V
Maximum Output Voltage	V _{OM+}	R _L = 10kΩ	11	13.3	-	11	13.3	-	V
	V _{OM-}		-	0.002	0.01	-	0.002	0.01	V
	V _{OM+}	R _L = ∞	14.99	15	-	14.99	15	-	V
	V _{OM-}		-	0	0.01	-	0	0.01	V
Maximum Output Current	I _{OM+} Source	V _O = 0V	12	22	45	12	22	45	mA
	I _{OM-} Sink	V _O = 15V	12	20	45	12	20	45	mA
Total Supply Current V _O (Amplifier A) = 7.5V V _O (Amplifier B) = 7.5V	I ₊	R _L = ∞	-	9	15.5	-	9	15.5	mA
			-	1.2	3	-	1.2	3	mA
			-	5	8.5	-	5	8.5	mA
Input Offset Voltage Temperature Drift	ΔV _{IO} /ΔT		-	6	-	-	8	-	μV/°C
Crosstalk		f = 1kHz	-	120	-	-	120	-	dB

Schematic Diagram



Dual-In-Line Plastic Packages (PDIP)



NOTES:

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and e_A are measured with the leads constrained to be perpendicular to datum $-C-$.
- e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D) 8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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