NEC

PRELIMINARY DATA SHEET

MOS INTEGRATED CIRCUIT

MC-42S1000LAD32S SERIES

1M -WORD BY 32-BIT DYNAMIC RAM MODULE

FAST PAGE MODE

Description

The MC-42S1000LAD32S series is a 1 048 576 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 2 pieces of 16M DRAM (uPD 42S18160L) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{CAS}$ before $\overline{RAS}$ self refresh,$\overline{CAS}$ before $\overline{RAS}$ refresh , $\overline{RAS}$ only refresh , Hidden refresh.
- 1 048 576 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC- 42S1000LAD32S-60	60ns	110ns	1 080mw	1.08mw (CMOS level)
MC- 42S1000LAD32S-70	70ns	130ns	1 008mw	
MC- 42S1000LAD32S-80	80ns	150ns	936mw	

- 1 024 refresh cycles/128 ms
- 72-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +3.3V±0.3V power supply

Ordering information

Part Number	Access time (MAX.)	Package	Mounted devices
MC- 42S1000LAD32SA-60	60ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	2 pieces of uPD42S18160LG5 (TSOP II) [Single side]
MC- 42S1000LAD32SA-70	70ns		
MC- 42S1000LAD32SA-80	80ns		

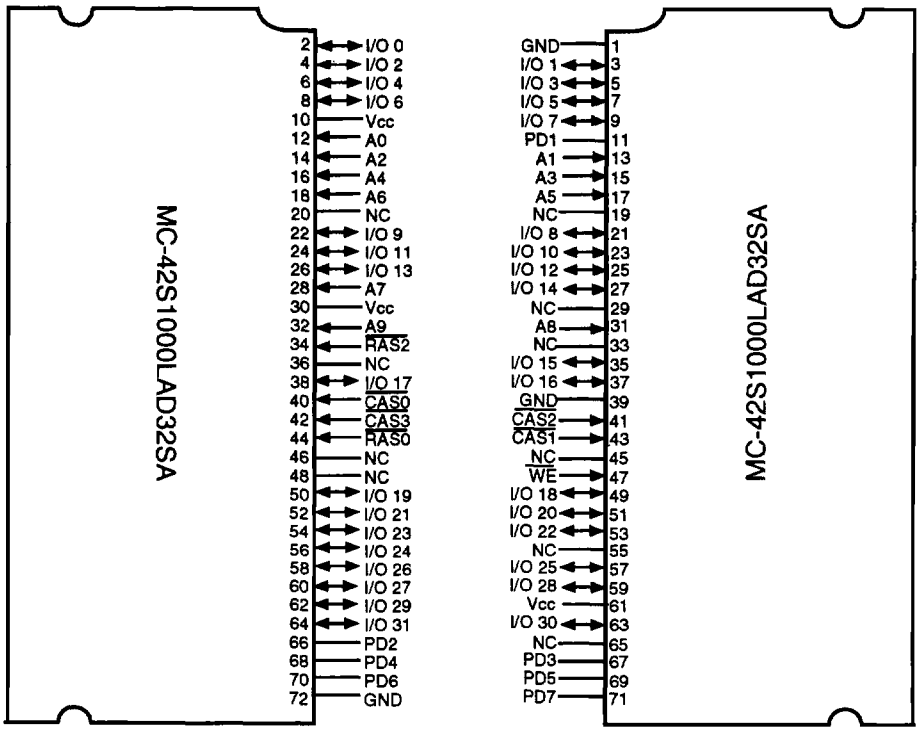
Quality grade

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



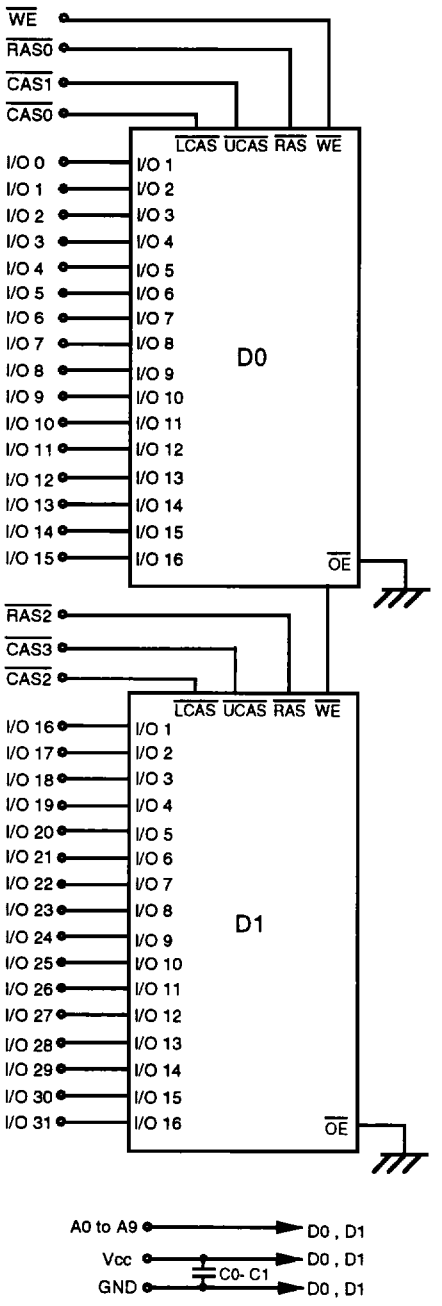
A0 - A9 : Address Inputs
I/O 0-I/O 31 : Data Inputs / Outputs
$\overline{RAS0}$,$\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$-$\overline{CAS3}$: Column Address Strobe
$\overline{WE}$: Write Enable
PD1- PD7 : Presence Detect Pins
Vcc : Power Supply
GND : Ground
NC : No connection

The internal connection of PD pins(PD1 - PD7)

Pin Name	Pin No.	Accsess Time		
		60ns	70ns	80ns
PD1	11	NC	NC	NC
PD2	66	GND	GND	GND
PD3	67	GND	GND	GND
PD4	68	NC	NC	NC
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram

Remark D0 - D1 : uPD42S18160L(TSOP(II))



Electrical Specifications Notes 1,2

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-0.5 to +4.6	V
Supply voltage	VCC		-0.5 to +4.6	V
Output current	IO		20	mA
Power dissipation	PD		2	W
Operating temperature	Topt		0 to +70	℃
Storage temperature	Tstg		-55 to +125	℃

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device in not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES : 1, 2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		3.0	3.3	3.6	V
High level input voltage	VIH		2.0		Vcc + 0.3	V
Low level input voltage	VIL		-0.3		+0.8	V
Ambient temperature	Ta		0		70	℃

CAPACITANCE (Ta=25℃ , f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI1	A0 to A9			60	pF
	CI2	$\overline{WE}$			60	
	CI3	$\overline{RAS0}$, $\overline{RAS2}$			40	
	CI4	$\overline{CAS0}$ - $\overline{CAS3}$			40	
Data Input/ Output capacitance	C I/O	I/O 0 - I/O31			27	pF

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
Operating Current	Icc1	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC}=t_{RC(MIN.)}$, IO=0mA	t_{RAC}=60ns		300	mA	3,4,7
			t_{RAC}=70ns		280		
			t_{RAC}=80ns		260		
Standby Current	Icc2	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH(MIN.)}$			1.0	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ Vcc-0.2V			0.3		
$\overline{RAS}$ only refresh current	Icc3	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≧ V_{IH} $t_{RC}=t_{RC(MIN.)}$, IO=0mA	t_{RAC}=60ns		300	mA	3,4,5,7
			t_{RAC}=70ns		280		
			t_{RAC}=80ns		260		
Operating Current (Fast Page Mode)	Icc4	$\overline{RAS}$ ≦ VIL, $\overline{CAS}$ Cycling tPC=tPC MIN., IO=0mA	t_{RAC}=60ns		180	mA	3,4,6
			t_{RAC}=70ns		160		
			t_{RAC}=80ns		140		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	Icc5	$t_{RC}=t_{RC(MIN.)}$ IO=0mA	t_{RAC}=60ns		300	mA	3,4
			t_{RAC}=70ns		280		
			t_{RAC}=80ns		260		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current	Icc6	$\overline{CAS}$ before $\overline{RAS}$ refresh : 2 048 Cycles / 128ms $\overline{RAS}$, $\overline{CAS}$: Vcc-0.2 V≦ VIH≦VIH(MAX) Standby : $\overline{RAS}$, $\overline{CAS}$ ≧ Vcc-0.2V Address : VIH or VIL $\overline{WE}$: VIH IO = 0 mA	t_{RAS}≦ 1us		360	μA	3,4
$\overline{CAS}$ before $\overline{RAS}$ self refresh current	Icc7	$\overline{RAS}$, $\overline{CAS}$: Vcc-0.2 V≦ VIH≦VIH(MAX) 0V ≦ VIL ≦ 0.2V IO = 0 mA			300	μA	4
Input Leakage Current	$I_{I(L)}$	VI=0 to 3.6V all other pins not under test = 0V		-5	+5	μA	
Output Leakage Current	$I_{O(L)}$	Outputs are disabled (Hi - Z) VO=0 to 3.6V		-5	+5	μA	
High level output voltage	V_{OH}	IO=-2.0mA		2.4		V	
Low level output voltage	V_{OL}	IO=+2.0mA			0.4	V	

AC CHARACTERISTICS

Notes 8,9

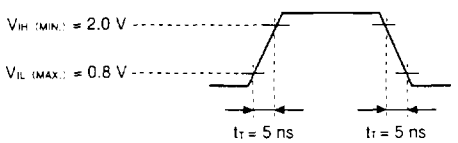
(Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		tRAC = 80ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read or Write Cycle Time	tRC	110	-	130	-	150	-	ns	
Fast Page Mode Cycle Time (Read or Write)	tPC	40	-	45	-	50	-	ns	
Access Time from $\overline{RAS}$	tRAC	-	60	-	70	-	80	ns	10,11
Access Time from $\overline{CAS}$	tCAC	-	15	-	20	-	20	ns	10,11
Access Time from Column Address	tAA	-	30	-	35	-	40	ns	10,11
Access Time from $\overline{CAS}$ Precharge	tACP	-	35	-	40	-	45	ns	11
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRAD	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	tCLZ	0	-	0	-	0	-	ns	11
Output Buffer Turn-off Delay Time ($\overline{CAS}$)	tOFF	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	tT	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	tRP	40	-	50	-	60	-	ns	
$\overline{RAS}$ Pulse Width (Random Read, Write Cycle)	tRAS	60	10 000	70	10 000	80	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	tRASP	60	125 000	70	125 000	80	125 000	ns	
$\overline{RAS}$ Hold Time	tRSH	15	-	18	-	20	-	ns	
$\overline{CAS}$ Pulse Width	tCAS	15	10 000	20	10 000	20	10 000	ns	
$\overline{CAS}$ Hold Time	tCSH	60	-	70	-	80	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	-	5	-	5	-	ns	13
$\overline{CAS}$ Precharge Time	tCPN	10	-	10	-	10	-	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	tCP	10	-	10	-	10	-	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	tRPC	5	-	5	-	5	-	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	tRHCP	35	-	40	-	45	-	ns	
Row Address Set Up Time	tASR	0	-	0	-	0	-	ns	
Row Address Hold Time	tRAH	10	-	10	-	12	-	ns	
Column Address Set Up Time	tASC	0	-	0	-	0	-	ns	
Column Address Hold Time	tCAH	15	-	15	-	15	-	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	tRAL	30	-	35	-	40	-	ns	
Read Command Set Up Time	tRCS	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	0	-	0	-	0	-	ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0	-	0	-	0	-	ns	14
Write Command Hold Time Referenced to $\overline{CAS}$	tWCH	10	-	10	-	15	-	ns	15
Data-in Set Up Time	tDS	0	-	0	-	0	-	ns	16
Data-in Hold Time	tDH	10	-	15	-	15	-	ns	16
Write Command Setup Time	tWCS	0	-	0	-	0	-	ns	17
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	tCSR	5	-	5	-	5	-	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	tCHR	10	-	10	-	10	-	ns	
$\overline{RAS}$ Puls Width($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)	tRASS	100	-	100	-	100	-	us	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)	tRPS	110	-	130	-	150	-	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)	tCHS	-50	-	-50	-	-50	-	ns	
$\overline{WE}$ Setup Time	tWSR	10	-	10	-	10	-	ns	
$\overline{WE}$ Hold Time	tWHR	15	-	15	-	15	-	ns	
Refresh Time	tREF	-	128	-	128	-	128	ms	

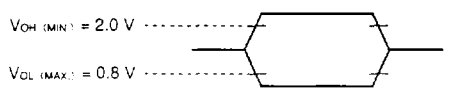
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycles rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL\ (MAX.)}$ and $\overline{CAS} \geqq V_{IH\ (MIN.)}$.
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification

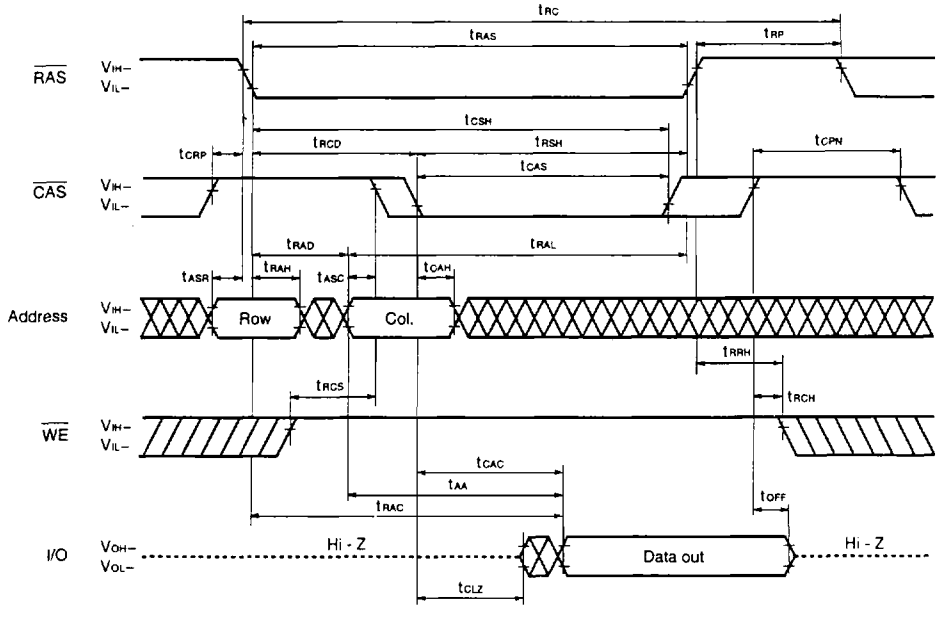


10. For read cycles, access time is defined as follows :

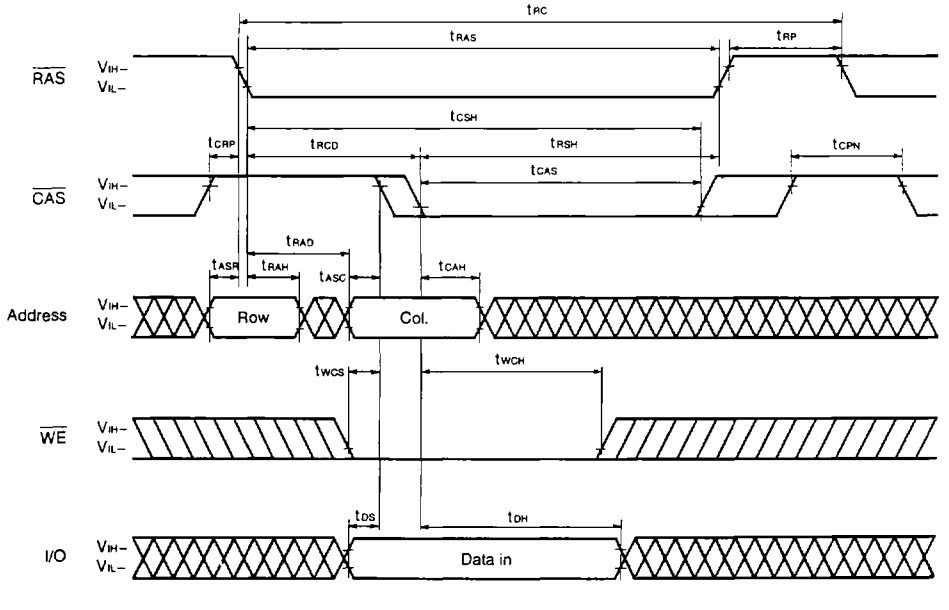
Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

    $t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specifided as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD\ (MAX.)}$ and $t_{RCD} \geqq t_{RCD\ (MAX.)}$ will not cause any operation problems.
11. Loading conditions are 1 TTL and 100 pF.
12. $t_{OFF\ (MAX.)}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirement should be applied for $\overline{RAS}$, $\overline{CAS}$ cycles preceded by any cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geqq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

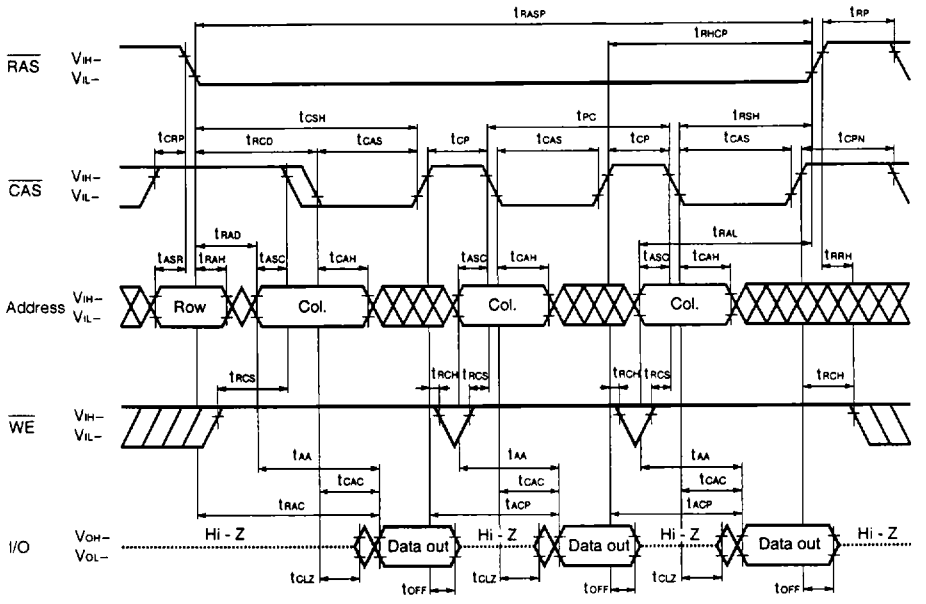
Read Cycle



Early Write Cycle

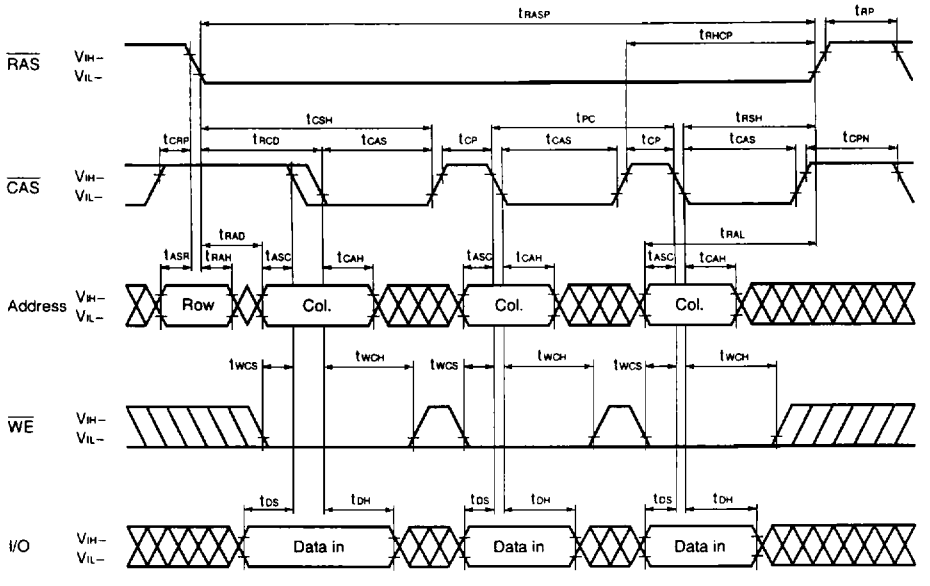


Fast Page Mode Read Cycle



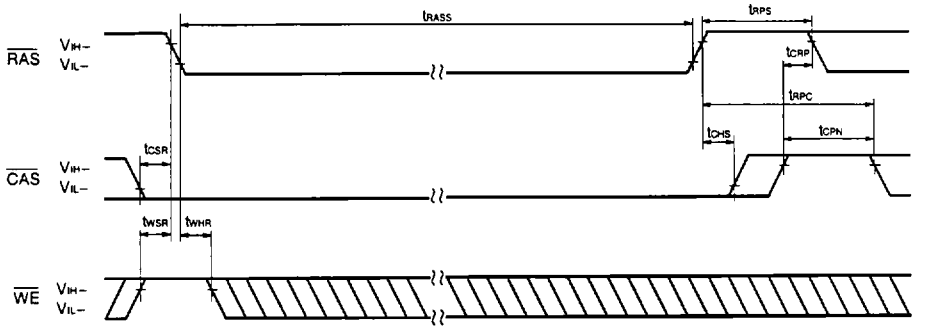
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle



Remark Address : Don't care I/O : Hi - Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with burst long $\overline{RAS}$ only refresh, the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh

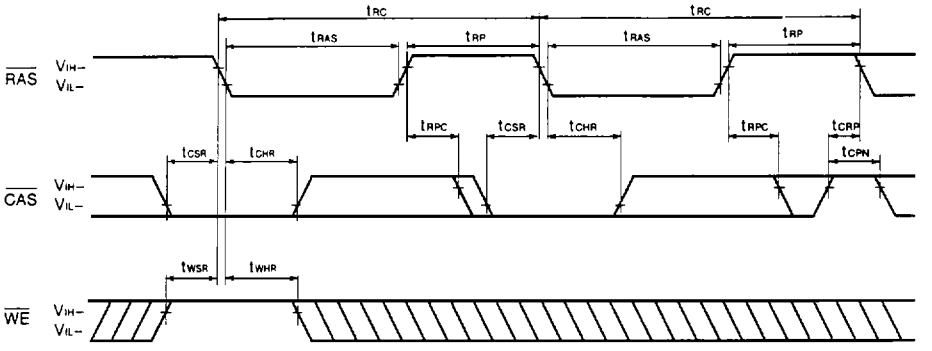
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 1 024 times within a 16 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst Long $\overline{RAS}$ Only Refresh

When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 1 024 times within an interval of 16 ms or less just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

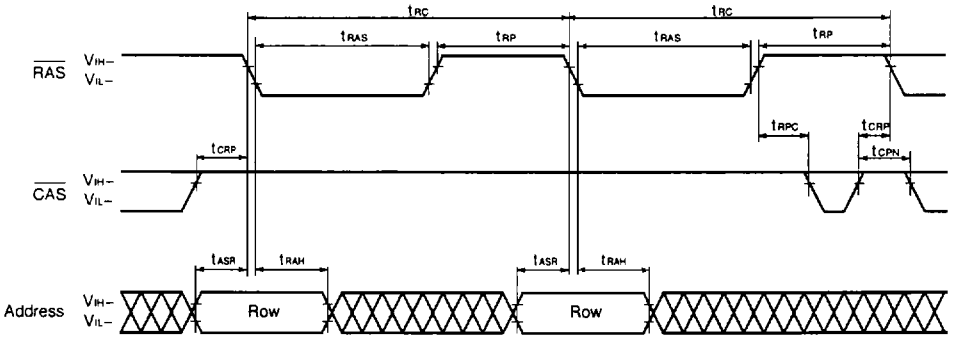
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



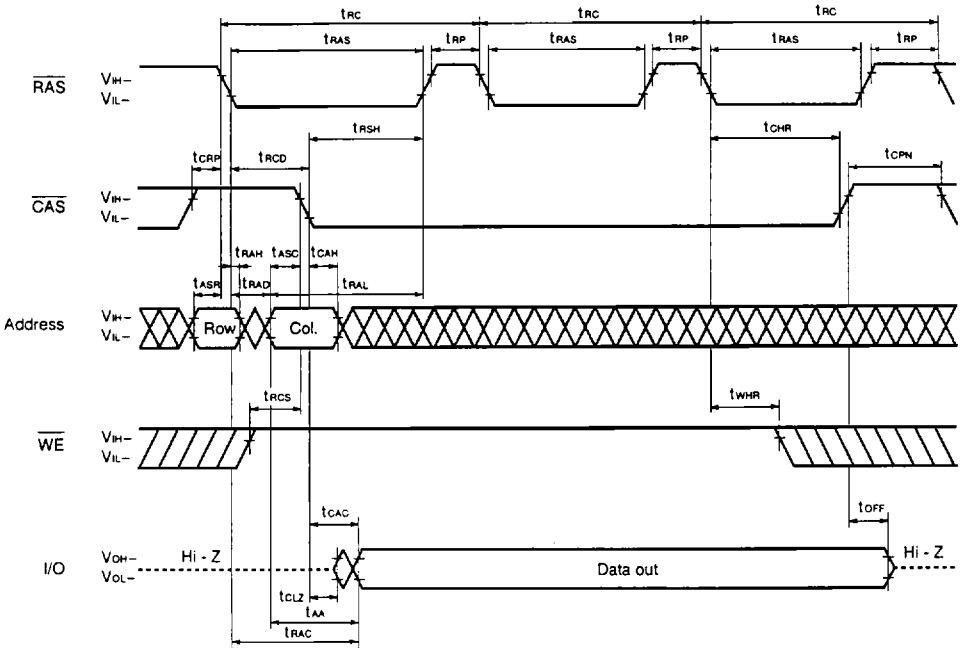
Remark Address = Don't care I/O = Hi - Z

$\overline{RAS}$ Only Refresh Cycle



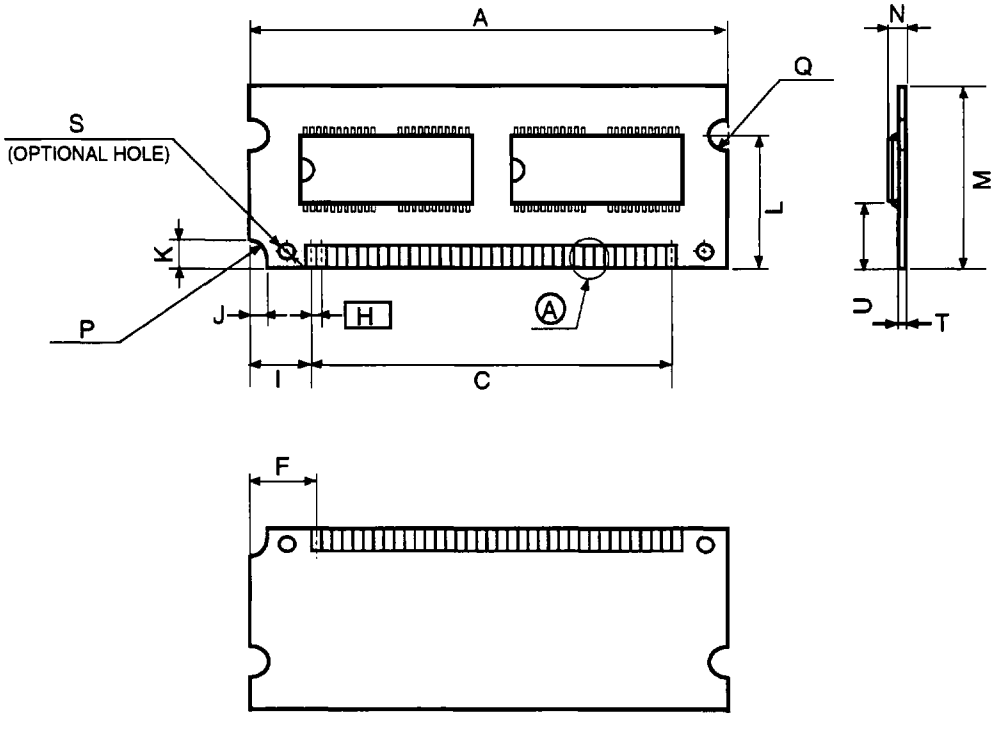
Remark $\overline{WE}$ = Don't care I/O = Hi - Z

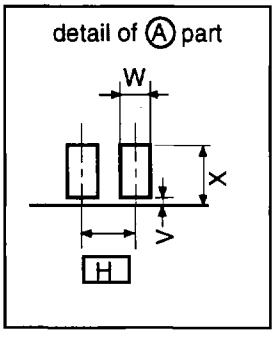
Hidden Refresh Cycle



Package Drawing

72 PIN DUAL IN-LINE MEMORY MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35 ±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.03	0.080
K	3.175	0.125
L	17.78	0.700
M	25.4	1.000
N	2.413 MAX.	0.095 MAX.
P	R1.57	R0.062
Q	R2.0	R0.079
S	Ø1.8	Ø0.071
T	1.016±0.1	0.04 ±0.004
U	3.175 MIN	0.125 MIN
V	0.25 MAX.	0.010 MAX.
W	1.04 ±0.05	0.041±0.002
X	2.54 MIN	0.100 MIN