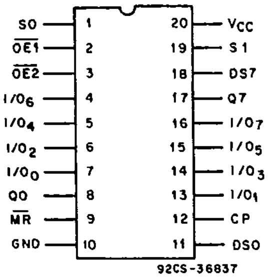
File Number **1485**

CD54/74HC299
CD54/74HCT299

HARRIS SEMICOND SECTOR 27E D ■ 4302271 0017770 7 ■HAS

T-46-09-05

High-Speed CMOS Logic



TERMINAL ASSIGNMENT

8-Bit Universal Shift Register; 3-State

Type Features:

- *Four Operation Modes: Shift Left, Shift Right, Load and Store*
- *Can be cascaded for N-bit word lengths*
- *I/O_0-I/O_7 bus drive capability and 3-state for bus oriented applications*
- *Buffered inputs*
- *Typical f_{MAX}=50 MHz @ V_{CC}=5 V, C_L=15 pF, T_A=25° C*

The RCA-CD54/74HC299 and CD54/74HCT299 are 8-bit shift/storage registers with 3-state bus interface capability. The register has four synchronous-operating modes controlled by the two select inputs as shown in the mode select (S0, S1) table. The mode select, the serial data (DS0, DS7) and the parallel data (I/O_0-I/O_7) respond only to the low-to-high transition of the clock (CP) pulse. S0, S1 and data inputs must be one set-up time prior to the clock positive transition.

The Master Reset ($\overline{MR}$) is an asynchronous active low input. When $\overline{MR}$ output is low, the register is cleared regardless of the status of all other inputs. The register can be expanded by cascading same units by tying the serial output (Q0) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DS0) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DS0 of the first stage.

The 3-state input/output I(/O) port has three modes of operation:

1. Both output enable ($\overline{OE}$1 and $\overline{OE}$2) inputs are low and S0 or S1 or both are low, the data in the register is presented at the eight outputs.
2. When both S0 and S1 are high, I/O terminals are in the high impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of $\overline{OE1}$ and $\overline{OE2}$.
3. Either one of the two output enable inputs being high will force I/O terminals to be in the off-state. It is noted that each I/O terminal is a 3-state output and an CMOS buffer input.

The CD54HC299 and CD54HCT299 are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC299 and CD74HCT299 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *N_{IL}=30%, N_{IH}=30% of V_{CC}; @ V_{CC}=5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL}=0.8 V Max., V_{IH}=2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

CD54/74HC299
CD54/74HCT299

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{cc}): (Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V < V_o < V_{CC} + 0.5V)	
For Q Outputs	±25mA
For I/O Outputs	±35mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±70mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +40 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING TEMPERATURE RANGE (T_A)	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

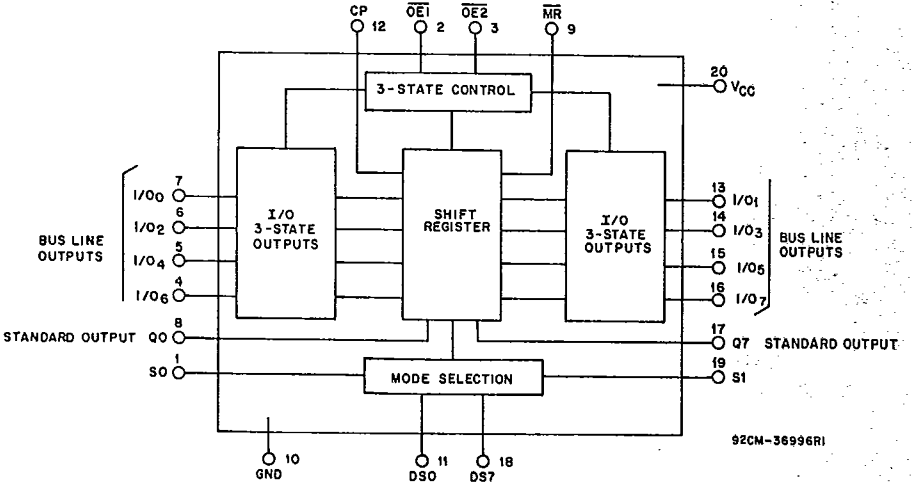

Fig. 1 — Function diagram.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC299/CD54HC299										CD74HCT299/CD54HCT299									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads Bus Driver and Standard Output	V_{IL} or V_{IH}	Qn I/On									V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4 -6	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2 -7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads Bus Driver and Standard Output	V_{IL} or V_{IH}	Qn I/On									V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4 6	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2 7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-State Leakage Current	V_{IL} or V_{IH}	V_O= V_{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
S1, $\overline{MR}$	0.25
I/O_0-I/O_7	0.25
DS0, DS7	0.25
$\overline{S0}$, CP	0.6
$\overline{OE1}$, $\overline{OE2}$	0.3

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C.

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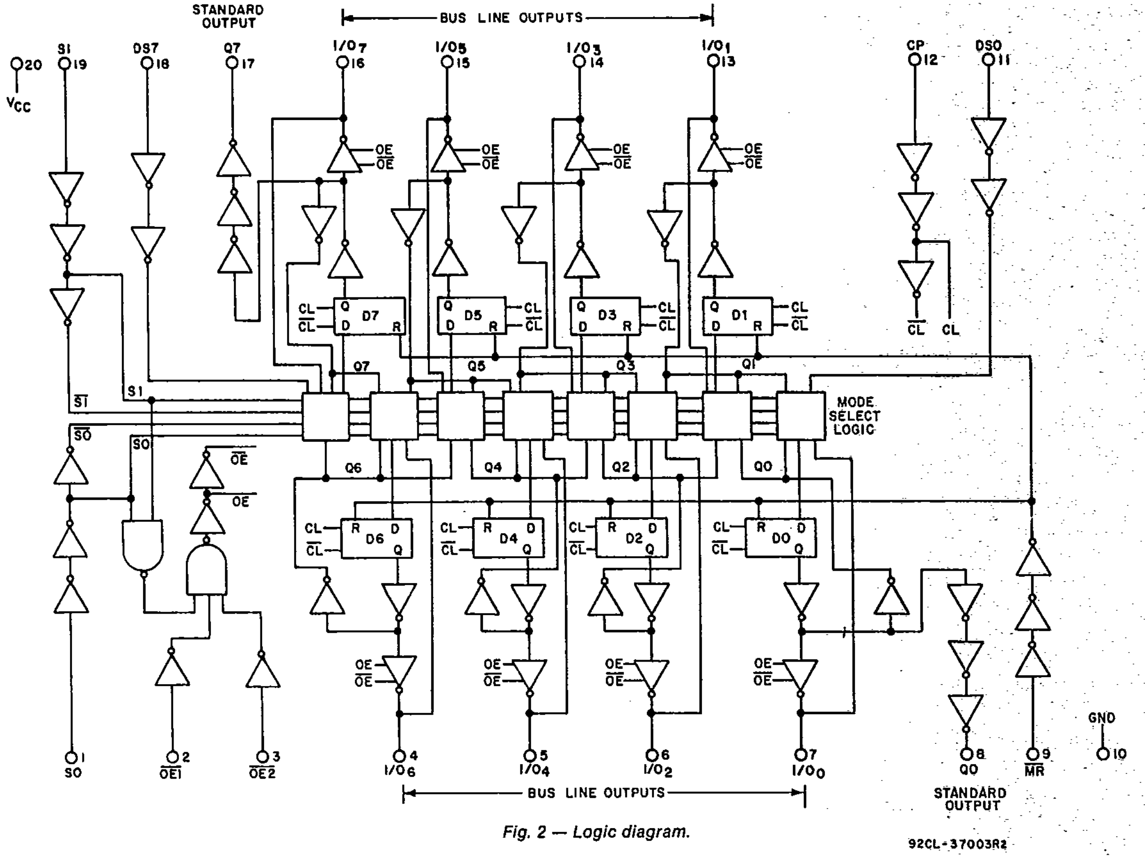

Fig. 2 — Logic diagram.

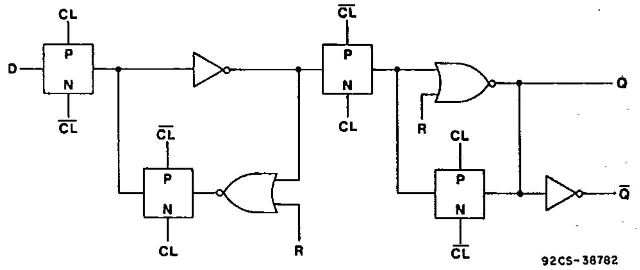

Fig. 3 — Flip-Flop detail (D0-D7).

MODE SELECT-FUNCTION TABLE

REGISTER OPERATING MODES

FUNCTION	INPUTS							REGISTER OUTPUTS				
	$\overline{MR}$	CP	S0	S1	DS0	DS7	I/On	Q0	Q1	---	Q6	Q7
Reset (Clear)	L	X	X	X	X	X	X	L	L	---	L	L
Shift Right	H	↑	h	l	l	X	X	L	q_0	---	q_5	q_6
	H	↑	h	l	h	X	X	H	q_0	---	q_5	Q6
Shift Left	H	↑	l	h	X	l	X	q_1	q2	---	q_7	L
	H	↑	l	h	X	h	X	q_1	q_2	---	q_7	H
Hold (do nothing)	H	↑	l	l	X	X	X	q_0	q_1	---	q_6	q_7
Parallel Load	H	↑	h	h	X	X	l	L	L	---	L	L
	H	↑	h	h	X	X	h	H	H	---	H	H

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MODE-SELECT FUNCTION TABLE
3-STATE I/O PORT OPERATING MODE

FUNCTION	INPUTS					INPUTS/OUTPUTS
	$\overline{OE1}$	$\overline{OE2}$	S0	S1	Qn(Register)	I/O0 - - - I/O7
Read Register	L	L	L	X	L	L
	L	L	L	X	H	H
	L	L	X	L	L	L
	L	L	X	L	H	H
Load Register	X	X	H	H	Qn = I/On	I/On = Inputs
Disable I/O	H	X	X	X	X	(Z)
	X	H	X	X	X	(Z)

H = Input voltage high level.
h = Input voltage high one set-up time prior clock transition.
L = Input voltage low level.
l = Input voltge low one set-up time prior clock transition.
q_n = Lower case letter indicates the state of the referenced output one set-up time prior clock transition.
X = Voltage level on logic status don't care.
Z = Output in high impedance state.
↗ = Low-to-high clock transition.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay Clock to I/O Outputs (Fig. 4)	t_{PLH} t_{PHL}	15	17	19	ns
Clock Q0 or Q7 (Fig. 4)					
$\overline{MR}$ to Outputs (Fig. 5)	t_{PHL}	15	17	19	
Output Enable and Disable Times (Fig. 6 & 7)	t_{PZL}, t_{PZH} t_{PLZ}, t_{PHZ}	15	10,13,15	10,13,15	
Power Dissipation Capacitance	C_{PD}*	—	150	170	pF

*C_{PD} is used to determine the dynamic power consumption, per register.
$PD = C_{PD} V_{CC}^2 fi + \Sigma (C_L V_{CC}^2 fo)$ where:
f_i=input frequency
f_o=output frequency
C_L=output load capacitance
V_{CC}=supply voltage

Pre-requisite for Switching Function

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	25	—	20	—	20	—	16	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	
$\overline{MR}$ Pulse Width (Fig. 5)	t_W	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	15	—	13	—	19	—	15	—	22	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Clock Pulse Width (Fig. 4)	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Setup Time DS0, DS7, I/On to Clock (Fig. 8)	t_{SU}	2	100	—	—	—	125	—	—	—	150	—	—	—	
		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Hold Time DS0, DS7, I/On, S0, S1 to Clock (Fig. 8)	t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
Recovery Time $\overline{MR}$ to Clock (Fig. 5)	t_{REC}	2	5	—	—	—	5	—	—	—	5	—	—	—	
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Setup Time S1, S0 to Clock	t_{SU}	2	120	—	—	—	150	—	—	—	180	—	—	—	
		4.5	24	—	27	—	30	—	34	—	36	—	41	—	
		6	20	—	—	—	26	—	—	—	31	—	—	—	

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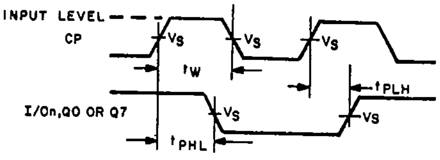
SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Clock to I/O Output (Fig. 4)	t_{PLH} t_{PHL}	2	—	200	—	—	—	250	—	—	—	300	—	—	ns
		4.5	—	40	—	45	—	50	—	56	—	60	—	68	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Clock to Q0 and Q7 (Fig. 4)		2	—	200	—	—	—	250	—	—	—	300	—	—	
		4.5	—	40	—	45	—	50	—	56	—	60	—	68	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Propagation Delay $\overline{MR}$ to Output (Fig. 5)	t_{PHL}	2	—	200	—	—	—	250	—	—	—	300	—	—	
		4.5	—	40	—	46	—	50	—	58	—	60	—	69	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Output High-Z to High Level (Fig. 6)	t_{PZH}	2	—	155	—	—	—	195	—	—	—	235	—	—	
		4.5	—	31	—	32	—	39	—	40	—	47	—	48	
		6	—	26	—	—	—	33	—	—	—	40	—	—	
Output High Level to High-Z (Fig. 6)	t_{PHZ}	2	—	185	—	—	—	230	—	—	—	280	—	—	
		4.5	—	37	—	37	—	46	—	46	—	56	—	56	
		6	—	31	—	—	—	39	—	—	—	48	—	—	
Output Low Level to High-Z (Fig. 7)	t_{PLZ}	2	—	155	—	—	—	195	—	—	—	235	—	—	
		4.5	—	31	—	32	—	39	—	40	—	47	—	48	
		6	—	26	—	—	—	33	—	—	—	40	—	—	
Output High-Z to Low Level (Fig. 7)	t_{PZL}	2	—	130	—	—	—	165	—	—	—	195	—	—	
		4.5	—	26	—	30	—	33	—	38	—	39	—	45	
		6	—	22	—	—	—	28	—	—	—	33	—	—	
Output Transition Time Q0, Q7 (Fig. 9)	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
I/O_0 to I/O_7 (Fig. 9)		2	—	60	—	—	—	75	—	—	—	90	—	—	
		4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	pF



	74/54 HC	74/54 HCT
INPUT LEVEL	VCC	3 V
VS	50 % VCC	1.3 V

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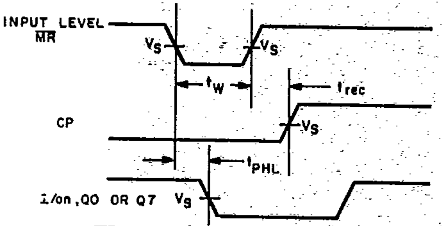
Fig. 4 — Clock pre-requisite and propagation delays.



	74/54HC	74/54 HCT
INPUT LEVEL	VCC	3V
VS	50% VCC	1.3V

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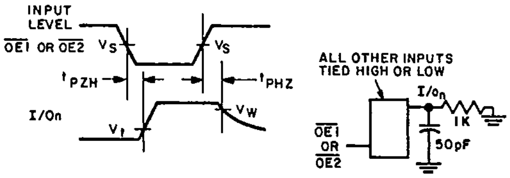
Fig. 5 — Master Reset pre-requisite and propagation delays.



	74/54 HC	74/54 HCT
INPUT LEVEL	VCC	3V
VS	50% VCC	1.3 V
Vt	50 % VCC	1.3 V
VW	90% VCC	90% VCC

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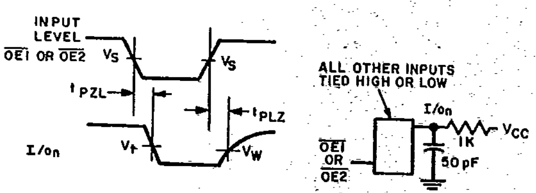
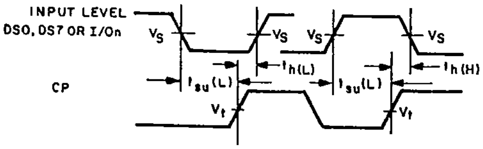
Fig. 6 — 3-state propagation delays.



	74/54 HC	74/54 HCT
INPUT LEVEL	VCC	3V
VS	50 % VCC	1.3 V
Vt	50 % VCC	1.3 V
VW	10% VCC	10% VCC

92CS-37000RI

Fig. 7 — 3-state propagation delays.



	74/54 HC	74/54 HCT
INPUT LEVEL	VCC	3 V
VS	50 % VCC	1.3 V
Vt	50 % VCC	1.3V

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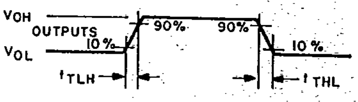
Fig. 8 — Data pre-requisite times.



	74/54 HC	74/54 HCT
INPUT LEVEL	VCC	3V

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Fig. 9 — Output transition times.