KEYBOARD ENCODER (JIS CODE STANDARD PRODUCT)

DESCRIPTION

The M58620-001S is a keyboard encoder for solid-state switches and is fabricated with P-channel aluminum-gate MOS technology.

It contains a 3640-bit mask-programmable read-only memory, and the 7-bit and 8-bit codes specified in JIS publication C-6220-1969 "Codes for Information Interchange" are stored in the ROM. The mode shift is selected by the combination of shift input, control input and shift control input. The output consists of a 9-bit plus parity bit code. All inputs and outputs are TTL-compatible.

FEATURES

- All inputs and outputs are TTL-compatible
- Output buffer register
- Strobe inhibit circuit for unused codes
- One shot output (the pulse width is variable) or static output for strobed output
- Chip enable terminal
- 2-key rollover capability (N-key rollover is also available, if the logic output of the switches is pulsive)

APPLICATION

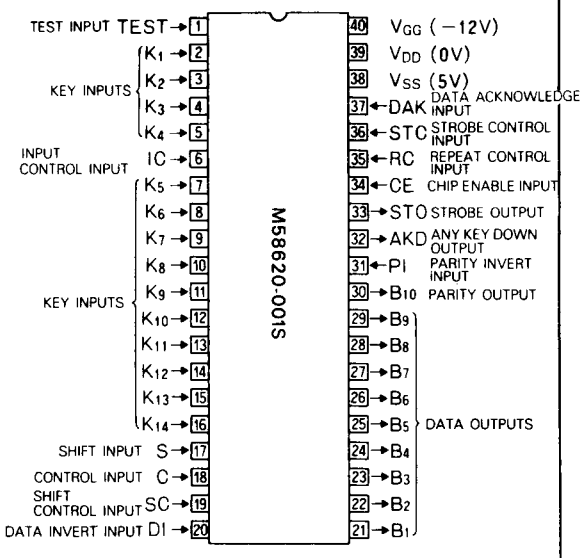
- Encoder for full-keyboard terminal equipment

FUNCTION

The output of each keyboard switch is connected to 2-key inputs selected from K_1~K_{14} (2 of 14) to form 91 addresses. Therefore, the character code for output is selected by 2 of 14 key inputs, shift input, control input and shift control input.

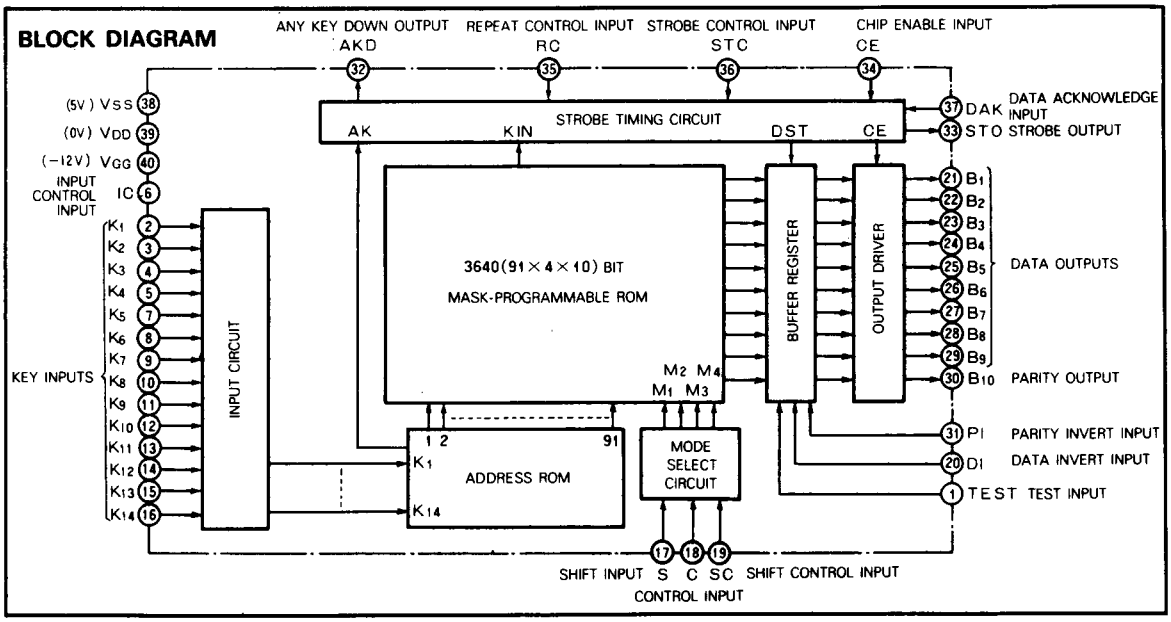
When a key is depressed, the output of that keyboard switch is applied to two key inputs selected from K_1~K_{14}; the address ROM generates an address that is used for input to the 3640-bit ROM. After the encoded data from the ROM is transferred to the buffer register, a strobed output is generated, validating the encoded data.

PIN CONFIGURATION (TOP VIEW)



Outline 40S1

BLOCK DIAGRAM



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FUNCTION (Data Output and Parity Output)

The relationships between B_1~B_8 in the code table and B_1 ~B_8 in data outputs are shown in Table 1, and those between the parity output (B_{10} or B_9) and the parity bit, in Tables 2 and 3. The parity bit in the tables is defined as a '0' when the number of '1's in the code (B_1~B_8 or B_1~B_7) is odd and a '1' when it is even.

Mode selection is shown in Table 4.

Table 1 Relation between code table and outputs

B_1 ~ B_8 in code table	Data invert input DI	Data output B_1 ~ B_8	Logic
1	L	H	Positive logic
1	H	L	Negative logic
0	L	L	Positive logic
0	H	H	Negative logic

Table 2 Parity output of 8-bit code

Parity bit	Parity invert output PI	Parity output B_{10}
1	L	H
1	H	L
0	L	L
0	H	H

Table 3 Parity output of 7-bit code

Parity bit	Data invert input DI	Data output B_9
1	L	H
1	H	L
0	L	L
0	H	H

Table 4 Mode selection

Shift input S	Control input C	Shift control input SC	Selected mode
L	L	L	1
H	L	L	2
L	H	L	3
H	H	L	4
L	L	H	4
H	L	H	–
L	H	H	–
H	H	H	–

CODE TABLE (JIS C-6220-1969)

NUMBER OF BITS																				
									0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
									0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
									0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
									0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
B_{10}† B_9*	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	ROW / COL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PARITY BIT					0	0	0	0	0	NUL	DLE	SP	0	@	P	`					—	タ	ミ		
					0	0	0	1	1	SOH	DC_1	!	1	A	Q					。	ア	チ	ム		
					0	0	1	0	2	STX	DC_2	"	2	B	R					「	イ	ツ	メ		
					0	0	1	1	3	ETX	DC_3	#	3	C	S					」	ウ	テ	モ		
					0	1	0	0	4	EOT		$	4	D	T					、	エ	ト	ヤ		
					0	1	0	1	5	ENQ	NAK	%	5	E	U					・	オ	ナ	ユ		
					0	1	1	0	6	ACK	SYN	&	6	F	V					ヲ	カ	ニ	ヨ		
					0	1	1	1	7	BEL	ETB	'	7	G	W					ァ	キ	ヌ	ラ		
					1	0	0	0	8	BS	CAN	(	8	H	X					ィ	ク	ネ	リ		
					1	0	0	1	9	HT	EM	)	9	I	Y					ゥ	ケ	ノ	ル		
					1	0	1	0	10	LF	SUB	*	:	J	Z					ェ	コ	ハ	レ		
					1	0	1	1	11	VT	ESC	+	;	K	[					ォ	サ	ヒ	ロ		
					1	1	0	0	12	FF		,	<	L	¥					ャ	シ	フ	ワ		
					1	1	0	1	13	CR		−	=	M	]					ュ	ス	ヘ	ン		
					1	1	1	0	14	SO		.	>	N	^					ョ	セ	ホ	゛		
					1	1	1	1	15	SI		/	?	O	_		DEL			ッ	ソ	マ	゜		

* B_9 is an odd parity bit for the 7-bit code (B_1 ~ B_7)

† B_{10} is an odd parity bit for the 8-bit code (B_1 ~ B_8)

Note 1 : When inputs DI and PI are low-level, a '1' in the code table indicates that the output level goes high, a '0' that it goes low

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CODE ARRANGEMENT TABLE

Kn \ Km	Mode	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14
K1	1	Z	X	C	V	B	N	M	,	.	／		A	S
	2								＜	＞	?	―		
	3	ツ	サ	ソ	ヒ	コ	ミ	モ	ネ	ル	メ	ロ	チ	ト
	4	ッ							､	｡	･			
K2	1		D	F	G	H	J	K	L	;	:	)	Q	W
	2					・				＋	＊	！		
	3		シ	ハ	キ	ク	マ	ノ	リ	レ	ケ	ム	タ	テ
	4											｣		
K3	1			E	R	T	Y	U	I	O	P	@	「	1
	2										゛	゜	」	!
	3			イ	ス	カ	ン	ナ	ニ	ラ	セ	、	・	ヌ
	4			ｲ									｢	
K4	1				2	3	4	5	6	7	8	9	0	―
	2				"	#	$	%	&	'	(	)		=
	3				フ	ア	ウ	エ	オ	ヤ	ユ	ヨ	ワ	ホ
	4					ｱ	ｳ	ｴ	ｵ	ｬ	ｭ	ｮ	ｦ	
K5	1					^	¥	DEL	SP	SOH	STX	ETX	EOT	ENQ
	2					―		DEL	SP	SOH	STX	ETX	EOT	ENQ
	3					へ	_	DEL	SP	SOH	STX	ETX	EOT	ENQ
	4							DEL	SP	SOH	STX	ETX	EOT	ENQ
K6	1						ACK	BEL	BS	HT	LF	VT	FF	CR
	2						ACK	BEL	BS	HT	LF	VT	FF	CR
	3						ACK	BEL	BS	HT	LF	VT	FF	CR
	4						ACK	BEL	BS	HT	LF	VT	FF	CR
K7	1							SO	SI	DLE	DC1	DC2	DC3	NAK
	2							SO	SI	DLE	DC1	DC2	DC3	NAK
	3							SO	SI	DLE	DC1	DC2	DC3	NAK
	4							SO	SI	DLE	DC1	DC2	DC3	NAK
K8	1								SYN	ETB	CAN	EM	SUB	ESC
	2								SYN	ETB	CAN	EM	SUB	ESC
	3								SYN	ETB	CAN	EM	SUB	ESC
	4								SYN	ETB	CAN	EM	SUB	ESC
K9	1									NUL	+	―	＝	・
	2									NUL	+	―	＝	・
	3									NUL	+	―	＝	・
	4									NUL	+	―	＝	・
K10	1										1	2	3	4
	2										1	2	3	4
	3										1	2	3	4
	4										1	2	3	4
K11	1											5	6	7
	2											5	6	7
	3											5	6	7
	4											5	6	7
K12	1												8	9
	2												8	9
	3												8	9
	4												8	9
K13	1													0
	2													0
	3													0
	4													0

SYMBOLOGY

Symbol	Code name	Col/Row in code table	km/kn/Mode in code arrangement table
SP	Space	2／0	K9 / K5 / 1～4
!	Exclamation mark	2／1	K14 / K3 / 2
"	Quotation mark, umlaut	2／2	K5 / K4 / 2
#	Number sign	2／3	K6 / K4 / 2
$	Dollar sign	2／4	K7 / K4 / 2
%	Percentage	2／5	K8 / K4 / 2
&	Ampersand	2／6	K9 / K4 / 2
'	Apostrophe, acute accent	2／7	K10 / K4 / 2
(	Left parenthesis	2／8	K11 / K4 / 2
)	Right parenthesis	2／9	K12 / K4 / 2
*	Asterisk, multiplication sign	2／10	K11 / K2 / 2
+	Positive sign, plus sign	2／11	K10 / K2 / 2 *
,	Comma	2／12	K9 / K1 / 1
−	Negative sign, subtraction sign	2／13	K14 / K4 / 1 *
.	Period	2／14	K10 / K1 / 1 *
／	Slash, virgule division sign, per	2／15	K11 / K1 / 1
:	Colon	3／10	K11 / K2 / 1
;	Semicolon	3／11	K10 / K2 / 1
<	Less than sign	3／12	K9 / K1 / 2
=	Equal sign	3／13	K14 / K4 / 2 *
>	Greater than sign	3／14	K10 / K4 / 2

*See K11～K14/K9/1～4

Symbol	Code name	Col/Row in code table	km/kn/Mode in code arrangement table
?	Question mark,	3／15	K11 / K1 / 2
@	At mark	4／0	K12 / K3 / 1
[	Left bracket	5／11	K13 / K3 / 1
¥	Yen sign	5／12	K7 / K5 / 1
]	Right bracket	5／13	K12 / K2 / 1
^	Circumflex accent	5／14	K6 / K5 / 1
_	Underline	5／15	K12 / K1 / 2
`	Grave accent	6／0	K12 / K3 / 2
{	Left brace	7／11	K13 / K3 / 2
|	Separate sign, logical add sign	7／12	K7 / K5 / 2
}	Right brace	7／13	K12 / K2 / 2
‾	Overline, logical not sign	7／14	K6 / K5 / 2
。	Japanese period	10／1	K10 / K1 / 4
「	Japanese initial quotation mark	10／2	K13 / K3 / 4
」	Japanese final quotation mark	10／3	K12 / K2 / 4
、	Japanese comma	10／4	K9 / K1 / 4
・	Middle dot	10／5	K11 / K1 / 4
―	Long vowel mark	11／0	K7 / K5 / 3
゛	Voiced consonant mark	13／14	K12 / K3 / 3
゜	Semi-voiced consonant mark	13／15	K13 / K3 / 3

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OPERATION

1. 2-Key Rollover (N-Key Lockout)

When more than 2 keyboard switches are depressed at the same time, all outputs 1~91 of the address ROM go high-level, and the 3640-bit ROM is not addressed. The internal key input signal also is not applied to the timing circuit; as a result, a strobe signal is not generated. Also, the coded outputs hold the preceding state. Then, if any one key (key 1) is not released while the other keys are, key 1 becomes valid.

2. N-Key Rollover

If the key input signals are pulsive, the primary depressed key (key 1) is read; after the coded output of key 1 is transferred to the buffer register, a strobe signal is generated and the coded output becomes valid. Then, if a second key is depressed while key 1 is in the depressed state, the second key (key 2) is read; and the coded output of key 2 is transferred to the buffer register succeeding the coded output of key 1 described above. A strobe signal is generated, and the coded output becomes valid. Then if a third, fourth . . . Nth key is depressed while preceding keys are still in the depressed state, its code will become valid as described above.

3. Any-Key-Down Output

When any one or more of the 91 keys are depressed, an internal any-key signal is transferred from the address ROM to the timing circuit where an any-key-down signal (AKD) is generated.

4. Strobe Inhibit When an Unused Code Is Addressed

If either an unused mode of the 4 modes or an unused key is selected (its ROM code is 0000000000), the strobe output is inhibited and it makes the key invalid. The data output still holds the preceding state.

5. Repeat Function

When a repeat signal is applied to the repeat control input (RC), a strobe signal is repeatedly generated so that any character can be repeated. The strobe signal is inhibited when the RC terminal is high.

6. Data Acknowledge Input

The strobe output is reset by applying a data acknowledge input. The pulse width of the strobe signal output can be adjusted with a resistor and a capacitor connected between the strobe output terminal (STO) and the data acknowledge input terminal (DAK).

7. Data Invert and Parity Invert Inputs

The level of each output B_1~B_9 and B_{10} can be inverted when data invert input (DI) and parity invert input (PI) are high-level.

8. Chip Enable Input

Data outputs B_1~B_{10}, strobe output and any-key-down output are in the floating state when chip enable input (CE) is high.

This floating state means a high-impedance state and is equivalent to an open-circuit output.

9. Input Control Input

When input control input (IC) is high, key inputs (K_1~K_{14}) can be operated with high-level signals.

10. Strobe Control Input

The strobe delay time can be set by the strobe control input STC terminal. The delay time is set to $t_{d(ST-B)}$, which depends on the internal delay circuit when the strobe control input terminal is connected to V_{SS}.

11. Test Input

Data outputs (B_1~B_{10}) can be independently set either high or low irrespective of the 3640-bit ROM outputs. When test input (TEST) is high, B_1~B_{10} goes high if both DI and PI are low, and B_1~B_{10} goes low if both DI and PI are high.

12. Pull-up Resistors

External resistors are not required because pull-up resistors are built-in at all input terminals. But if the strobe control input terminal is not used, it should be connected to V_{SS}. To determine the value of the resistor required, see Electrical Characteristics.

Pull-up resistors

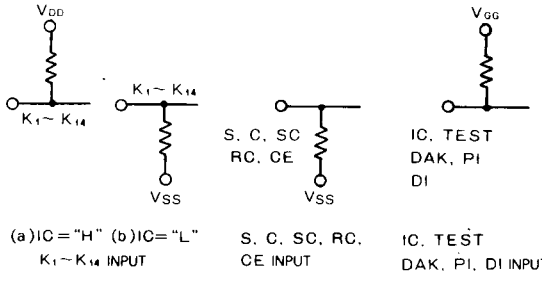

Table 1 Data-output level in relation to data invert (DI), parity invert (PI) and chip enable (CE)

ROM CODE	DI, PI	CE	B1~B10
1	H	L	L
	L	L	H
0	H	L	H
	L	L	L
1	H	H	Z
	L	H	Z
0	H	H	Z
	L	H	Z

Note 2 : Z indicates a floating state.
3 : The code table is described in positive logic, for outputs B_1 ~ B_{10}, when DI and PI are low.

Table 2 Function table of the mode select circuit

S	C	SC	MODE
H	H	H	–
L	H	H	–
H	L	H	–
L	L	H	M_4
H	H	L	M_4
L	H	L	M_3
H	L	L	M_2
L	L	L	M_1

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{GG}	Supply voltage	With respect to V_{SS}	0.3～−20	V
V_{DD}	Supply voltage		0.3～−20	V
V_I	Input voltage		0.3～−20	V
Pd	Power dissipation	Ta=25°C	1.0	W
Topr	Operating free-air temperature range		−20～75	°C
Tstg	Storage temperature range		−40～125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=−20～75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{GG}	Supply voltage	−10.8	−12	−13.2	V
V_{DD}	Supply voltage		0		V
V_{SS}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage, all inputs except STC	Vss−1.5		V_{SS}	V
V_{IL}	Low-level input voltage	V_{DD}		Vss−3.5	V
t_r	Rise time (10～90%), all inputs except DAK			1	μs
t_f	Fall time (10～90%)			1	μs
$t_{r(DAK)}$	Rise time (10～90%), DAK			100	μs
$t_{f(DAK)}$	Fall time (10～90%), DAK			100	μs

ELECTRICAL CHARACTERISTICS (Ta=−20～75°C, V_{GG}=−12V±10%, V_{DD}=0V, V_{SS}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage	I_{OH}=−100μA	Vss−1			V
V_{OL}	Low-level input voltage	I_{OL}=1.6mA, (Note 2)			0.4	V
$I_{I(1)}$	Input current, TEST, IC, DI, PI, and DAK	$V_I=V_{GG}$		−0.01	−10	μA
$I_{I(2)}$	Input current, K_1～K_{14}	$V_I=V_{DD}$, $V_{I(IC)}=V_{IH}$		−0.02	−20	μA
$R_{I(1)}$	Input resistance, IC, PI, DI, DAK, and TEST	$V_I=V_{SS}$, Ta=25°C	100	180	300	kΩ
$R_{I(2)}$	Input resistance, S, C, SC, CE, and RC	$V_I=V_{DD}$, Ta=25°C	5		30	kΩ
$R_{I(3)}$	Input resistance, K_1～K_{14}	$V_I=V_{SS}$, $V_{I(IC)}=V_{IH}$, Ta=25°C	10	20	40	kΩ
$R_{I(4)}$	Input resistance, K_1～K_{14}	$V_I=V_{DD}$, $V_{I(IC)}=V_{IL}$, Ta=25°C	2	5	15	kΩ
Pd	Power dissipation	Ta=25°C		350	500	mW
Ci	Input capacitance	All terminals except the tested terminal are 0V. V_I=0V, Vrms=25mV, f=1MHz			15	pF

Note 4 : Current flowing into an IC is positive; out is negative.

5 : When all outputs are at I_{OL}=1.6mA, V_{OL}max=0.6V

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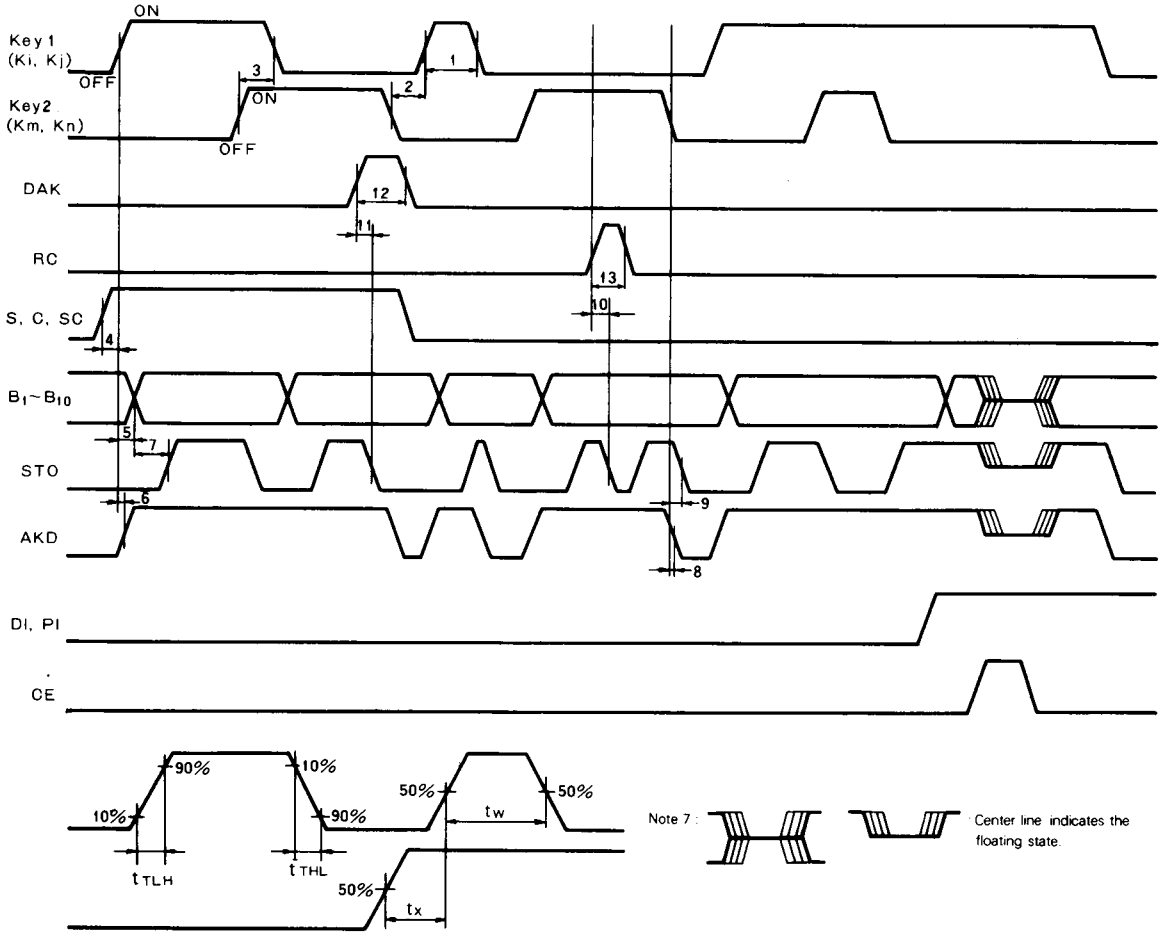
KEYBOARD ENCODER (JIS CODE STANDARD PRODUCT)

SWITCHING CHARACTERISTICS (T_a=25°C, V_{GG}=−12V±10%, V_{DD}=0V, V_{SS}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions (Note 6)	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-to-high-level output transition time	C_L=50pF, I_{OH}=−0.1mA		0.7	2	μs
t_{THL}	High-to-low-level output transition time	C_L=50pF, I_{OL}=1.6mA		0.5	1.5	μs
$t_{w(KI)}$	Key input pulse width	*1, tw	30			μs
$t_{d(KILH-K2HL)}$	Delay time from key 1 low-to-high-level	*2, tx	10			μs
$t_{h(K_1-K_2)}$	Key 1 hold time with respect to key 2	*3, tx	10			μs
$t_{su(M-KON)}$	S. C. SC setup time with respect to key input (ON)	*4, tx			1.5	μs
$t_{D(B-KON)}$	Delay time from key input (ON) to B_1~B_{10}	*5, tx	2	7	15	μs
$t_{D(AK-KON)}$	Delay time from key input (ON) to AKD	*6, tx		0.5	2	μs
$t_{d(ST-B)}$	Delay time from B_1~B_{10} to STO	*7, tx, C_L=50pF, STC-Vss shorted	1	5	12	μs
$t_{D(AK-KOF)}$	Delay time from key input (OFF) to AKD	*8, tx, C_L=50pF		0.5	2	μs
$t_{D(ST-KOF)}$	Delay time from key input (OFF) to STO	*9, tx, C_L=50pF		4	10	μs
$t_{(ST-RC)}$	Delay time from RC to STO	*10, tx, C_L=50pF		3.5	20	μs
$t_{D(ST-DAK)}$	Delay time from DAK to STO	*11, tx, C_L=50pF		4	10	μs
$t_{w(DAK)}$	DAK pulse width	*12, tw	10			μs
$t_{w(RC)}$	RC pulse width	*13, tw	15			μs
$t_{w(STO)}$	STO pulse width	tw, C_L=50pF, STO-DAK shorted	1	4	10	μs

Note 6 : See the Timing Diagram for 'tw' and 'tx'. Numbers 1 through 13 in the diagram correspond to *1 through *13 above.

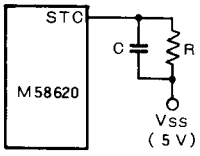
TIMING DIAGRAM



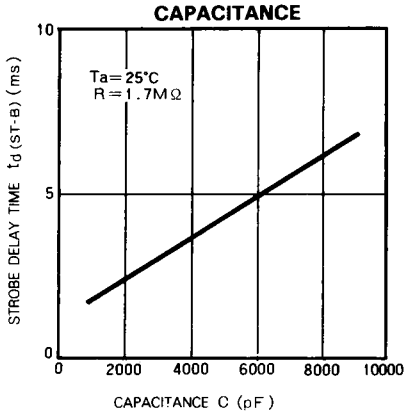
MITSUBISHI ELECTRIC

TYPICAL CHARACTERISTICS ($V_{GG}=-12V$, $V_{DD}=0V$, $V_{SS}=5V$)

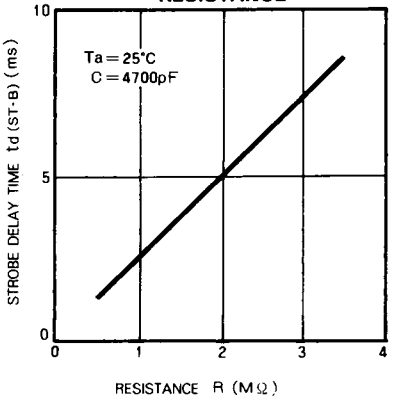
MEASUREMENT CIRCUIT



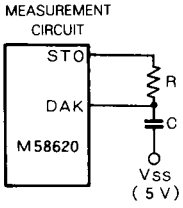
STROBE DELAY TIME VS. CAPACITANCE



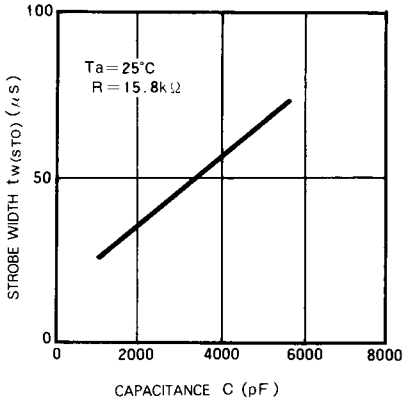
STROBE DELAY TIME VS. RESISTANCE



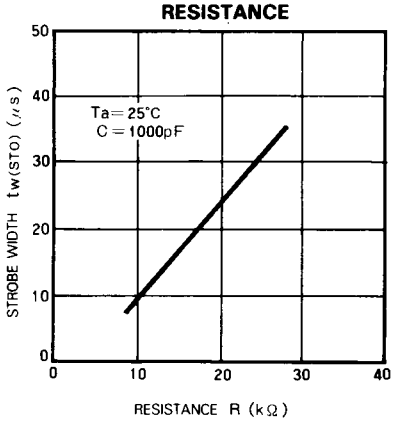
MEASUREMENT CIRCUIT



STROBE WIDTH VS. CAPACITANCE



STROBE WIDTH VS. RESISTANCE



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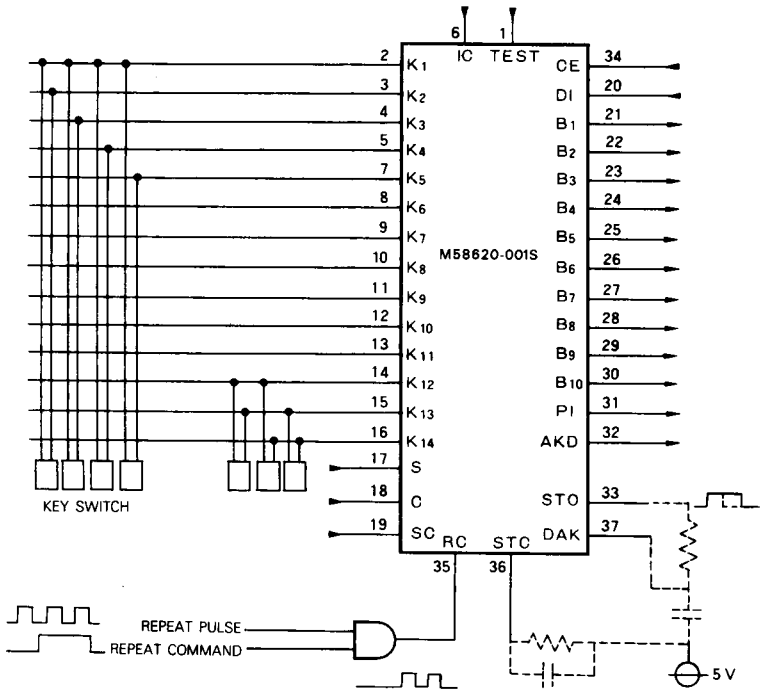
KEYBOARD ENCODER (JIS CODE STANDARD PRODUCT)

TYPICAL APPLICATION CIRCUIT



Note 8 : Use a key switch having outputs that are open-collector, or mutually separated by diodes.