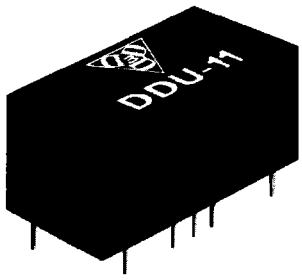
Digital Delay Units

SERIES DDU-11 — 5 Taps ECL Interfaced



Features:

- **Input & Output Buffered**
- **5 Equally Spaced Taps**
- **Fits in Standard 16 Pins DIP**

Specifications:

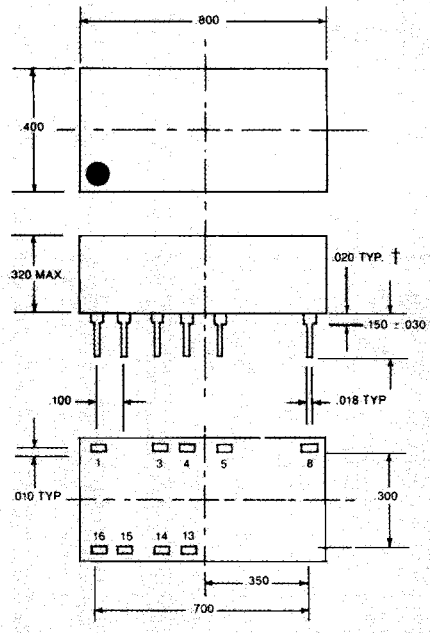
- **Total Delay Tolerance:** ± 5% or better, or 2 ns whichever is greater.
- **No. Taps:** 5 equally spaced.
- **Rise-time:** 2 ns typical.
- **Supply voltage:** -5.2V
- **Operating Temperature:** -30° C to 85° C.
- **Power Dissipation:** -200 mw typ. (no load).
- **Temperature coefficient:** 100 PPM/° C.
- **DC Parameters:** See ECL-10K Logic Table on Page 6.

Part No.	Total Delay (ns)	Delay Tap (ns)
*DDU-11-5	4	1 ± .3
*DDU-11-10	8	2 ± .4
*DDU-11-20	16	4 ± .5
DDU-11-25	25	5 ± 1.0
DDU-11-50	50	10 ± 2.0
DDU-11-75	75	15 ± 2.0
DDU-11-100	100	20 ± 2.0
DDU-11-150	150	30 ± 2.0
DDU-11-200	200	40 ± 2.0
DDU-11-250	250	50 ± 2.5
DDU-11-300	300	60 ± 3.0
DDU-11-400	400	80 ± 4.0
DDU-11-500	500	100 ± 5.0

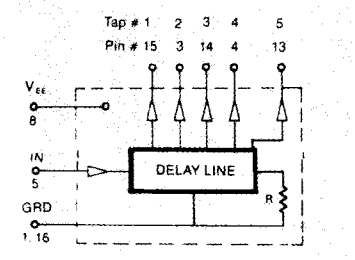
*Time delay measurements referenced to 1st tap. 3.5 ns ± 1 ns inherent delay.

Test Conditions:

- Input pulse-width: 150% of total delay.
- Input pulse rise-time: 6 ns.
- Input pulse voltage: -.7V
- Rise-time measured from 20% to 80% of leading edge.
- Delay time measured at 50% of leading edge.
- All measurements taken @ V_{EE} = -5.2V and T_A = 25° C.
- Unless otherwise specified, all time-delays are referenced to the input pin.



† or case stand-offs



Pull-down resistor on output taps not provided inside unit.

3 Mt. Prospect Avenue, Clifton, New Jersey 07013 ■ (201) 773-2299 ■ FAX (201) 773-9672 ■ TWX 710-989-7008