National Semiconductor

54F/74F784
8-Bit Serial/Parallel Multiplier with Adder/Subtractor

General Description

The 'F784 is an 8-bit by 1-bit sequential logic element that multiplies two numbers represented in twos complement notation. The device implements Booth's algorithm internally to produce a twos complement product that needs no subsequent correction. In addition to the serial product output (SP), an S ± B output is obtained with an internal adder/subtractor stage which adds a B bit to the SP product. Parallel inputs accept and store an 8-bit multiplicand (X_0–X_7). The add/subtract ($\overline{A}$/S), B_n and B_{n-1} inputs control the internal adder/subtractor stage. The multiplier word is then applied to the Y input in a serial bit stream, least significant bit first. The product is clocked out at the SP output and the product ± B at the S ± B output delayed by one clock cycle. Both appear least significant bit first.

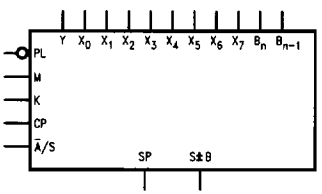
The K input is used for expansion to longer X words, using two or more 'F784 devices by connecting the output (SP) of one device to the K input of the other device. The Mode Control (M) input is used to establish the most significant device. An asynchronous Parallel Load ($\overline{PL}$) input clears the internal flip-flops to the start condition and enables the X latches to accept new multiplicand data. The Parallel Load ($\overline{PL}$) also clears the outputs (SP and S ± B).

Features

- Twos complement multiplication
- 8-bit by 1-bit sequential logic element
- Includes product output (SP) and product ± B output (S ± B)
- Parallel inputs accept and store an 8-bit multiplicand (X_0–X_7)
- K input is used for expansion to longer X words
- Combines the 'F384 and 'F385 in one chip

Ordering Code: See Section 5

Logic Symbol



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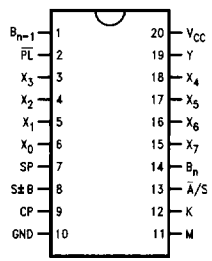
Connection Diagrams

Pin Assignment for DIP and SOIC



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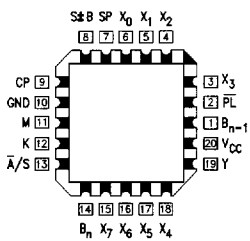
Pin Assignment for LCC



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Input Loading/Fan-Out: See Section 2

Pin Names	Description	54F/74F (U.L.) High/Low	I_{IH}/I_{IL} I_{OH}/I_{OL}
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
K	Serial Expansion Input	1.0/1.0	20 μA/−0.6 mA
M	Mode Control Input	1.0/1.0	20 μA/−0.6 mA
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/2.0	20 μA/−1.2 mA
X_0–X_7	Multiplicand Data Inputs	1.0/1.0	20 μA/−0.6 mA
Y	Serial Multiplier Input	1.0/1.0	20 μA/−0.6 mA
$\overline{A}$/S	Add/Subtract	1.0/1.0	20 μA/−0.6 mA
B_n	Serial B Input	1.0/1.0	20 μA/−0.6 mA
B_{n-1}	Delayed Serial B Input	1.0/1.0	20 μA/−0.6 mA
S ± B	Serial X • Y ± B Output	50/33.3	−1 mA/20 mA
SP	Serial X • Y Product Output	50/33.3	−1 mA/20 mA

Functional Description

The 'F784 is a serial-parallel 8-bit multiplier. Also included is an adder/subtractor stage. The X word (multiplicand) is loaded into a register while simultaneously clearing the arithmetic cell flip-flops in preparation for a multiplication. The Y word (multiplier) is clocked in serially. (See *Figure A*).

Expansion capability is provided via the M and K inputs. The K (cascade) input is connected to the S_0 output of the more significant chip. The M (mode) input is used to determine whether the multiplicand is to be treated as a two's complement or unsigned number.

The 'F784 has logic to enable complex arithmetic to be performed. A serial adder/subtractor enables constants to be added to the product. Typically this feature would be used in FFT butterfly networks to reduce package count and power.

Two outputs are provided: the product XY and the product XY ±B. Because of the internal adder/subtractor, a speed advantage is gained when using the 'F784 over using a separate adder and multiplier chip. (Refer to *Figure B*).

During a multiplication operation, the first clock cycle is used to load both the X word (multiplicand) and the first bit of the Y word (operand) into the input registers. At this time there is no valid data at the SP output so that B bits added will not give the correct sum output. In order to load the first B bit on the same clock as X and Y, a B_{n-1} input is provided which delays the B data by one clock cycle. Thus, a valid output results.

Inputs			Function
$\overline{A}/S$	B_n	B_{n-1}	
L	H	C_n	Add C_n to product (C_n loaded at the same time as Y_n)
L	C_n	H	Add C_n to product (C_n must be delayed one clock cycle)
H	H	C_n	Subtract C_n from product (C_n loaded at the same time as Y_n)
H	C_n	H	Subtract C_n from product (C_n must be delayed one clock cycle)

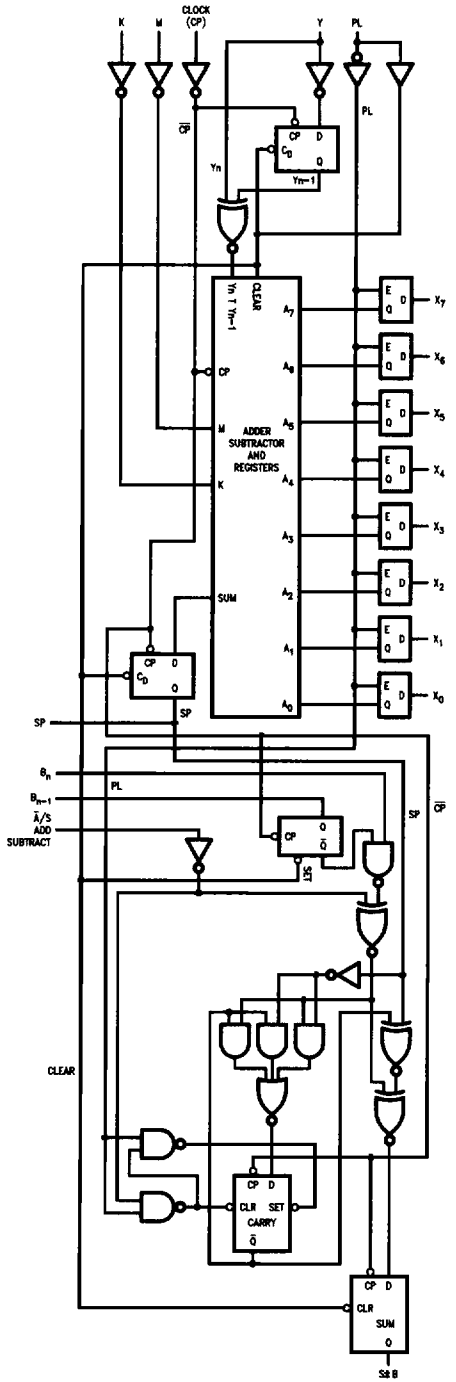
L = LOW Voltage Level H = HIGH Voltage Level C_n = Constant

Function Table

Inputs						Internal	Outputs		Function
$\overline{PL}$	CP	K	M	X_i	Y	Y_{a-1}	SP	S ± B	
X	X	L	L	X	X	X	X	X	Most Significant Multiplier Device
X	X	CS	H	X	X	X	X	X	Devices Cascaded in Multiplier String
L	X	X	X	OP	X	L	L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H	X	X	X	X	X	X	X	X	Device Enabled
H	↑	X	X	X	L	L	P	P ± B	Shift Sum Register
H	↑	X	X	X	L	H	P	P ± B	Add Multiplicand to Sum Register and Shift
H	↑	X	X	X	H	L	P	P ± B	Subtract Multiplicand from Sum Register and Shift
H	↑	X	X	X	H	H	P	P ± B	Shift Sum Register

H = HIGH Voltage Level
L = LOW Voltage Level
↑ = LOW-to-HIGH Transition
CS = Connected to SP output of high order device
OP = X_i latches open for new data (i = 0–7)
P = Output as required per Booth's algorithm
P ± B = Product ± a constant (delayed one clock cycle)
X = Immaterial

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FIGURE A

Timing Waveforms

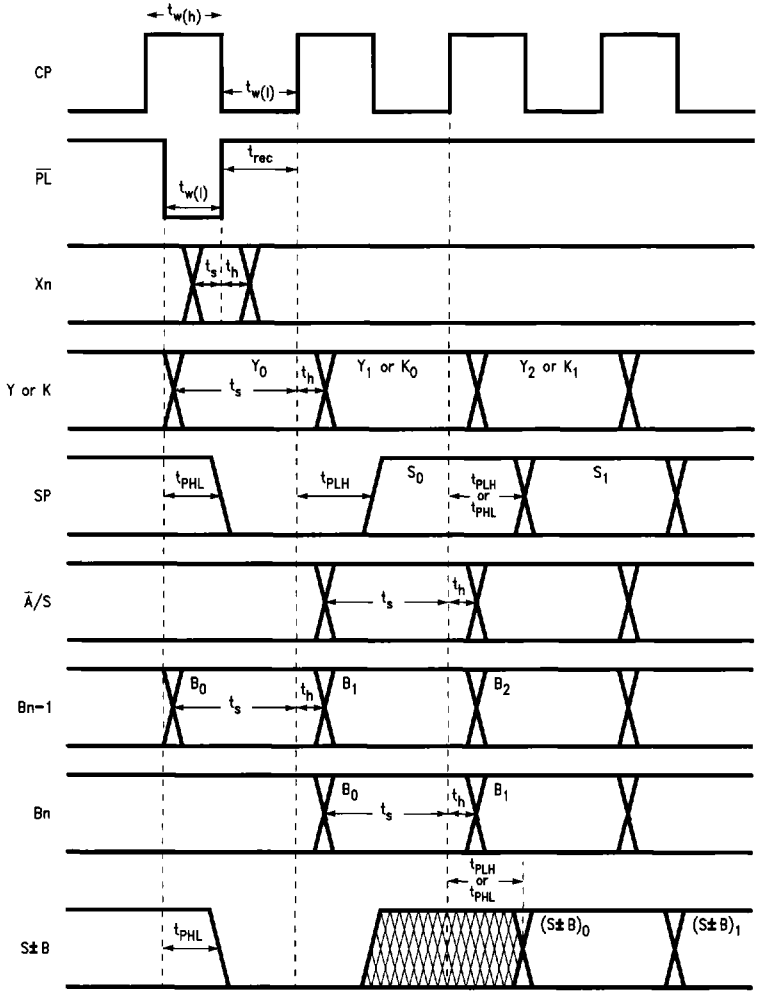

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FIGURE B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (Except $\overline{PL}$)
					−1.2	mA	Max	V_{IN} = 0.5V ($\overline{PL}$)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CC}	Power Supply Current			70	100	mA	Max	V_O = HIGH

AC Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			54F T_A, V_{CC} = Mil $C_L = 50$ pF		74F T_A, V_{CC} = Com $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	50	65				50		MHz	2-1
t_{PHL}	Propagation Delay $\overline{PL}$ to SP	6.0	10.0	13.0			5.0	14.5	ns	2-3
t_{PHL}	Propagation Delay $\overline{PL}$ to S ±B	5.5	9.5	12.0			4.5	13.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay CP to SP	4.0 4.5	6.5 8.0	9.0 10.5			3.5 4.0	10.0 12.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay CP to S ± B	4.0 4.0	7.0 7.0	9.0 9.0			3.5 3.5	10.0 10.0	ns	2-3

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0V$			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW K to CP	9.0 9.0					10.0 10.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW K to CP	2.0 2.0					2.0 2.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Y to CP	15.0 15.0					15.0 15.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Y to CP	2.0 2.0					2.0 2.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW X to $\overline{PL}$	3.0 6.0					4.0 7.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW X to $\overline{PL}$	2.0 4.0					2.0 4.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW B_n to CP	7.0 7.0					8.0 8.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW B_n to CP	0 0					0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A/$\overline{S}$ to CP	12.0 12.0					13.0 13.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A/$\overline{S}$ to CP	0 0					0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW B_{n-1} to CP	5.0 5.0					5.0 5.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW B_{n-1} to CP	1.0 1.0					2.0 2.0			
$t_w(L)$	$\overline{PL}$ Pulse Width, LOW	6.5					7.0		ns	2-4
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	7.0 7.0					7.0 7.0		ns	2-4
t_{rec}	Recovery Time $\overline{PL}$ to CP	6.0					10.0		ns	2-6