

### Description

The [SiT3373](#) is a 220.000001 MHz to 725 MHz differential MEMS VCXO engineered for low-jitter applications. Utilizing SiTime's unique DualMEMS<sup>®</sup> temperature sensing and TurboCompensation<sup>®</sup> technology, the SiT3373 delivers exceptional dynamic performance by providing resistance to airflow, thermal gradients, shock and vibration. This device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for a dedicated external LDO.

The SiT3373 can be factory programmed for any combination of frequency, stability, voltage, output signaling, and pull range. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each frequency is custom built.

The wide frequency range and programmability makes this device ideal for telecom, networking, and industrial applications that require a variety of pullable frequencies and operate in noisy environments.

Refer to [Manufacturing Notes](#) for proper reflow profile, tape and reel dimension, and other manufacturing related information.

### Features

- Any frequency between 220.000001 MHz and 725 MHz accurate to 6 decimal places  
(For frequencies 1 MHz to 220 MHz, refer to [SiT3372](#))
- Widest pull range options:  $\pm 25$ ,  $\pm 50$ ,  $\pm 80$ ,  $\pm 100$ ,  $\pm 150$ ,  $\pm 200$ ,  $\pm 400$ ,  $\pm 800$ ,  $\pm 1600$ ,  $\pm 3200$  ppm
- 0.225 ps RMS phase jitter (typ) over 12 kHz to 20 MHz bandwidth
- Frequency stability as low as  $\pm 15$  ppm
- Wide temperature range support from  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$
- Industry-standard packages: 7.0 x 5.0 mm, 5.0 x 3.2 mm, 3.2 x 2.5 mm packages

### Applications

- Cable Modem Termination System (CMTS), Video, Broadcasting System, Audio, Industrial Sensors, Remote Radio Head (RRH)
- SATA, SAS, 10/40/100/400 Gbps Ethernet, Fibre Channel, PCI-Express
- Optical Transport Network (OTN)

INSTANT SAMPLES	SEARCH INVENTORY	GREEN SOLUTIONS	LIFETIME WARRANTY

### Block Diagram

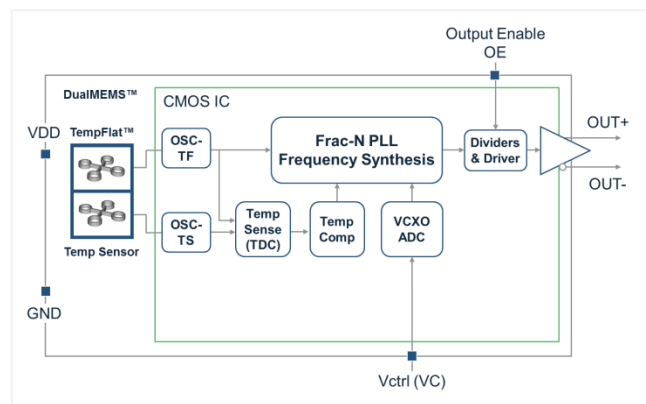


Figure 1. SiT3373 Block Diagram

### 3.2 x 2.5 mm Package Pinout

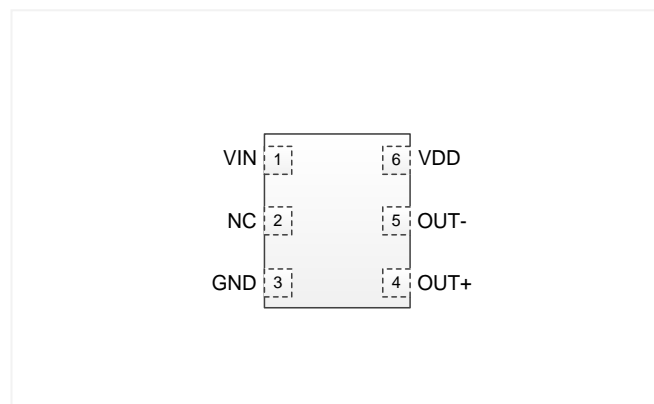
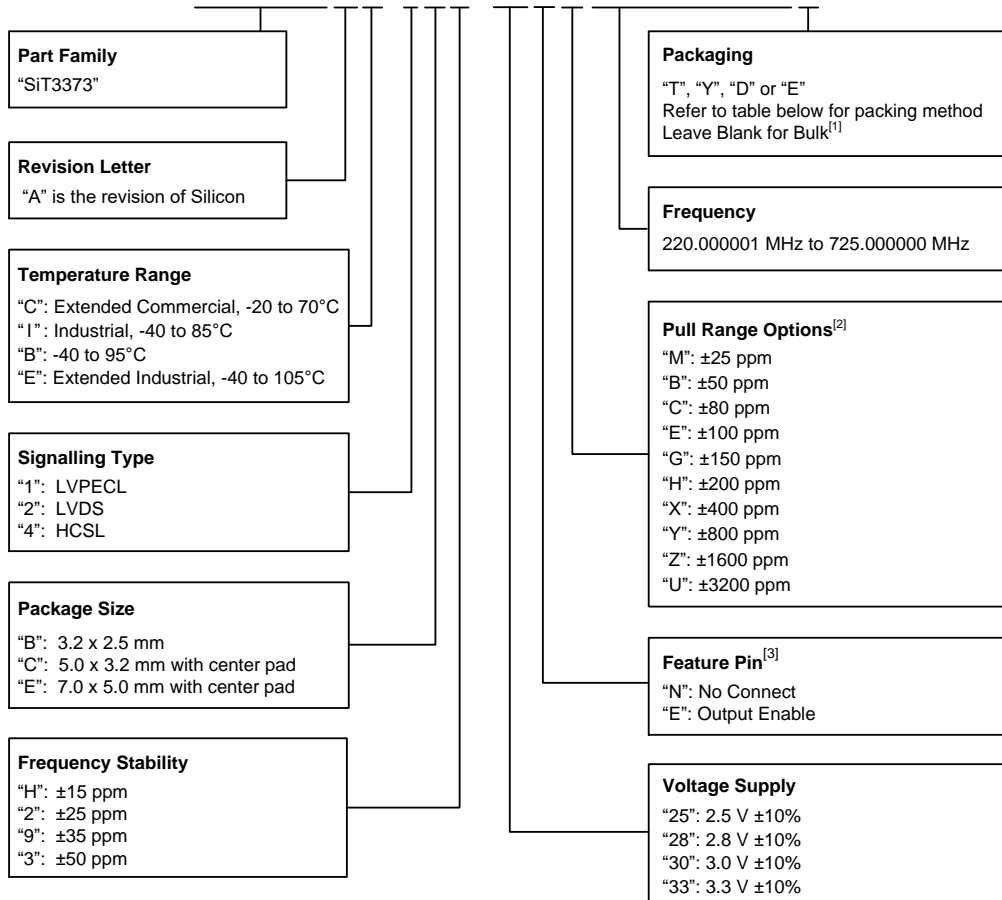


Figure 2. Pin Assignments (Top view)  
(Refer to [Table 6](#) for Pin Descriptions)

Ordering Information

SiT3373AC-1B2-33NH220.123456T



Notes:

1. Bulk is available for sampling only.
2. Contact SiTime for custom pull range options.
3. "E": Output Enable function is only available in 7.0 x 5.0 mm and 5.0 x 3.2 mm packages.

Table 1. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0	-	-	-	-	T	Y
5.0 x 3.2	-	-	T	Y	-	-
3.2 x 2.5	D	E	T	Y	-	-

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## Electrical Characteristics

**Table 2. Electrical Characteristics – Common to LVPECL, LVDS and HCSL**

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Frequency Range</b>						
<b>Output Frequency Range</b>	f	220.000001	–	725	MHz	Accurate to 6 decimal places
<b>Frequency Stability</b>						
<b>Frequency Stability</b>	F_stab	-15	–	+15	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variations, and first year aging at 25°C, with VIN voltage at Vdd/2. ±15 ppm is only guaranteed for pull range up to ±100 ppm.
		-25	–	+25	ppm	
		-35	–	+35	ppm	
		-50	–	+50	ppm	
<b>Temperature Range</b>						
<b>Operating Temperature Range</b>	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
		-40	–	+95	°C	
		-40	–	+105	°C	Extended Industrial
<b>Supply Voltage</b>						
<b>Supply Voltage</b>	Vdd	2.97	3.30	3.63	V	
		2.70	3.00	3.30	V	
		2.52	2.80	3.08	V	
		2.25	2.50	2.75	V	
<b>Voltage Control Characteristics</b>						
<b>Pull Range</b>	PR	±25, ±50, ±80, ±100, ±150, ±200, ±400, ±800, ±1600, ±3200			ppm	See the APR (Absolute Pull Range) <a href="#">Table 11</a> . <a href="#">Contact SiTime</a> for custom pull range options
<b>Upper Control Voltage</b>	VC_U	90%	–	–	Vdd	Voltage at which maximum frequency deviation is guaranteed
<b>Lower Control Voltage</b>	VC_L	–	–	10%	Vdd	Voltage at which minimum frequency deviation is guaranteed
<b>Control Voltage Input Impedance</b>	VC_z	–	10	–	MΩ	
<b>Control Voltage Input Bandwidth</b>	V_c	–	10	–	kHz	<a href="#">Contact SiTime</a> for other input bandwidth options
<b>Pull Range Linearity</b>	Lin	–	–	1.0	%	
<b>Frequency Change Polarity</b>	–	Positive Slope			–	
<b>Input Characteristics</b>						
<b>Input Voltage High</b>	VIH	70%	–	–	Vdd	Pin 2, OE
<b>Input Voltage Low</b>	VIL	–	–	30%	Vdd	Pin 2, OE
<b>Input Pull-up Impedance</b>	Z_in	–	100	–	kΩ	Pin 2, OE logic high or logic low
<b>Output Characteristics</b>						
<b>Duty Cycle</b>	DC	45	–	55	%	
<b>Startup and OE Timing</b>						
<b>Start-up Time</b>	T_start	–	–	3.0	ms	Measured from the time Vdd reaches its rated minimum value.
<b>OE Enable/Disable Time</b>	T_oe	–	–	3.8	μs	f = 322.265625 MHz. Measured from the time OE pin reaches rated VIH and VIL to the time clock pins reach 90% of swing and high-Z. See <a href="#">Figure 9</a> and <a href="#">Figure 10</a>

**Table 3. Electrical Characteristics – LVPECL Specific**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Current Consumption</b>						
Current Consumption	I <sub>dd</sub>	–	–	97	mA	Excluding Load Termination Current, V <sub>dd</sub> = 3.3 V or 2.5 V
OE Disable Supply Current	I <sub>OE</sub>	–	–	63	mA	OE = Low
Output Disable Leakage Current	I <sub>leak</sub>	–	0.15	–	μA	OE = Low
Maximum Output Current	I <sub>driver</sub>	–	–	32	mA	Maximum average current drawn from OUT+ or OUT-
<b>Output Characteristics</b>						
Output High Voltage	VOH	V <sub>dd</sub> -1.15	–	V <sub>dd</sub> -0.7	V	See <a href="#">Figure 5</a>
Output Low Voltage	VOL	V <sub>dd</sub> -1.9	–	V <sub>dd</sub> -1.5	V	See <a href="#">Figure 5</a>
Output Differential Voltage Swing	V <sub>Swing</sub>	1.2	1.6	2.0	V	See <a href="#">Figure 6</a>
Rise/Fall Time	T <sub>r</sub> , T <sub>f</sub>	–	225	290	ps	20% to 80%, see <a href="#">Figure 6</a>
<b>Jitter – 7.0 x 5.0 mm Package</b>						
RMS Period Jitter <sup>[4]</sup>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 322.265625 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.220	0.270	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs, pull range = ±100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.220	0.300	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs, pull range = ±100 ppm. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all V <sub>dd</sub> levels
<b>Jitter – 5.0 x 3.2 mm and 3.2 x 2.5 mm Packages</b>						
RMS Period Jitter <sup>[4]</sup>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 322.265625 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.225	0.282	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs, pull range = ±100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.225	0.315	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs, pull range = ±100 ppm. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all V <sub>dd</sub> levels

**Notes:**

4. Measured according to JESD65B.

Table 4. Electrical Characteristics – LVDS Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Current Consumption</b>						
Current Consumption	I <sub>dd</sub>	–	–	89	mA	Excluding Load Termination Current, V <sub>dd</sub> = 3.3 V or 2.5 V
OE Disable Supply Current	I <sub>OE</sub>	–	–	67	mA	OE = Low
Output Disable Leakage Current	I <sub>leak</sub>	–	0.15	–	μA	OE = Low
<b>Output Characteristics</b>						
Differential Output Voltage	V <sub>OD</sub>	250	–	450	mV	See <a href="#">Figure 7</a>
Delta VOD	ΔV <sub>OD</sub>	–	–	50	mV	See <a href="#">Figure 7</a>
Offset Voltage	V <sub>OS</sub>	1.125	–	1.375	V	See <a href="#">Figure 7</a>
Delta VOS	ΔV <sub>OS</sub>	–	–	50	mV	See <a href="#">Figure 7</a>
Rise/Fall Time	T <sub>r</sub> , T <sub>f</sub>	–	370	470	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see <a href="#">Figure 8</a>
<b>Jitter – 7.0 x 5.0 mm package</b>						
RMS Period Jitter <sup>[5]</sup>	T <sub>jitt</sub>	–	0.92	1.6	ps	f = 322.265625 MHz, V <sub>dd</sub> = 3.3V or 2.5V
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.215	0.265	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs, pull range = ±100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.215	0.280	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs, pull range = ±100 ppm. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels
<b>Jitter – 5.0 x 3.2 mm and 3.2 x 2.5 mm packages</b>						
RMS Period Jitter <sup>[5]</sup>	T <sub>jitt</sub>	–	0.92	1.6	ps	f = 322.265625 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.235	0.282	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs, pull range = ±100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.235	0.310	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs, pull range = ±100 ppm. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels

**Notes:**

5. Measured according to JESD65B.

**Table 5. Electrical Characteristics – HCSL Specific**

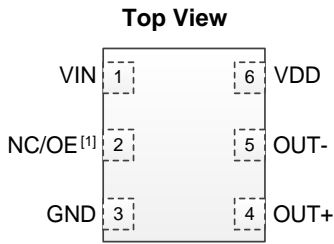
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Current Consumption</b>						
<b>Current Consumption</b>	I <sub>dd</sub>	–	–	102	mA	Excluding Load Termination Current, V <sub>dd</sub> = 3.3 V or 2.5 V
<b>OE Disable Supply Current</b>	I <sub>OE</sub>	–	–	67	mA	OE = Low
<b>Output Disable Leakage Current</b>	I <sub>leak</sub>	–	0.15	–	μA	OE = Low
<b>Output Characteristics</b>						
<b>Output High Voltage</b>	V <sub>OH</sub>	0.6	–	0.90	V	See <a href="#">Figure 5</a>
<b>Output Low Voltage</b>	V <sub>OL</sub>	-0.05	–	0.08	V	See <a href="#">Figure 5</a>
<b>Output Differential Voltage Swing</b>	V <sub>Swing</sub>	1.2	1.4	1.8	V	See <a href="#">Figure 6</a>
<b>Rise/Fall Time</b>	T <sub>r</sub> , T <sub>f</sub>	–	360	470	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see <a href="#">Figure 6</a>
<b>Jitter – 7.0 x 5.0 mm package</b>						
<b>RMS Period Jitter<sup>[6]</sup></b>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 322.265625 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
<b>RMS Phase Jitter (random)</b>	T <sub>phj</sub>	–	0.215	0.265	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs, Pull Range = ±100 ppm
		–	0.215	0.282	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs, pull range = ±100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels
<b>Jitter – 5.0 x 3.2 mm and 3.2 x 2.5 mm packages</b>						
<b>RMS Period Jitter<sup>[6]</sup></b>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 322.265625 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
<b>RMS Phase Jitter (random)</b>	T <sub>phj</sub>	–	0.235	0.282	0.215	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs, pull range = ±100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.235	0.305	0.215	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs, pull range = ±100 ppm. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	0.1	f = 322.265625 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels

**Notes:**

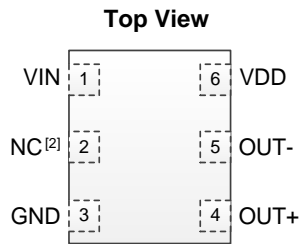
6. Measured according to JESD65B.

**Table 6. Pin Description**

Pin	Symbol		Functionality
1	VIN	Input	Control Voltage
2	NC/OE	No Connect (NC)	No Connect: Leave floating or connect to GND for better heat dissipation. NC for all 3.2 x 2.5 mm package options.
		Output Enable (OE)	H <sup>[7,8]</sup> : specified frequency output L: output is high impedance. Only output driver is disabled. OE function only available on 7050 and 5032 packages. Pin 2 on 3225 package is NC.
3	GND	Power	Vdd Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage <sup>[9]</sup>



**Figure 3. Pin Assignments (7.0 x 5.0 mm and 5.0 x 3.2 mm packages)**



**Figure 4. Pin Assignments (3.2 x 2.5 mm package)**

**Notes:**

- 7. A pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
- 8. OE mode is only available in the 7050 and 5032 packages. 3225 package is NC.
- 9. A capacitor of value 0.1 μF or higher between VDD and GND is required. An additional 10 μF capacitor between VDD and GND is required for the best phase jitter performance.

**Table 7. Absolute Maximum Ratings**

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Continuous Power Supply Voltage Range (V <sub>dd</sub> )	-0.5	4.0	V
Input Voltage, Maximum (any input pin)		V <sub>dd</sub> + 0.3V	V
Input Voltage, Minimum (any input pin)	-0.3		V
Storage Temperature	-65	150	°C
Maximum Junction Temperature		145	°C
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C

**Table 8. Thermal Considerations<sup>[10]</sup>**

Package	$\theta_{JA}$ , 4 Layer Board (°C/W)	$\theta_{JC}$ , Bottom (°C/W)
3225, 6-pin	80	30
5032, 6-pin	53 <sup>[11]</sup>	20
7050, 6-pin	52 <sup>[11]</sup>	19

**Notes:**

10. Refer to JESD51 for  $\theta_{JA}$  and  $\theta_{JC}$  definitions, and reference layout used to determine the  $\theta_{JA}$  and  $\theta_{JC}$  values in the above table.  
 11. Value for  $\theta_{JA}$  assumes the center pad is soldered down.

**Table 9. Maximum Operating Junction Temperature<sup>[12]</sup>**

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature: 3225 Package	Maximum Operating Junction Temperature: 5032, 7050 Packages
70°C	105°C	95°C
85°C	130°C	110°C
95°C	130°C	120°C
105°C	145°C	130°C

**Notes:**

12. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

**Table 10. Environmental Compliance**

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	<i>g</i>
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	<i>g</i>
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

### Waveform Diagrams

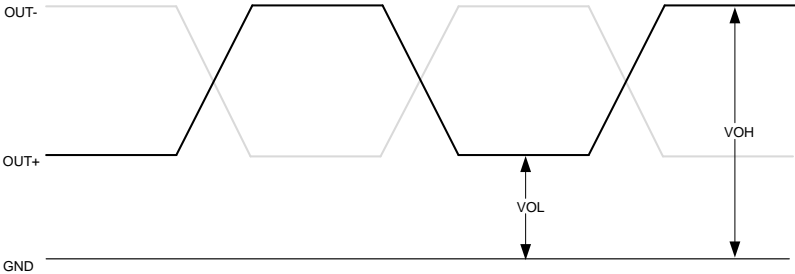


Figure 5. LVPECL, HCSL Voltage Levels per Differential Pin (i.e. OUT+, or OUT-)

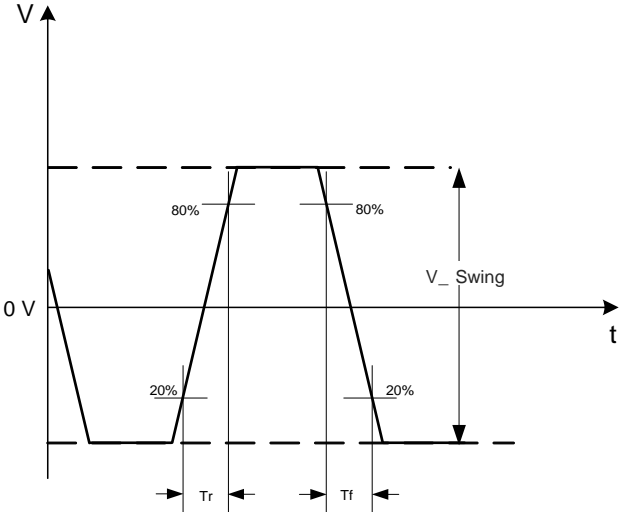
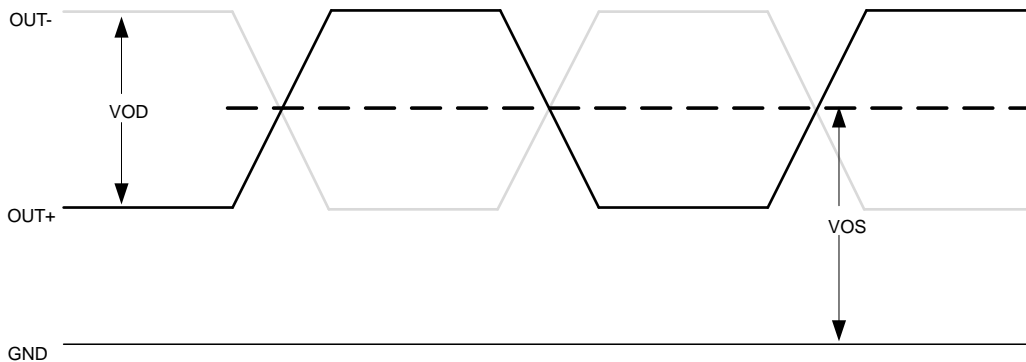
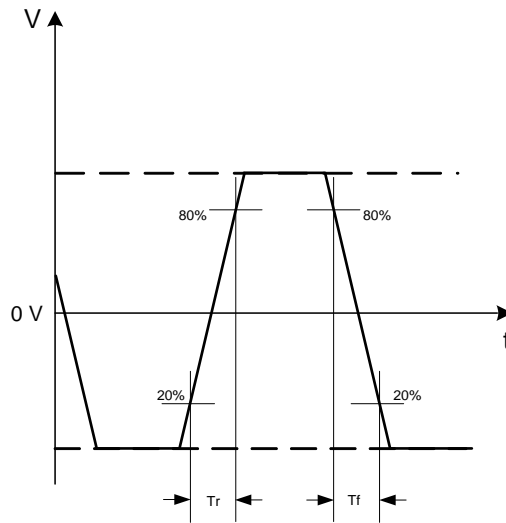


Figure 6. LVPECL, HCSL Voltage Levels across Differential Pair (i.e. OUT+ minus OUT-)

**Waveform Diagrams (continued)**

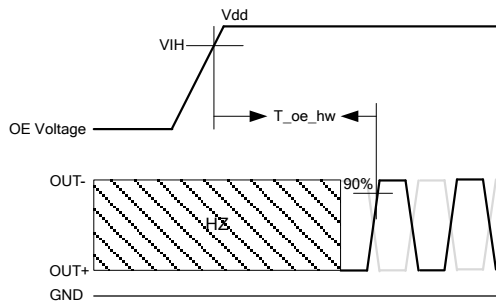


**Figure 7. LVDS Voltage Levels per Differential Pin (i.e. OUT+, or OUT-)**

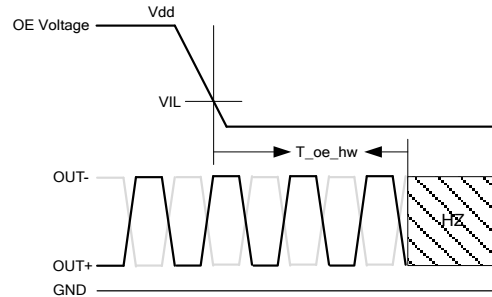


**Figure 8. LVDS Differential Waveform (i.e. OUT+ minus OUT-)**

**Timing Diagrams**



**Figure 9. Hardware OE Enable Timing**



**Figure 10. Hardware OE Disable Timing**

## Termination Diagrams

### LVPECL

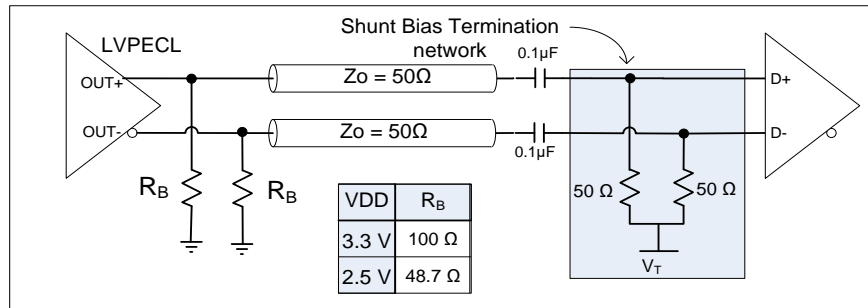


Figure 11. LVPECL with AC-coupled termination

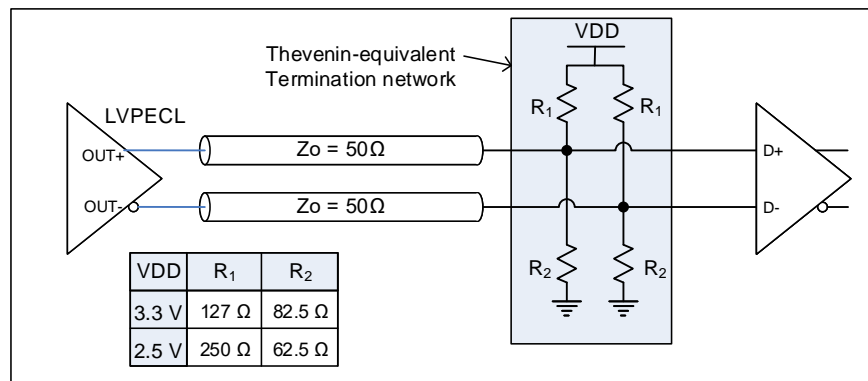


Figure 12. LVPECL DC-coupled load termination with Thevenin equivalent network

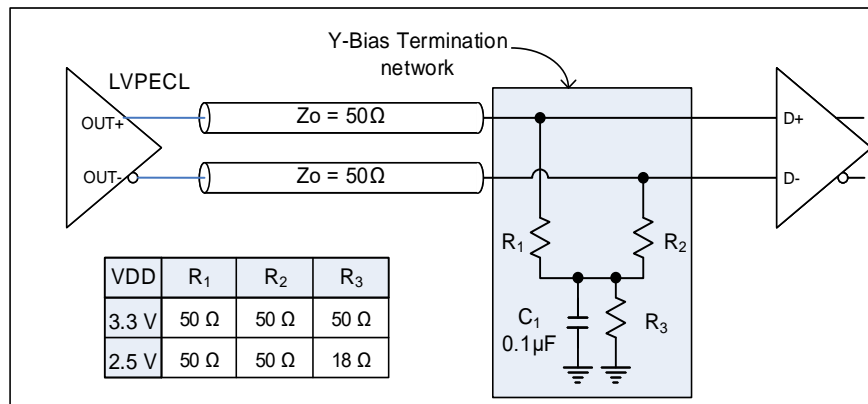


Figure 13. LVPECL with Y-Bias termination

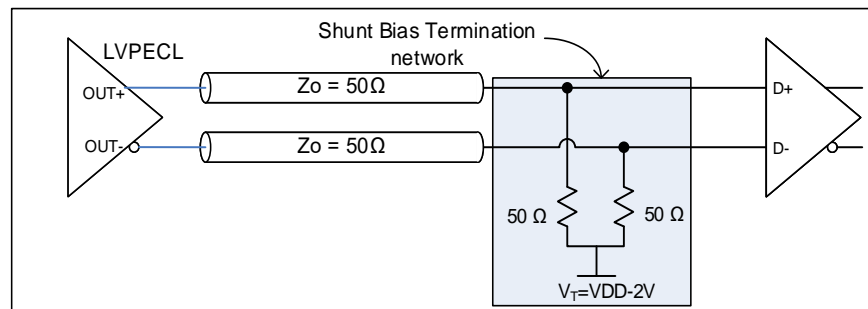
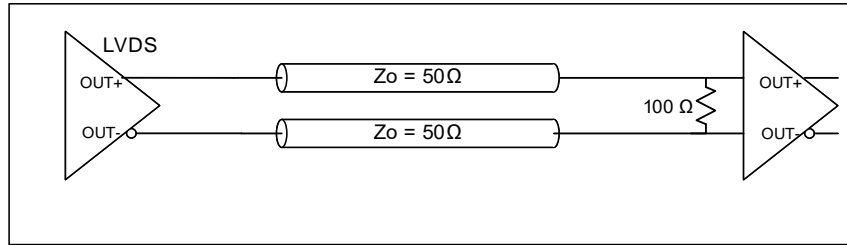


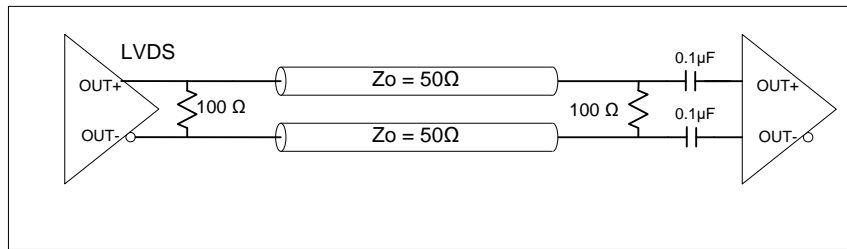
Figure 14. LVPECL with DC-coupled parallel shunt load termination

**Termination Diagrams (continued)**

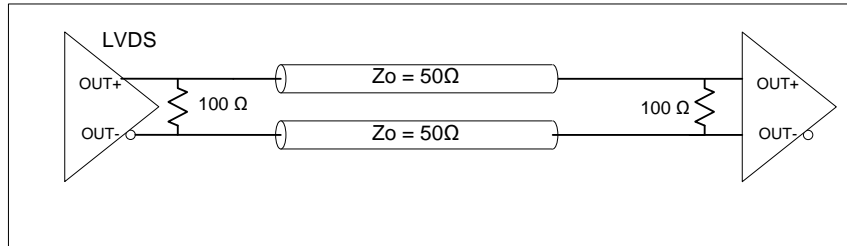
**LVDS**



**Figure 15. LVDS single DC termination at the load**

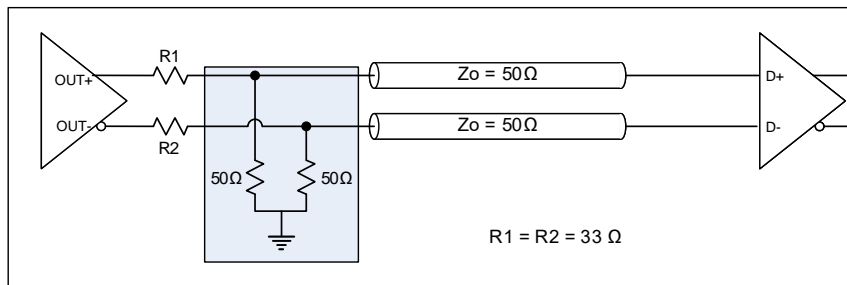


**Figure 16. LVDS double AC termination with capacitor close to the load**



**Figure 17. LVDS double DC termination**

**HCSL**



**Figure 18. HCSL interface termination**

### Dimensions and Patterns — 3.2 x 2.5 mm

Package Size – Dimensions (Unit: mm) <sup>[13]</sup>	Recommended Land Pattern (Unit: mm) <sup>[14]</sup>																																																																																		
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### Dimensions and Patterns — 5.0 x 3.2 mm

Package Size – Dimensions (Unit: mm) <sup>[13]</sup>	Recommended Land Pattern (Unit: mm) <sup>[14]</sup>																																																																																											
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## Dimensions and Patterns — 7.0 x 5.0 mm

Package Size – Dimensions (Unit: mm) <sup>[16]</sup>	Recommended Land Pattern (Unit: mm) <sup>[17]</sup>																																																																																						
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**Table 11. APR Table**

Absolute pull range (APR) = Nominal pull range (PR) - frequency stability (F\_stab) - aging<sup>19</sup>

Nominal Pull Range	Frequency Stability			
	±15	±25	±35	±50
	APR (ppm)			
±25	±5	—	—	—
±50	±30	±20	±10	—
±80	±60	±50	±40	±25
±100	±80	±70	±60	±45
±150	—	±120	±110	±95
±200	—	±170	±160	±145
±400	—	±370	±360	±345
±800	—	±770	±760	±745
±1600	—	±1570	±1560	±1545
±3200	—	±3170	±3160	±3145

**Note:**

19. Aging includes solder down shift and 20-year aging.

**Additional Information**

**Table 12. Additional Information**

Document	Description	Download Link
<b>ECCN #: EAR99</b>	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
<b>HTS Classification Code: 8542.39.0000</b>	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
<b>Part number Generator</b>	Tool used to create the part number based on desired features.	<a href="https://www.sitime.com/part-number-generator">https://www.sitime.com/part-number-generator</a>
<b>Time Machine II</b>	MEMS oscillator programmer	<a href="http://www.sitime.com/support/time-machine-oscillator-programmer">http://www.sitime.com/support/time-machine-oscillator-programmer</a>
<b>Manufacturing Notes</b>	Tape & Reel dimension, reflow profile and other manufacturing related info	<a href="https://www.sitime.com/sites/default/files/gated/Manufacturing-Notes-for-SiTime-Products.pdf">https://www.sitime.com/sites/default/files/gated/Manufacturing-Notes-for-SiTime-Products.pdf</a>
<b>Qualification Reports</b>	RoHS report, reliability reports, composition reports	<a href="http://www.sitime.com/support/quality-and-reliability">http://www.sitime.com/support/quality-and-reliability</a>
<b>Performance Reports</b>	Additional performance data such as phase noise, current consumption, and jitter for selected frequencies	<a href="http://www.sitime.com/support/performance-measurement-report">http://www.sitime.com/support/performance-measurement-report</a>
<b>Termination Techniques</b>	AN10029 Termination design recommendations	<a href="http://www.sitime.com/support/application-notes">http://www.sitime.com/support/application-notes</a>
<b>Layout Techniques</b>	AN10006 Layout recommendations	<a href="http://www.sitime.com/support/application-notes">http://www.sitime.com/support/application-notes</a>
<b>Evaluation Boards</b>	SiT6085EB, SiT6086EB and SiT6097EB for Differential Oscillators	<a href="https://www.sitime.com/support/user-guides">https://www.sitime.com/support/user-guides</a>

## Revision History

Table 13. Revision History

Revision	Release Date	Change Summary
1.0	10/13/2017	Initial release
1.01	02/02/2018	Corrected ppm ordering codes. Corrected minor formatting errors. Added Additional Information table. Added Extended Industrial temperature range (-40°C – 95°C and -40°C – 105°C )
1.03	05/10/2018	Updated the Part Ordering info with added 5.0 x 3.2 mm package
1.04	10/29/2018	±15 ppm option
1.05	06/07/2020	Formatting updates Corrected typos Updated package Dimensions Drawings Updated Table 8 Thermal Considerations for 5032 package Added Evaluation Boards SiT6085EB reference in Additional Information Rearranged layout, added Description, Block Diagram and TOC Added HTS classification code Clarified ±15 ppm pull range up to ±100 ppm Modified maximum junction temperatures Removed I_driver HCSL specification as not applicable
1.06	17-Mar-2021	Updated L1 and Dimple Width package dimensions for 3.2 x 2.5 mm package Updated trademarks and changed rev table date format

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