Product Preview

HSTL Low Voltage Differential Clock

MPC9994

HSTL LOW VOLTAGE DIFFERENTIAL CLOCK SYNTHESIZER FOR 340 – 640 MHZ

The MPC9994 is a low voltage 3.3V, HSTL differential clock synthesizer. The clock is designed to support single and multiple processor systems requiring HSTL differential inputs. The MPC9994 supports two differential HSTL output pairs that may be operated from 340 MHz to 640 MHz.

Features:

- 2 clock outputs: (PCLK0 and PCLK1), each fully selectable
- Fully integrated PLL
- Output frequencies from 340 MHz to 640 MHz
- HSTL outputs
- HSTL and LVPECL reference clocks
- 32 lead LQFP packaging

4

The fully integrated Phase Locked Loop multiplies the HSTL_CLK input or the PECL_CLK input frequency to the desired processor clock frequency.

The PLL may be bypassed for test purposes such that the PCLK outputs are fed directly from the HSTL_CLK or PECL_CLK input.

All outputs are HSTL. The PCLK outputs are capable of driving 25Ω to ground with at least 600mV p-p signals. The EXTFB_OUT is capable of driving 50Ω ground with at least a 600 mV p-p signal. For on-chip power reduction, the outputs are powered from 1.8V external supply. For zero delay applications the buffer can operate with either external or internal feedback.

FA SUFFIX
LQFP PACKAGE
CASE 873A

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.
Rev 1

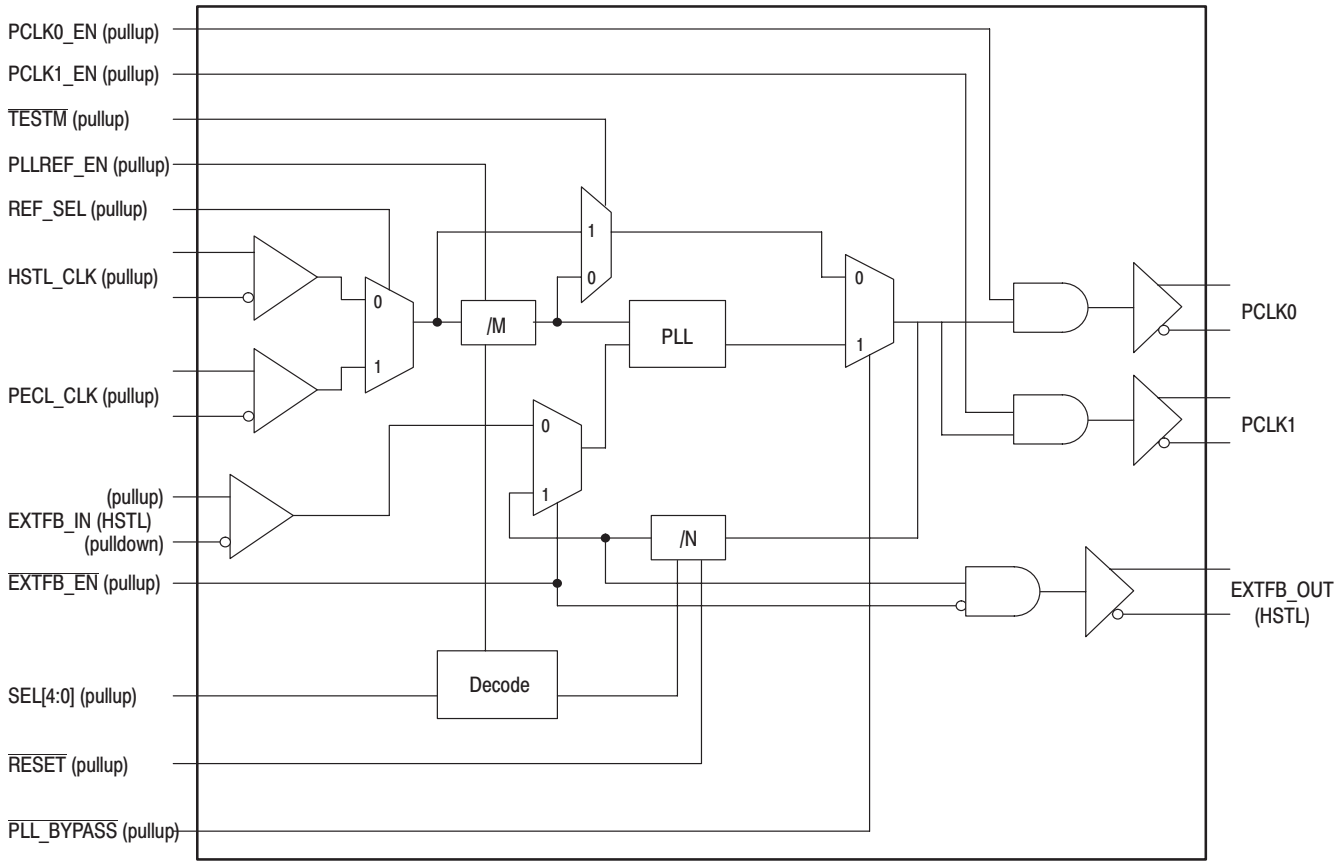

Figure 1. MPC9994 Logic Diagram

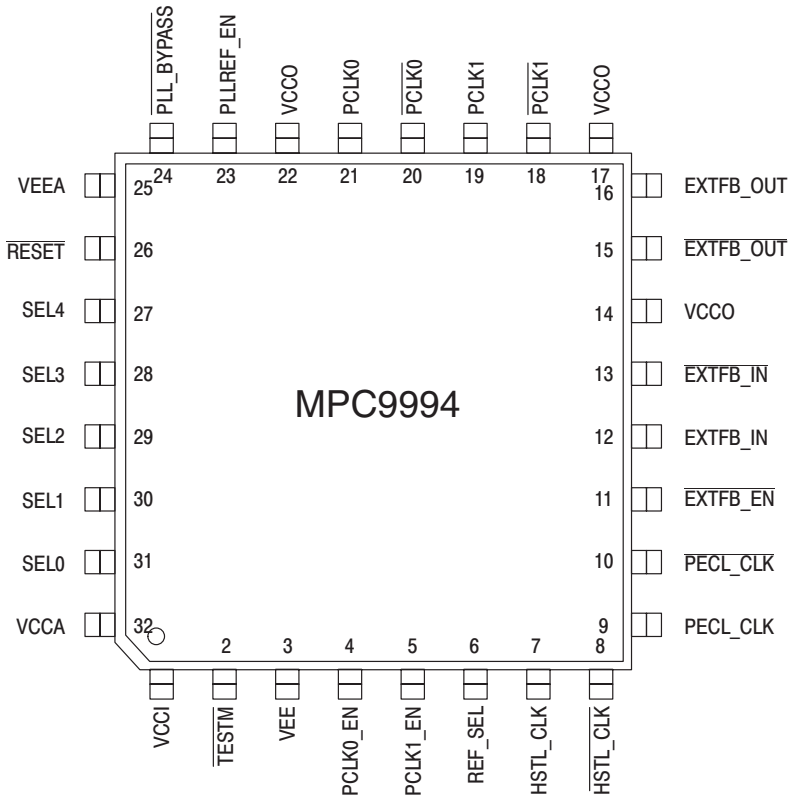

Figure 2. 32 Lead Package Pinout (Top View)

PIN CONFIGURATION

Pin #	Pin	I/O Type	Type	Description
1	VCCI	Power	Power Supply	3.3 V
2	$\overline{\text{TESTM}}$	Input	LVCMOS	M divider test pins
3	VEE	Power (GND)	Ground	Digital GND
4	PCLK0_EN	Input	LVCMOS	PCLK0 enable
5	PCLK1_EN	Input	LVCMOS	PCLK1 enable
6	REF_SEL	Input	LVCMOS	Selects the PLL input reference clock
7	HSTL_CLK	Input	Differential HSTL	PLL reference clock input
8	$\overline{\text{HSTL\_CLK}}$	Input	Differential HSTL	PLL reference clock input
9	PECL_CLK	Input	Differential LVPECL	PLL reference clock input
10	$\overline{\text{PECL\_CLK}}$	Input	Differential LVPECL	PLL reference clock input
11	$\overline{\text{EXTFB\_EN}}$	Input	LVCMOS	External feedback enable
12	EXTFB_IN	Input	Differential HSTL	External feedback input
13	$\overline{\text{EXTFB\_IN}}$	Input	Differential HSTL	External feedback input
14	VCCO	Power	Power Supply	Output buffers power supply
15	$\overline{\text{EXTFB\_OUT}}$	Output	Differential HSTL	External feedback output clock
16	EXTFB_OUT	Output	Differential HSTL	External feedback output clock
17	VCCO	Power	Power Supply	Ouput buffers power supply
18	$\overline{\text{PCLK1}}$	Output	Differential HSTL	Output clock 1
19	PCLK1	Output	Differential HSTL	Output clock 1
20	$\overline{\text{PCLK0}}$	Output	Differential HSTL	Output clock 0
21	PCLK0	Output	Differential HSTL	Output clock 0
22	VCCO	Power	Power Supply	Ouput buffers power supply
23	PLLREF_EN	Input	LVCMOS	PLL reference enable
24	$\overline{\text{PLL\_BYPASS}}$	Input	LVCMOS	Input signal PLL bypass
25	VEEA	Power (GND)	Ground	Analog GND for PLL
26	$\overline{\text{RESET}}$	Input	LVCMOS	PLL bypass reset (for test use)
27	SEL[4]	Input	LVCMOS	Selection of input and feedback frequency
28	SEL[3]	Input	LVCMOS	Selection of input and feedback frequency
29	SEL[2]	Input	LVCMOS	Selection of input and feedback frequency
30	SEL[1]	Input	LVCMOS	Selection of input and feedback frequency
31	SEL[0]	Input	LVCMOS	Selection of input and feedback frequency
32	VCCA	Power	Power Supply	3.3 V filtered for PLL (PLL power supply)

FREQUENCY SELECTION TABLE

SEL					Input Divide	Feedback Divide
4	**3**	**2**	**1**	**0**	**M**	**N**
0	0	0	0	0	5	16
0	0	0	0	1	5	17
0	0	0	1	0	5	18
0	0	0	1	1	5	19
0	0	1	0	0	5	20
0	0	1	0	1	5	21
0	0	1	1	0	5	22
0	0	1	1	1	5	23
0	1	0	0	0	5	24
0	1	0	0	1	5	25
0	1	0	1	0	5	26
0	1	0	1	1	5	27
0	1	1	0	0	5	28
0	1	1	0	1	5	29
0	1	1	1	0	5	30
0	1	1	1	1	5	31
1	0	0	0	0	5	32
1	0	0	0	1	5	33
1	0	0	1	0	5	34
1	0	0	1	1	5	35
1	0	1	0	0	5	36
1	0	1	0	1	5	37
1	0	1	1	0	5	38
1	0	1	1	1	5	39
1	1	0	0	0	5	40
1	1	0	0	1	5	41
1	1	0	1	0	5	42
1	1	0	1	1	5	43
1	1	1	0	0	5	44
1	1	1	0	1	5	45
1	1	1	1	0	5	46
1	1	1	1	1	5	47

FUNCTION TABLE (CONTROLS)

Control Pin	0	1
REF_SEL	HSTL_CLK	PECL_CLK
$\overline{\text{TESTM}}$	M divider test mode enabled	Reference fed to Bypass mux
PLLREF_EN	Disable the input to the PLL and reset the M divider	Enable the input to the PLL
$\overline{\text{PLL\_BYPASS}}$	Outputs fed by input reference or M divider	Outputs fed by VCO
$\overline{\text{EXTFB\_EN}}$	External feedback enabled	Internal feedback enabled
PCLK0_EN	PCLK0 = low, $\overline{\text{PCLK0}}$ = high	PCLK0 = high, $\overline{\text{PCLK0}}$ = low
PCLK1_EN	PCLK1 = low, $\overline{\text{PCLK1}}$ = high	PCLK1 = high, $\overline{\text{PCLK1}}$ = low
$\overline{\text{RESET}}$	Resets feedback N divider	Feedback enabled
SEL[4:0]	See Selection Frequency Table	

ABSOLUTE MAXIMUM RATINGS*

4

Symbol	Characteristics	Min	Max	Unit	Condition
VCC	Supply Voltage	-0.5	4.4	V	
VCCO	Output Supply Voltage	-0.5	4.4	V	
VIN	Input Voltage	-0.5	VCC+0.3	V	
IIN	Input Current	-1	1	mA	
TS	Storage temperature	-50	150	°C	

NOTE: Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS (VCCA=VCCI = 3.3V ± 5%, VCCO = 1.7 to 2.1V, TA = 0 to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
VIH	Input high voltage	2.0		VCCI	V	LVCMOS
VIL	Input low voltage	0.0		0.8	V	LVCMOS
VCMR	Input high voltage[a]	1		VCCI - 0.3	V	LVPECL
VPP	Input low voltage[a]	0.5		1	V	LVPECL[b]
V_{IN} (dc)	DC input signal voltage	-0.3		1.45	V	HSTL[c]
V_{DIF}(dc)	DC differential input voltage	0.4		1.75	V	HSTL[d]
V_{CM}(dc)	DC common mode input voltage	0.4		1.0	V	HSTL[e]
VOH	Output High Voltage	V_X + 0.3	V_X + 0.5	1.4	V	HSTL[f,a]
VOL	Output Low Voltage	0.0	V_X - 0.5	V_X - 0.3	V	HSTL[f]
ICCI	Core Supply Current			140	mA	
ICCA	PLL Supply Current		15	20	mA	
ICCO	Output Supply Current		150		mA	Note [g]
$Theta_{JA}$	Junction to ambient thermal resistance		53		°C/W	Note [h]

a) DC levels will vary 1:1 with VCC.
b) VPP minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum VPP of 200mV.
c) V_{IN} (dc) specifies the maximum allowable dc excursion of each differential input.
d) V_{DIF} (dc) specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching, where V_{TR} is the "true" input signal and V_{CP} is the "complement" input signal.
e) V_{CM}(dc) specifies the maximum allowable range of input signal crosspoint voltage
f) V_X is the differential output crosspoint voltage defined in the "AC CHARACTERISTICS" section
g) 2 PCLK into 25Ω and 1 EXTFB into 50Ω
h) Measured with 1.3M/s (250fpm) airflow

AC CHARACTERISTICS (V_{CCA} = V_{CCI} = 3.3V ± 5%, V_{CCO} = 1.7 to 2.1V, T_A = 0 to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
fref	Input Frequency		100 - 125		MHz	
fMAX	Maximum Output Frequency	340		640	MHz	Note [b]
tsk(o)	Skew Error (PCLK)			35	ps	Note [c]
$t_{jit(0)}$	Phase jitter (IO jitter)			output period / 2		Note [c]
$t_{jit(cc)}$	Cycle–to–cycle jitter (full period)			5%		Note [c, e]
$t_{jit(1/2per)}$	Cycle–to–cycle jitter (half period)			6%	Note[d]	Note [c, d]
V_{DIFout}	Differential Output pk–pk swing	0.6			V	For all HSTL output pairs
Vx	Differential output crosspoint voltage	0.68		0.9	V	For all HSTL output pairs
t_{lock}	Maximum PLL lock time			10	ms	

a) All PCLK outputs are terminated in 25Ω to ground, EXTFB_OUT is terminated in 50Ω to ground (applies to all measurements).
b) With PLL active but in bypass mode, fref Max is limited by input buffer; best performance is expected with PECL input.
c) Measured at differential pair crossover.
d) Reference to half PCLK period.
e) Reference to full PCLK period.

4

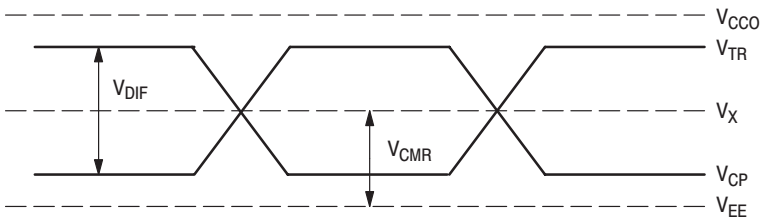

Figure 3. HSTL Differential Input Levels

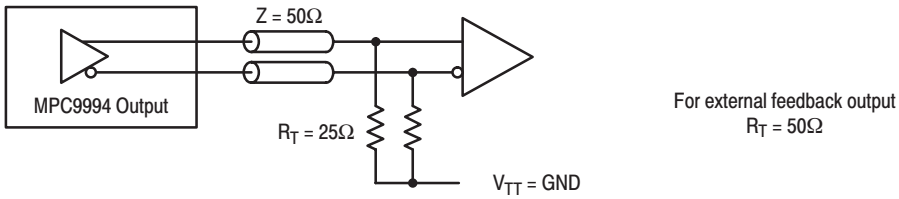

Figure 4. Output Termination and AC Test Reference

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC9994 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9994 provides separate power supplies for the output buffers (V_{CCO}) and the phase-locked loop (V_{CCA}) of the device.

The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC9994. Figure 5illustrates a typical power supply filter scheme. The MPC9994 is most susceptible to noise with spectral content in the 10kHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC9994. From the data sheet the I_{VCCA} current (the current sourced through the V_{CCA} pin) is typically 15 mA (20 mA maximum), assuming that a minimum of 3.3V–5% must be maintained on the V_{CCA} pin. Very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 5 “Power Supply Filter” must have a resistance of 5-15Ω to meet the voltage drop criteria.. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8-10 Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

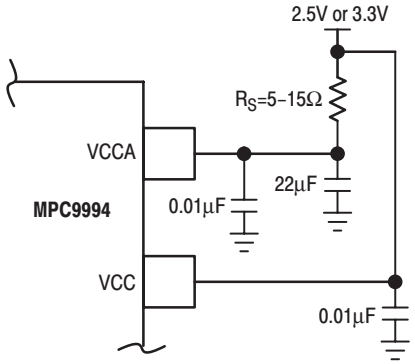

Figure 5. Power Supply Filter

Although the MPC9994 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.