Sound fader control circuit TEA6320

FEATURES

- Source selector for four stereo and one mono inputs
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass and treble control
- Mute control at audio signal zero crossing
- Fast mute control via I²C-bus
- Fast mute control via pin
- I²C-bus control for all functions
- Power supply with internal power-on reset.

GENERAL DESCRIPTION

The sound fader control circuit TEA6320 is an I²C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	26	–	mA
$V_{o(rms)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	voltage gain		−86	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
G_{bass}	bass control		−15	–	+15	dB
G_{treble}	treble control		−12	–	+12	dB
$G_{step(treble)}$	step resolution (bass, treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_O = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(rms)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	76	–	dB
α_{cs}	channel separation	250 Hz ≤ f ≤ 10 kHz; G_v = 0 dB	90	96	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6320	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
TEA6320T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

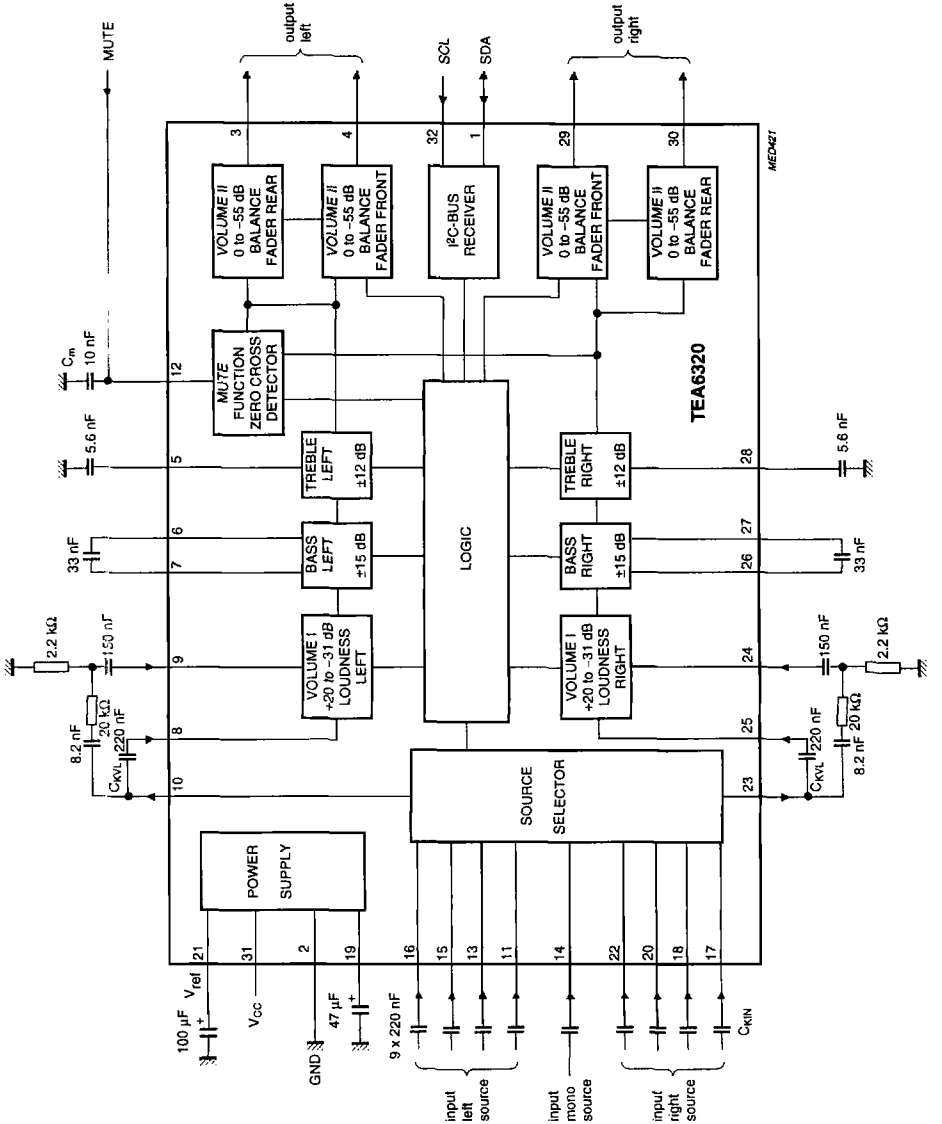


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
GND	2	ground
OUTLR	3	output left rear
OUTLF	4	output left front
TL	5	treble control capacitor left channel or input from an external equalizer
B2L	6	bass control capacitor left channel or output to an external equalizer
B1L	7	bass control capacitor, left channel
IVL	8	input volume I, left control part
ILL	9	input loudness, left control part
QSL	10	output source selector, left channel
IDL	11	input D left source
MUTE	12	mute control
ICL	13	input C left source
IMO	14	input mono source
IBL	15	input B left source
IAL	16	input A left source
IAR	17	input A right source
IBR	18	input B right source
CAP	19	electronic filtering for supply
ICR	20	input C right source
V_{ref}	21	reference voltage ($0.5V_{CC}$)
IDR	22	input D right source
QSR	23	output source selector right channel
ILR	24	input loudness right channel
IVR	25	input volume I, right control part
B1R	26	bass control capacitor right channel
B2R	27	bass control capacitor right channel or output to an external equalizer
TR	28	treble control capacitor right channel or input from an external equalizer
OUTRF	29	output right front
OUTRR	30	output right rear
V_{CC}	31	supply voltage
SCL	32	serial clock input

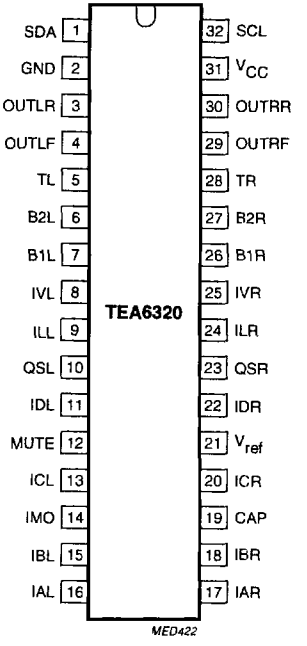


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The source selector selects one of 4 stereo inputs or the mono input. The maximum input signal voltage is $V_{i(rms)}$ = 2 V. The outputs of the source selector and the inputs of the following volume control parts are available at pins 8 and 10 for the left channel and pins 23 and 25 for the right channel. This offers the possibility of interfacing a noise reduction system.

The volume control function is split into two sections: volume I control block and volume II control block.

The control range of volume I is between +20 dB and −31 dB in steps of 1 dB. The volume II control range is between 0 dB and −55 dB in steps of 1 dB. Although the theoretical possible control range is 106 dB (+20 to −86 dB), in practice a range of 86 dB (+20 to −66 dB) is recommended. The gain/attenuation setting of the volume I control block is common for both channels.

The volume I control block operates in combination with the loudness control. The filter is linear when the maximum gain for the volume I control (+20 dB) is selected. The filter characteristic increases automatically over a range of 32 dB down to a setting of −12 dB. That means the maximum filter characteristic is obtained at −12 dB setting of volume I. Further reduction of the volume does not further influence the filter characteristic (see Fig.5). The maximum selected filter characteristic is determined by external components. The proposed application gives a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched on or off via I²C-bus control (see Table 7).

The volume I control block is followed by the bass control block. A single external capacitor of 33 nF for each channel in combination with internal resistors, provides the frequency response of the bass control (see Fig.3). The adjustable range is between −15 and +15 dB at 40 Hz.

Both loudness and bass control result in a maximum bass boost of 32 dB for low volume settings.

The treble control block offers a control range between −12 and +12 dB in steps of 1.5 dB at 15 kHz. The filter characteristic is determined by a single capacitor of 5.6 nF for each channel in combination with internal resistors (see Fig.4).

The basic step width of bass and treble control is 3 dB. The intermediate steps are obtained by switching 1.5 dB boost and 1.5 dB attenuation steps.

The bass and treble control functions can be switched off via I²C-bus. In this event the internal signal flow is disconnected. The connections B2L and B2R are outputs and TL and TR are inputs for inserting an external equalizer.

The last section of the circuit is the volume II block. The balance and fader functions are performed using the same control blocks. This is realized by 4 independently controllable attenuators, one for each output. The control range of these attenuators is 55 dB in steps of 1 dB with an additional mute step.

The circuit provides 3 mute modes:

1. Zero crossing mode mute via I²C-bus using 2 independent zero crossing detectors (ZCM, see Tables 2 and 9 and Fig.16).
2. Fast mute via MUTE pin (see Fig.10).
3. Fast mute via I²C-bus either by general mute (GMU, see Tables 2 and 9) or volume II block setting (see Table 4).

The mute function is performed immediately if ZCM is cleared (ZCM = 0). If the bit is set (ZCM = 1) the mute is activated after changing the GMU bit. The actual mute switching is delayed until the next zero crossing of the audio frequency signal. As the two audio channels (left and right) are independent, two comparators are built-in to control independent mute switches.

To avoid a large delay of mute switching when very low frequencies are processed, the maximum delay time is limited to typically 100 ms by an integrated timing circuit and an external capacitor (C_m = 10 nF, see Fig.10). This timing circuit is triggered by reception of a new data word for the switch function which includes the GMU bit. After a discharge and charge period of an external capacitor the muting switch follows the GMU bit if no zero crossing was detected during that time.

The mute function can also be controlled externally. If the mute pin is switched to ground all outputs are muted immediately (hardware mute). This mute request overwrites all mute controls via the I²C-bus for the time the pin is held LOW. The hardware mute position is not stored in the TEA6320.

For the turn on/off behaviour the following explanation is generally valid. To avoid AF output caused by the input signal coming from preceding stages, which produces output during drop of V_{CC}, the mute has to be set, before the V_{CC} will drop. This can be achieved by I²C-bus control or by grounding the MUTE pin.

For use where is no mute in the application before turn off, a supply voltage drop of more than 1 × V_{BE} will result in a mute during the voltage drop.

The power supply should include a V_{CC} buffer capacitor, which provides a discharging time constant. If the input signal does not disappear after turn off the input will become audible after certain time. A 4.7 kΩ resistor discharges the V_{CC} buffer capacitor, because the internal current of the IC does not discharge it completely.

The hardware mute function is favourable for use in Radio Data System (RDS) applications. The zero crossing mute avoids modulation plops. This feature is an advantage for mute during changing presets and/or sources (e.g. traffic announcement during cassette playback).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	10	V
V_n	voltage at all pins except pin 2 referenced to GND (pin 2)		0	V_{CC}	V
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C
V_{es}	electrostatic handling	note 1			

Note

1. Human body model: C = 100 pF; R = 1.5 kΩ; V ≥ 2 kV. Charge device model: C = 200 pF; R = 0 Ω; V ≥ 500 V.

CHARACTERISTICS

V_{CC} = 8.5 V; R_S = 600 Ω; R_L = 10 kΩ; C_L = 2.5 nF; AC coupled; f = 1 kHz; T_{amb} = 25 °C; gain control G_v = 0 dB; bass linear; treble linear; fader off; balance in mid position; loudness off; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current		–	26	33	mA
V_{DC}	internal DC voltage at inputs and outputs		3.83	4.25	4.68	V
V_{ref}	internal reference voltage at pin 21		–	4.25	–	V
$G_{v(max)}$	maximum voltage gain	R_S = 0 Ω; R_L = ∞	19	20	21	dB
$V_{o(rms)}$	output voltage level for					
	P_{max} at the power output stage	THD ≤ 0.5%; see Fig.11	–	2000	–	mV
	start of clipping	THD = 1%	2300	–	–	mV
		R_L = 2 kΩ; C_L = 10 nF; THD = 1%	2000	–	–	mV
$V_{i(rms)}$	input sensitivity	V_o = 2000 mV; G_v = 20 dB	–	200	–	mV
f_{ro}	roll-off frequency	C_{KIN} = 220 nF; C_{KVL} = 220 nF; $Z_i = Z_{i(min)}$				
		low frequency (–1 dB)	60	–	–	Hz
		low frequency (–3 dB)	30	–	–	Hz
		high frequency (–1 dB)	20000	–	–	Hz
		C_{KIN} = 470 nF; C_{KVL} = 100 nF; $Z_i = Z_{i(typ)}$ low frequency (–3 dB)	17	–	–	Hz
α_{cs}	channel separation	V_i = 2 V; frequency range 250 Hz to 10 kHz	90	96	–	dB
THD	total harmonic distortion	frequency range 20 Hz to 12.5 kHz				
		V_i = 100 mV; G_v = 20 dB	–	0.1	–	%
		V_i = 1 V; G_v = 0 dB	–	0.05	0.15	%
		V_i = 2 V; G_v = 0 dB	–	0.1	–	%
		V_i = 2 V; G_v = –10 dB	–	0.1	–	%
RR	ripple rejection	$V_{r(rms)}$ < 200 mV				
		f = 100 Hz	70	76	–	dB
		f = 40 Hz to 12.5 kHz	–	66	–	dB
(S+N)/N	signal-plus-noise to noise ratio	unweighted; 20 Hz to 20 kHz (RMS); V_o = 2.0 V; see Figs 6 and 7	–	105	–	dB
		CCIR468-2 weighted; quasi peak; V_o = 2.0 V				
		G_v = 0 dB	–	95	–	dB
		G_v = 12 dB	–	88	–	dB
		G_v = 20 dB	–	81	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$P_{no(rms)}$	noise output power (RMS value) only contribution of TEA6320; power amplifier for 6 W	mute position; note 1	–	–	10	nW
α_{ct}	crosstalk $\left(20 \log \frac{V_{bus(\rho-p)}}{V_{o(rms)}}\right)$ between bus inputs and signal outputs	note 2	–	110	–	dB
Source selector						
Z_i	input impedance		25	35	45	kΩ
α_S	input isolation of one selected source to any other input	f = 1 kHz	–	105	–	dB
		f = 12.5 kHz	–	95	–	dB
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.5%; V_{CC} = 8.5 V	–	2.15	–	V
		THD < 0.5%; V_{CC} = 7.5 V	–	1.8	–	V
V_{offset}	DC offset voltage at source selector output by selection of any inputs		–	–	10	mV
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		10	–	–	kΩ
C_L	output load capacity		0	–	2500	pF
G_v	voltage gain, source selector		–	0	–	dB
Control part (source selector disconnected; source resistance 600 Ω)						
Z_i	input impedance volume input		100	150	200	kΩ
	input impedance loudness input		25	33	40	kΩ
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		2	–	–	kΩ
C_L	output load capacity		0	–	10	nF
R_{DCL}	DC load resistance at output to ground		4.7	–	–	kΩ
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.5%	–	2.15	–	V
V_{no}	noise output voltage	CCIR468-2 weighted; quasi peak				
		G_v = 20 dB	–	110	220	μV
		G_v = 0 dB	–	33	50	μV
		G_v = −66 dB	–	13	22	μV
		mute position	–	10	–	μV
CR_{tot}	total continuous control range		–	106	–	dB
	recommended control range		–	86	–	dB
G_{step}	step resolution		–	1	–	dB
	step error between any adjoining step		–	–	0.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_a	attenuator set error	G_v = +20 to −50 dB	–	–	2	dB
		G_v = −51 to −66 dB	–	–	3	dB
ΔG_t	gain tracking error	G_v = +20 to −50 dB	–	–	2	dB
$MUTE_{att}$	mute attenuation	see Fig.10	100	110	–	dB
V_{offset}	DC step offset between any adjoining step	G_v = 0 to −66 dB	–	0.2	10	mV
		G_v = 20 to 0 dB	–	2	15	mV
	DC step offset between any step to mute	G_v = 0 to −66 dB	–	–	10	mV
Volume I control and loudness						
CR_{vol}	continuous volume control range		–	51	–	dB
G_v	voltage gain		−31	–	+20	dB
G_{step}	step resolution		–	1	–	dB
L_{Bmax}	maximum loudness boost	loudness on; referred to loudness off; boost is determined by external components				
		f = 40 Hz	–	17	–	dB
		f = 10 kHz	–	4.5	–	dB
Bass control						
G_{bass}	bass control, maximum boost	f = 40 Hz	14	15	16	dB
	maximum attenuation	f = 40 Hz	14	15	16	dB
G_{step}	step resolution (toggle switching)	f = 40 Hz	–	1.5	–	dB
	step error between any adjoining step	f = 40 Hz	–	–	0.5	dB
V_{offset}	DC step offset in any bass position		–	–	20	mV
Treble control						
G_{treble}	treble control, maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	–	–	15	dB
G_{step}	step resolution (toggle switching)	f = 15 kHz	–	1.5	–	dB
	step error between any adjoining step	f = 15 kHz	–	–	0.5	dB
V_{offset}	DC step offset in any treble position		–	–	10	mV
Volume II, balance and fader control						
CR	continuous attenuation fader and volume control range		53.5	55	56.5	dB
G_{step}	step resolution		–	1	2	dB
	attenuation set error		–	–	1.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mute function (see Fig.10)						
HARDWARE MUTE						
V_{sw}	mute switch level ($2 \times V_{BE}$)		–	1.45	–	V
mute active						
V_{swLOW}	input level		–	–	1.0	V
I_i	input current	V_{swLOW} = 1 V	–300	–	–	µA
mute passive: level internally defined						
V_{swHIGH}	saturation voltage		–	–	V_{CC}	V
$t_{d(mute)}$	delay until mute passive		–	–	0.5	ms
ZERO CROSSING MUTE						
I_d	discharge current		0.3	0.6	1.2	µA
I_{ch}	charge current		–300	–150	–	µA
V_{swDEL}	delay switch level ($3 \times V_{BE}$)		–	2.2	–	V
t_d	delay time	C_m = 10 nF	–	100	–	ms
V_{wind}	window for audio signal zero crossing detection		–	30	40	mV
Muting at power supply drop						
V_{CCdrop}	supply drop for mute active		–	V_{19} – 0.7	–	V
Power-on reset (when reset is active the GMU-bit (general mute) is set and the I²C-bus receiver is in reset position)						
V_{CC}	increasing supply voltage start of reset		–	–	2.5	V
	end of reset		5.2	6.5	7.2	V
	decreasing supply voltage start of reset		4.2	5.5	6.2	V
Digital part (I²C-bus pins); note 3						
V_{iH}	HIGH level input voltage		3	–	9.5	V
V_{iL}	LOW level input voltage		–0.3	–	+1.5	V
I_{iH}	HIGH level input current		–10	–	+10	µA
I_{iL}	LOW level input current		–10	–	+10	µA
V_{oL}	LOW level output voltage	I_L = 3 mA	–	–	0.4	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier at 4 Ω with 20 dB gain and a fixed attenuator of 12 dB in front of it. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. The transmission contains: total initialization with MAD and subaddress for volume and 8 data words, see also definition of characteristics, clock frequency = 50 kHz, repetition burst rate = 400 Hz, maximum bus signal amplitude = 5 V (p-p).
3. The AC characteristics are in accordance with the I²C-bus specification. This specification, *"The I²C-bus and how to use it"*, can be ordered using the code 9398 393 40011.

I²C-BUS PROTOCOL

I²C-bus format

S[1]	SLAVE ADDRESS[2]	A[3]	SUBADDRESS[4]	A[3]	DATA[5]	A[3]	P[6]

Notes

1. S = START condition.
2. SLAVE ADDRESS (MAD) = 1000 0000.
3. A = acknowledge, generated by the slave.
4. SUBADDRESS (SAD), see Table 1.
5. DATA, see Table 1; if more than 1 byte of DATA is transmitted, then auto-increment of the significant subaddress is performed.
6. P = STOP condition.

Table 1 Second byte after MAD

FUNCTION	BIT	MSB							LSB
		7	6	5	4	3	2[1]	1[1]	0[1]
Volume/loudness	V	0	0	0	0	0	0	0	0
Fader front right	FFR	0	0	0	0	0	0	0	1
Fader front left	FFL	0	0	0	0	0	0	1	0
Fader rear right	FRR	0	0	0	0	0	0	1	1
Fader rear left	FRL	0	0	0	0	0	1	0	0
Bass	BA	0	0	0	0	0	1	0	1
Treble	TR	0	0	0	0	0	1	1	0
Switch	S	0	0	0	0	0	1	1	1

Note

1. Significant subaddress.

Table 2 Definition of third byte after MAD and SAD

FUNCTION	BIT	MSB							LSB
		7	6	5	4	3	2	1	0
Volume/loudness	V	ZCM[1]	LOFF[2]	V5[3]	V4[3]	V3[3]	V2[3]	V1[3]	V0[3]
Fader front right	FFR	X[4]	X[4]	FFR5[5]	FFR4[5]	FFR3[5]	FFR2[5]	FFR1[5]	FFR0[5]
Fader front left	FFL	X[4]	X[4]	FFL5[6]	FFL4[6]	FFL3[6]	FFL2[6]	FFL1[6]	FFL0[6]
Fader rear right	FRR	X[4]	X[4]	FRR5[7]	FRR4[7]	FRR3[7]	FRR2[7]	FRR1[7]	FRR0[7]
Fader rear left	FRL	X[4]	X[4]	FRL5[8]	FRL4[8]	FRL3[8]	FRL2[8]	FRL1[8]	FRL0[8]
Bass	BA	X[4]	X[4]	X[4]	BA4[9]	BA3[9]	BA2[9]	BA1[9]	BA0[9]
Treble	TR	X[4]	X[4]	X[4]	TR4[10]	TR3[10]	TR2[10]	TR1[10]	TR0[10]
Switch	S	GMU[11]	X[4]	X[4]	X[4]	X[4]	SC2[12]	SC1[12]	SC0[12]

Notes

1. Zero crossing mode.
2. Switch loudness on/off.
3. Volume control.
4. Don't care bits (logic 1 during testing).
5. Fader control front right.
6. Fader control front left.
7. Fader control rear right.
8. Fader control rear left.
9. Bass control.
10. Treble control.
11. Mute control for all outputs (general mute).
12. Source selector control.

Table 3 Volume I setting

G_v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
Loudness on: the increment of the loudness characteristics is linear at every volume step in the range from +20 to −11 dB						
+20	1	1	1	1	1	1
+19	1	1	1	1	1	0
+18	1	1	1	1	0	1
+17	1	1	1	1	0	0
+16	1	1	1	0	1	1
+15	1	1	1	0	1	0
+14	1	1	1	0	0	1
+13	1	1	1	0	0	0
+12	1	1	0	1	1	1
+11	1	1	0	1	1	0
+10	1	1	0	1	0	1
+9	1	1	0	1	0	0
+8	1	1	0	0	1	1
+7	1	1	0	0	1	0
+6	1	1	0	0	0	1
+5	1	1	0	0	0	0
+4	1	0	1	1	1	1
+3	1	0	1	1	1	0
+2	1	0	1	1	0	1
+1	1	0	1	1	0	0
0	1	0	1	0	1	1
−1	1	0	1	0	1	0
−2	1	0	1	0	0	1
−3	1	0	1	0	0	0
−4	1	0	0	1	1	1
−5	1	0	0	1	1	0
−6	1	0	0	1	0	1
−7	1	0	0	1	0	0
−8	1	0	0	0	1	1
−9	1	0	0	0	1	0
−10	1	0	0	0	0	1
−11	1	0	0	0	0	0

G_v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
Loudness characteristic is constant in a range from –11 dB to –31 dB						
–12	0	1	1	1	1	1
–13	0	1	1	1	1	0
–14	0	1	1	1	0	1
–15	0	1	1	1	0	0
–16	0	1	1	0	1	1
–17	0	1	1	0	1	0
–18	0	1	1	0	0	1
–19	0	1	1	0	0	0
–20	0	1	0	1	1	1
–21	0	1	0	1	1	0
–22	0	1	0	1	0	1
–23	0	1	0	1	0	0
–24	0	1	0	0	1	1
–25	0	1	0	0	1	0
–26	0	1	0	0	0	1
–27	0	1	0	0	0	0
–28	0	0	1	1	1	1
–29	0	0	1	1	1	0
–30	0	0	1	1	0	1
–31	0	0	1	1	0	0
Repetition of steps in a range from –28 dB to –31 dB						
–28	0	0	1	0	1	1
–29	0	0	1	0	1	0
–30	0	0	1	0	0	1
–31	0	0	1	0	0	0
–28	0	0	0	1	1	1
–29	0	0	0	1	1	0
–30	0	0	0	1	0	1
–31	0	0	0	1	0	0
–28	0	0	0	0	1	1
–29	0	0	0	0	1	0
–30	0	0	0	0	0	1
–31	0	0	0	0	0	0

Table 4 Volume II setting (fader and balance); note 1

G_v (dB)	DATA					
	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
0	1	1	1	1	1	1
−1	1	1	1	1	1	0
−2	1	1	1	1	0	1
−3	1	1	1	1	0	0
−4	1	1	1	0	1	1
−5	1	1	1	0	1	0
−6	1	1	1	0	0	1
−7	1	1	1	0	0	0
−8	1	1	0	1	1	1
−9	1	1	0	1	1	0
−10	1	1	0	1	0	1
−11	1	1	0	1	0	0
−12	1	1	0	0	1	1
−13	1	1	0	0	1	0
−14	1	1	0	0	0	1
−15	1	1	0	0	0	0
−16	1	0	1	1	1	1
−17	1	0	1	1	1	0
−18	1	0	1	1	0	1
−19	1	0	1	1	0	0
−20	1	0	1	0	1	1
−21	1	0	1	0	1	0
−22	1	0	1	0	0	1
−23	1	0	1	0	0	0
−24	1	0	0	1	1	1
−25	1	0	0	1	1	0
−26	1	0	0	1	0	1
−27	1	0	0	1	0	0
−28	1	0	0	0	1	1
−29	1	0	0	0	1	0
−30	1	0	0	0	0	1
−31	1	0	0	0	0	0
−32	0	1	1	1	1	1
−33	0	1	1	1	1	0
−34	0	1	1	1	0	1

G_v (dB)	DATA					
	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
−35	0	1	1	1	0	0
−36	0	1	1	0	1	1
−37	0	1	1	0	1	0
−38	0	1	1	0	0	1
−39	0	1	1	0	0	0
−40	0	1	0	1	1	1
−41	0	1	0	1	1	0
−42	0	1	0	1	0	1
−43	0	1	0	1	0	0
−44	0	1	0	0	1	1
−45	0	1	0	0	1	0
−46	0	1	0	0	0	1
−47	0	1	0	0	0	0
−48	0	0	1	1	1	1
−49	0	0	1	1	1	0
−50	0	0	1	1	0	1
−51	0	0	1	1	0	0
−52	0	0	1	0	1	1
−53	0	0	1	0	1	0
−54	0	0	1	0	0	1
−55	0	0	1	0	0	0
mute	0	0	0	1	1	1
mute	0	0	0	1	1	0
mute	0	0	0	1	0	1
mute	0	0	0	1	0	0
mute	0	0	0	0	1	1
mute	0	0	0	0	1	0
mute	0	0	0	0	0	1
mute	0	0	0	0	0	0

Note

1. For a particular range the data is always the same, only the subaddress changes.

Table 5 Bass setting

G_{bass} (dB)	DATA				
	BA4	BA3	BA2	BA1	BA0
+15.0	1	1	1	1	1
+13.5	1	1	1	1	0
+15.0	1	1	1	0	1
+13.5	1	1	1	0	0
+15.0	1	1	0	1	1
+13.5	1	1	0	1	0
+12.0	1	1	0	0	1
+10.5	1	1	0	0	0
+9.0	1	0	1	1	1
+7.5	1	0	1	1	0
+6.0	1	0	1	0	1
+4.5	1	0	1	0	0
+3.0	1	0	0	1	1
+1.5	1	0	0	1	0
0[1]	1	0	0	0	1
0[2]	1	0	0	0	0
−1.5	0	1	1	1	1
−3.0	0	1	1	1	0
−4.5	0	1	1	0	1
−6.0	0	1	1	0	0
−7.5	0	1	0	1	1
−9.0	0	1	0	1	0
−10.5	0	1	0	0	1
−12.0	0	1	0	0	0
−13.5	0	0	1	1	1
−15.0	0	0	1	1	0
−13.5	0	0	1	0	1
−15.0	0	0	1	0	0
note 3	0	0	0	1	1
note 3	0	0	0	1	0
note 3	0	0	0	0	1
notes 3 and 4	0	0	0	0	0

Notes

1. Recommended data word for step 0 dB.
2. Result of 1.5 dB boost and 1.5 dB attenuation.
3. The last four bass control data words mute the bass response.
4. The last bass control and treble control data words (00000) enable the external equalizer connection.

Table 6 Treble setting

G_{treble} (dB)	DATA				
	TR4	TR3	TR2	TR1	TR0
+12.0	1	1	1	1	1
+10.5	1	1	1	1	0
+12.0	1	1	1	0	1
+10.5	1	1	1	0	0
+12.0	1	1	0	1	1
+10.5	1	1	0	1	0
+12.0	1	1	0	0	1
+10.5	1	1	0	0	0
+9.0	1	0	1	1	1
+7.5	1	0	1	1	0
+6.0	1	0	1	0	1
+4.5	1	0	1	0	0
+3.0	1	0	0	1	1
+1.5	1	0	0	1	0
0(1)	1	0	0	0	1
0(2)	1	0	0	0	0
−1.5	0	1	1	1	1
−3.0	0	1	1	1	0
−4.5	0	1	1	0	1
−6.0	0	1	1	0	0
−7.5	0	1	0	1	1
−9.0	0	1	0	1	0
−10.5	0	1	0	0	1
−12.0	0	1	0	0	0
note 3	0	0	1	1	1
note 3	0	0	1	1	0
note 3	0	0	1	0	1
note 3	0	0	1	0	0
note 3	0	0	0	1	1
note 3	0	0	0	1	0
note 3	0	0	0	0	1
notes 3 and 4	0	0	0	0	0

Notes

1. Recommended data word for step 0 dB.
2. Result of 1.5 dB boost and 1.5 dB attenuation.
3. The last eight treble control data words select treble output.
4. The last treble control and bass control data words (00000) enable the external equalizer connection.

Table 7 Loudness setting

CHARACTERISTIC	DATA LOFF
With loudness	0
Linear	1

Table 8 Selected input

FUNCTION	DATA		
	SC2	SC1	SC0
Stereo inputs IAL and IAR	1	1	1
Stereo inputs IBL and IBR	1	1	0
Stereo inputs ICL and ICR	1	0	1
Stereo inputs IDL and IDR	1	0	0
Mono input IMO	0	X(1)	X(1)

Note

1. X = don't care bits (logic 1 during testing).

Table 9 Mute mode

FUNCTION	DATA	
	GMU	ZCM
Direct mute off	0	0
Mute off delayed until the next zero crossing	0	1
Direct mute	1	0
Mute delayed until the next zero crossing	1	1

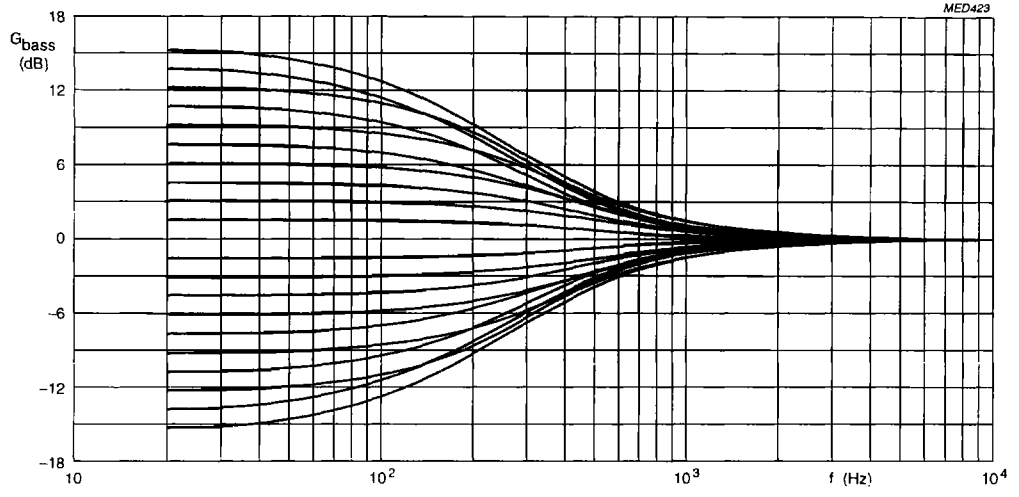


Fig.3 Bass control.

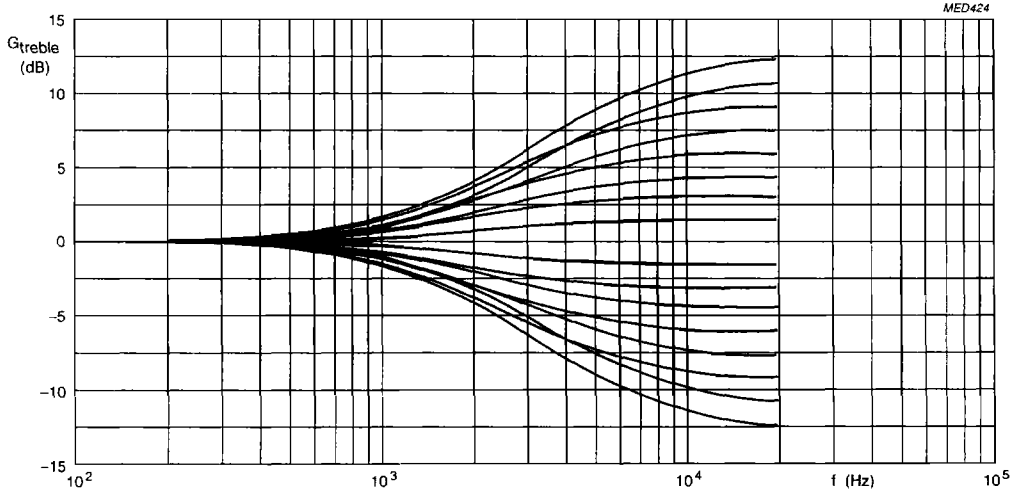


Fig.4 Treble control.

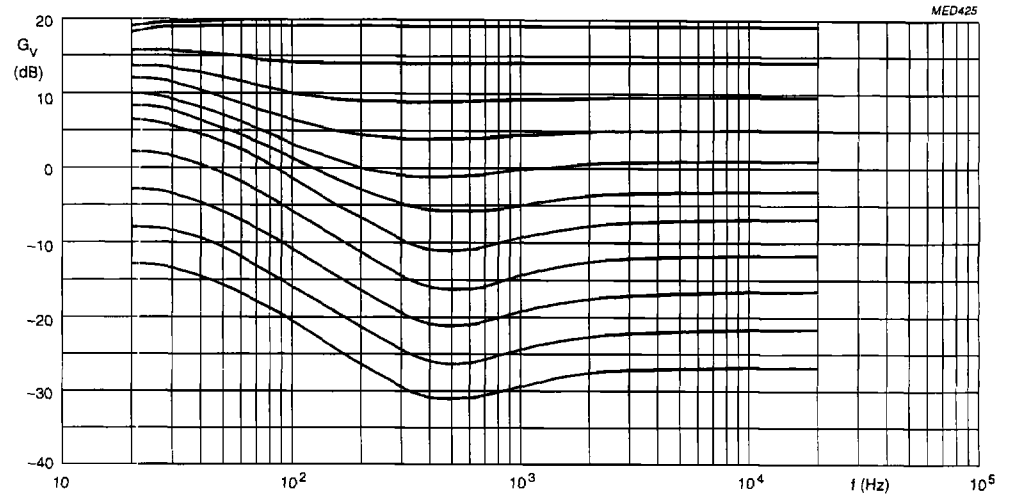
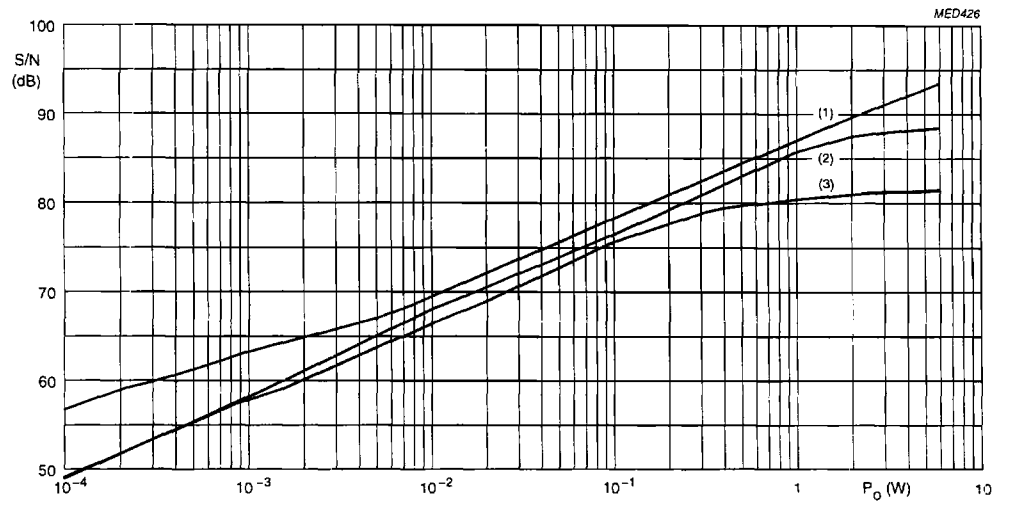
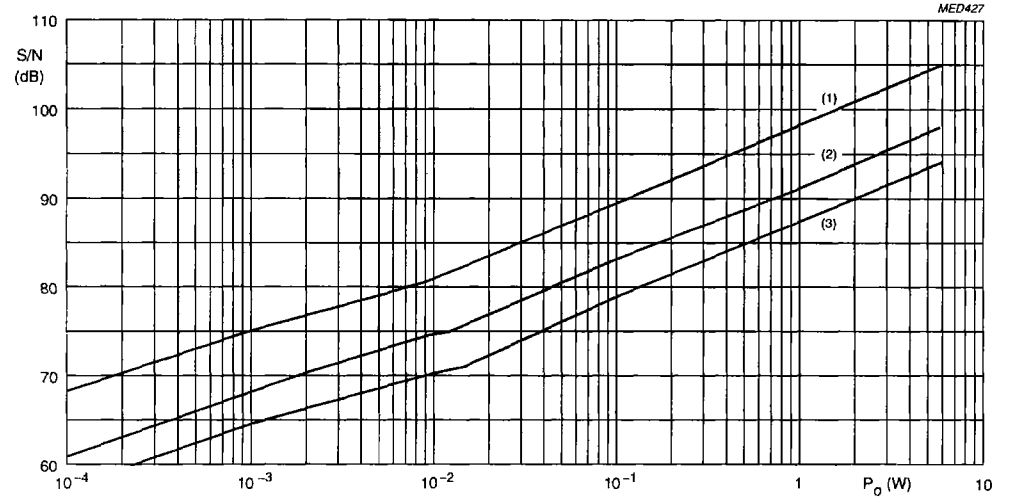


Fig.5 Volume control with loudness (including low roll-off frequency).



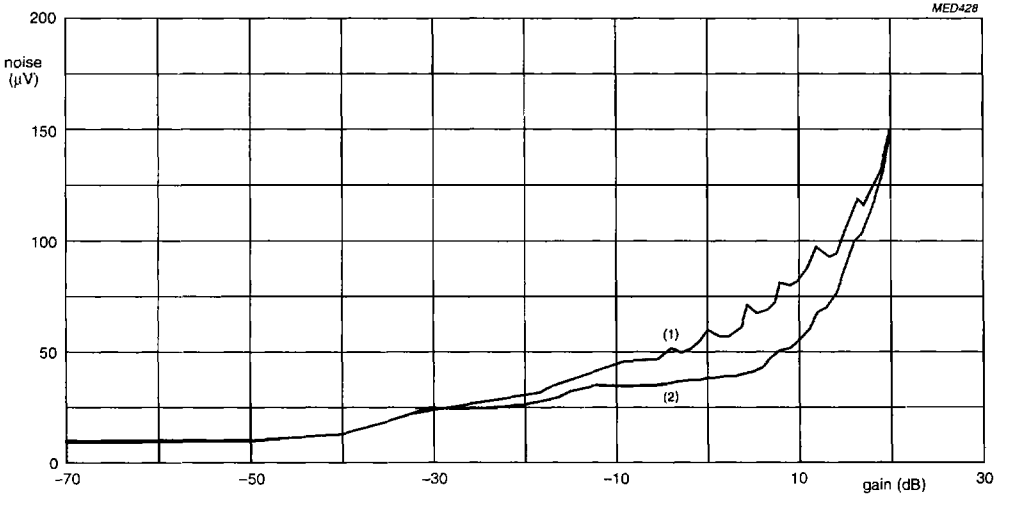
(1) V_i = 2.0 V.
(2) V_i = 0.5 V.
(3) V_i = 0.2 V.

Fig.6 Signal-to-noise ratio; noise weighted: CCIR468-2, quasi peak.



(1) Unweighted RMS.
(2) CCIR468-2 RMS.
(3) CCIR468-2 quasi peak.

Fig.7 Signal-to-noise ratio; $V_i = 2$ V; $P_{max} = 6$ W.



Stereo/mono inputs.
(1) Loudness on.
(2) Loudness off.

Fig.8 Noise output voltage; CCIR468-2, quasi peak.

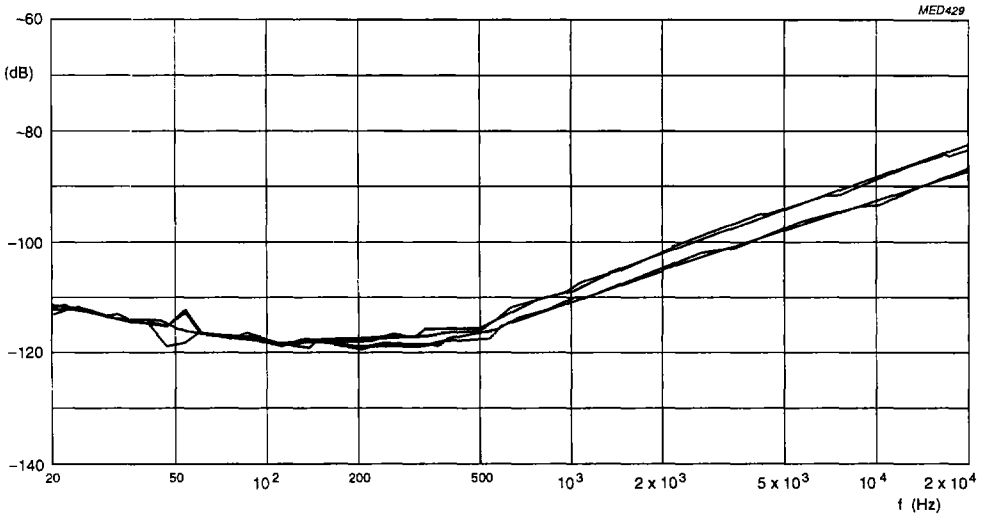
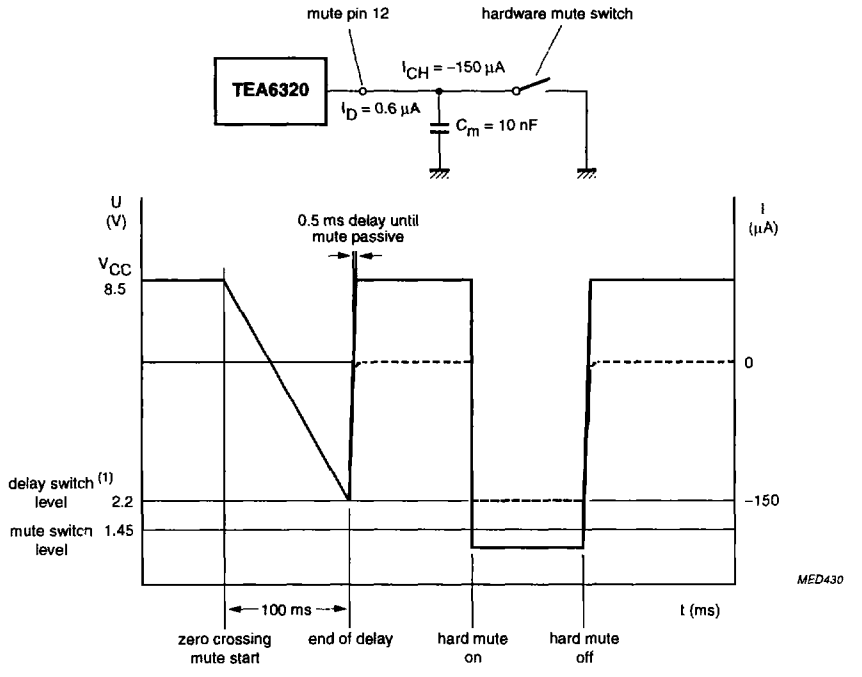

MED429
-60
(dB)
-80
-100
-120
-140
20
50
10 2
200
500
10 3
2 x 10 3
5 x 10 3
10 4
2 x 10 4
f (Hz)

Fig.9 Muting.

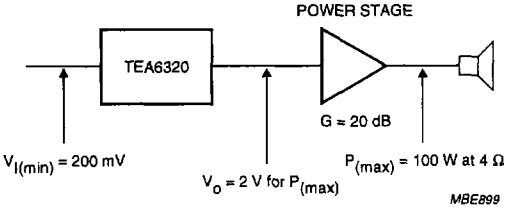


(1) Typically 2.2 V; referenced to $3 \times V_{BE}$.

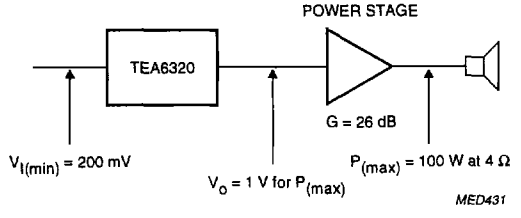
Fig.10 Mute function diagram.

If the 20 dB gain is not required for the maximum volume position, it will be an advantage to use the maximum boost gain and then increased attenuation in the last section, Volume II.

Therefore the loudness will be at the correct place and a lower noise and offset voltage will be achieved.



a.



b.

a. Gain volume I = 20 dB ($G_{v(max)}$); gain volume II = 0 dB; fader and balance range = 55 dB.
b. Gain volume I = 20 dB ($G_{v(max)}$); gain volume II = −6 dB global setting; fader and balance range now 49 dB, previously 55 dB.

Fig.11 Level diagram.

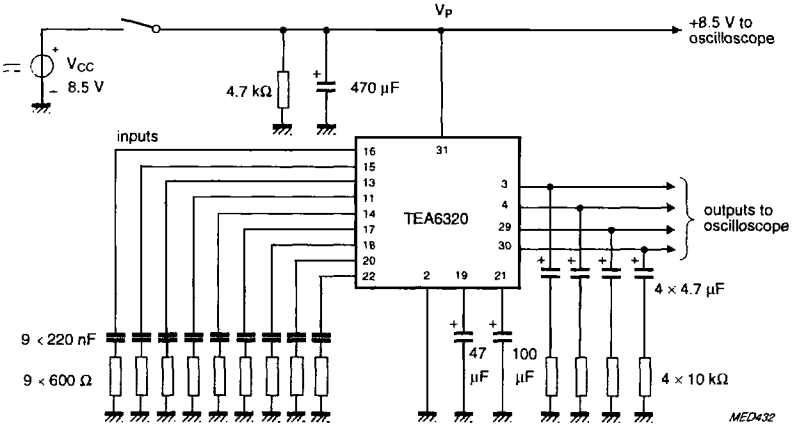
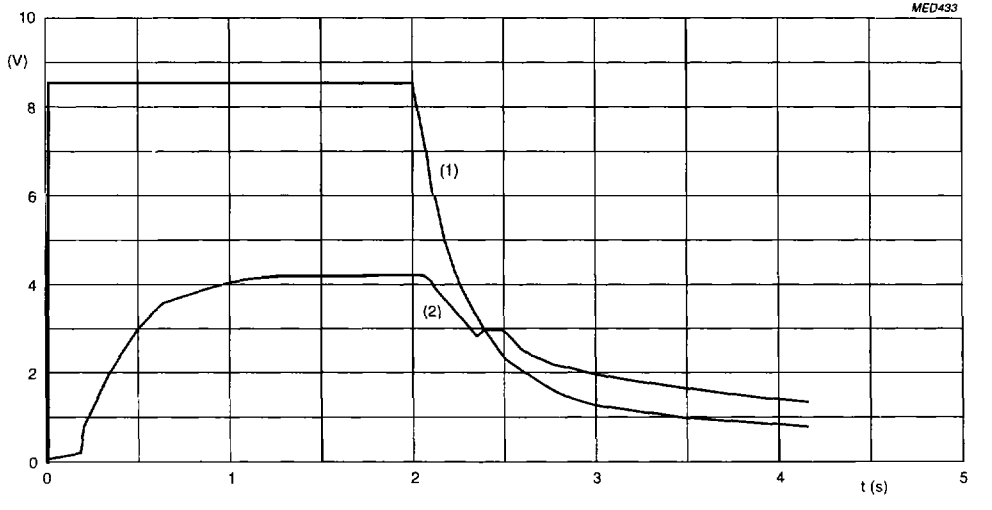


Fig.12 Turn-on/off power supply circuit diagram.



(1) V_{CC}.
(2) V_O.

Fig.13 Turn-on/off behaviour.

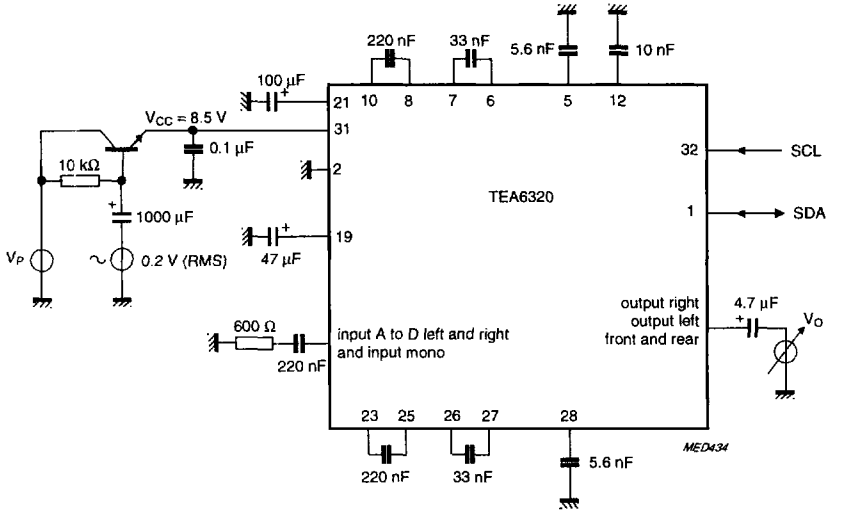


Fig.14 Test circuit for power supply ripple rejection (RR).

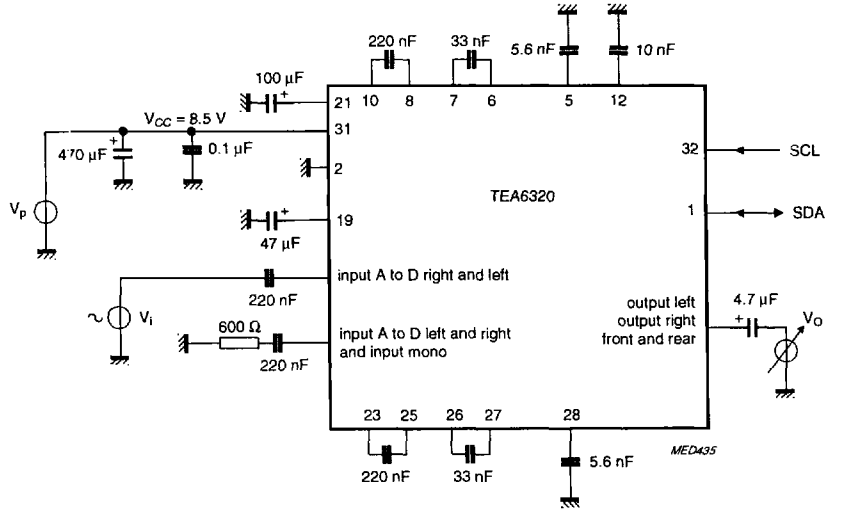


Fig.15 Test circuit for channel separation (α_{cs}).

Selection of input signals by using the zero crossing mute mode

A selection from input A (IAL) to input B (IBL) left sources produces a modulation click depending on the difference of the signal values at the time of switching.

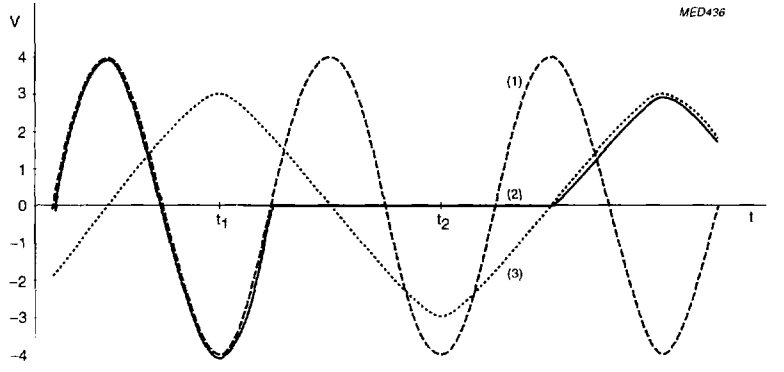
At t_1 the maximum possible difference between signals is 7 V(p-p) (see Fig. 16) and gives a large click. Using the cross detector no modulation click is audible.

For example: The selection is enabled at t_1, the microcontroller sets the zero cross bit (ZCM = 1) and then the mute bit (GMU = 1) via the I²C-bus. The output signal follows the input A signal, until the next zero crossing occurs and then activates mute.

After a fixed delay time at t_2, the microcontroller sends the bits for input switching and mute inactive.

The output signal remains muted until the next signal zero crossing of input B (IBL) occurs, and then follows that signal.

The delay time $t_2 - t_1$ is e.g. 40 ms. Therefore the capacity C_m = 3.3 nF. The zero cross function is working at the lowest frequency of 40 Hz determined by the C_m capacitor.



(1) Input A (IAL).
(2) Output.
(3) Input B (IBL).

Fig.16 Zero cross function; only one channel shown.

Loudness filter calculation example

Figure 17 shows the basic loudness circuit with an external low-pass filter application. R1 allows an attenuation range of 21 dB while the boost is determined by the gain stage V_2. Both result in a loudness control range of +20 to −12 dB.

Defining f_{ref} as the frequency where the level does not change while switching loudness on/off. The external resistor R3 for $f_{ref} \rightarrow \infty$ can be calculated as:

$$R3 = R1\frac{10^{\frac{G_v}{20}}}{1 - 10^{\frac{G_v}{20}}}$$. With G_v = −21 dB and R1 = 33 kΩ,

R3 = 3.2 kΩ is generated.

For the low-pass filter characteristic the value of the external capacitor C1 can be determined by setting a specific boost for a defined frequency and referring the gain to G_v at f_{ref} as indicated above.

$$\left|\frac{1}{j(\omega C1)}\right| = \frac{(R1 + R3) \times 10^{\frac{G_v}{20}} - R3}{1 - 10^{\frac{G_v}{20}}}$$

For example: 3 dB boost at f = 1 kHz
$G_v = G_{v(ref)}$ + 3 dB = −18 dB; f = 1 kHz and C1 = 100 nF.

If a loudness characteristic with additional high frequency boost is desired, an additional high-pass section has to be included in the external filter circuit as indicated in the block diagram. A filter configuration that provides AC coupling avoids offset voltage problems.

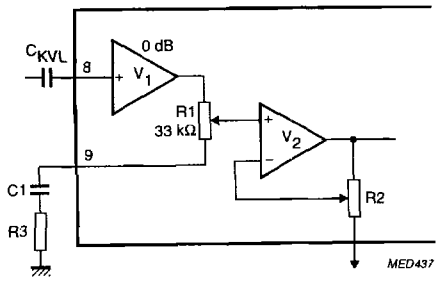


Fig.17 Basic loudness circuit.

INTERNAL PIN CONFIGURATIONS

Values shown in Figs 18 to 30 are typical DC values;
V_{CC} = 8.5 V.

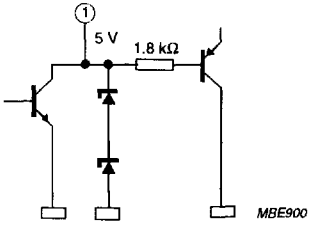


Fig.18 Pin 1: SDA (I²C-bus data).

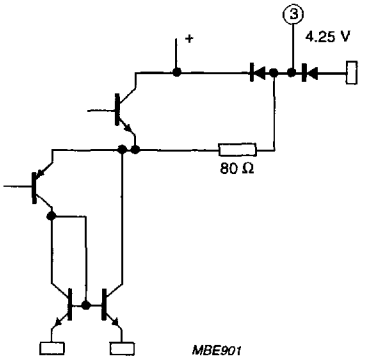


Fig.19 Pins 3, 4, 29, 30: output signals.

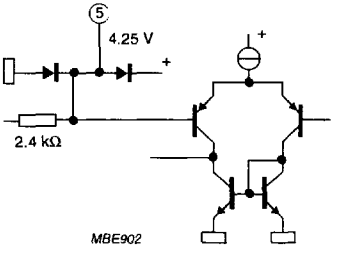


Fig.20 Pins 5 and 28: treble control capacitors.

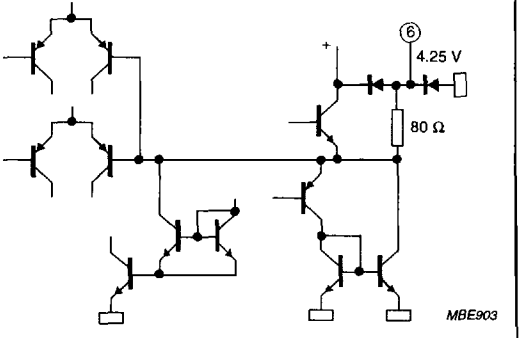


Fig.21 Pins 6 and 27: bass control capacitor outputs.

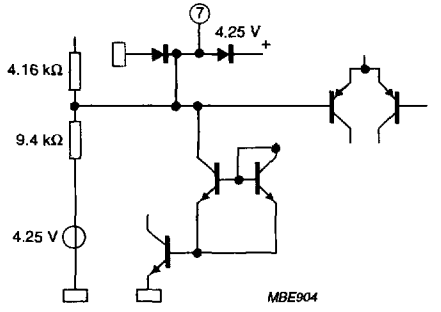


Fig.22 Pins 7 and 26: bass control capacitor inputs.

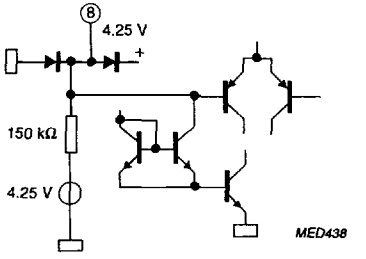


Fig.23 Pins 8 and 25: input volume 1, control part.

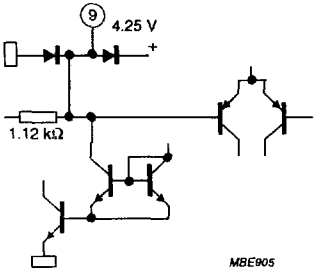


Fig.24 Pins 9 and 24: input loudness, control part.

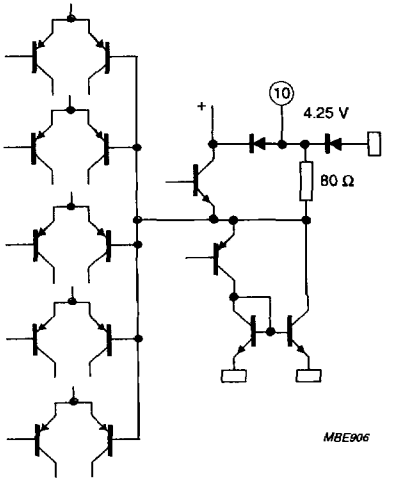


Fig.25 Pins 10 and 23: output source selector.

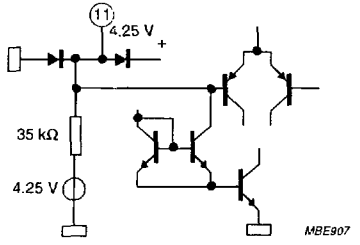


Fig.26 Pins 11, 13 to 18, 20, 22: inputs.

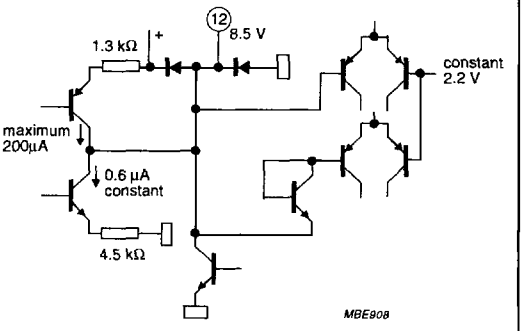


Fig.27 Pin 12: mute control.

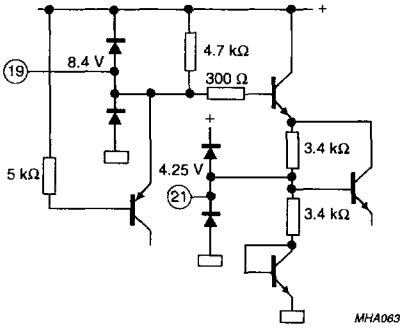


Fig.28 Pin 19: filtering for supply; pin 21: reference voltage.

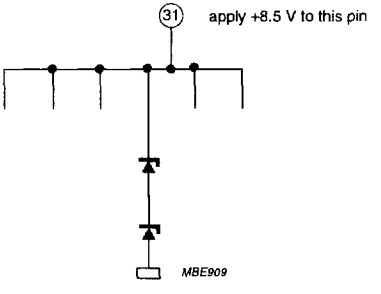


Fig.29 Pin 31: supply voltage.

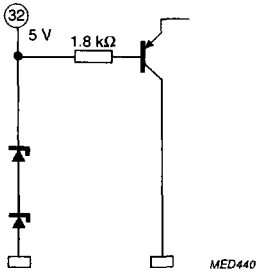


Fig.30 Pin 32: SCL (I^2C-bus clock).