FEATURES

- **A complete SONET/SDH Transmitter & Receiver**
- **Complies with Bellcore, ITU/CCITT and ANSI specifications**
- **On-chip PLL for clock generation**
- **SONET framing (defeatable)**
- **Supports 622.08 Mbits/sec data rates (OC-12)**
- **Reference frequency of 19.44MHz, 51.84MHz or 77.76MHz**
- ***TTL/CMOS-compatible parallel I/O***
- **Differential PECL high-speed serial I/O**
- **Single +5 volt power supply**
- **Frame Detect output**
- **Compatible with Synergy's SY87701 Clock Recovery Unit and other SONET-compliant clock recovery devices**
- **Seamless operation with PMC-Sierra's PM5355 S/UNI-622**
- **Available in compact 100-pin thermally enhanced metal and plastic QFP packages (plastic QFP w/ embedded heatslug)**

DESCRIPTION

Synergy's SY69612 Transceiver contains a fully-integrated serialization/deserialization SONET OC-12 (622.08 Mbit/s) interface circuit. This device performs all necessary serial-to-parallel and parallel-to-serial conversions per SONET and SDH standards. The SY69612 is ideally suited for SONET-based ATM applications, and is fabricated in Synergy's proprietary ASSET™ bipolar process.

On-chip clock generation is performed by a low-jitter phase-locked loop (PLL), allowing use of a 77.76MHz, 51.84MHz or 19.44MHz clock as a reference. Clock recovery is performed via an external recovery chip, such as Synergy's SY87701V, or via an integrated Optical-to-Electrical module. The SY69612 can also perform SONET/SDH frame detection and alignment on the input data stream.

Compliance with the bit-error rate requirements of the Bellcore, ITU/CCITT and ANSI standards is ensured by Synergy's advanced PLL technology and Positive-ECL (PECL) I/O.

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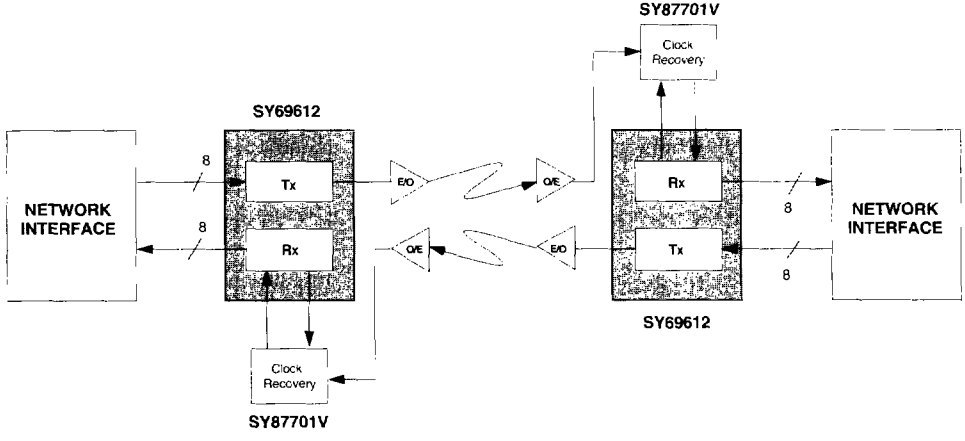
BLOCK DIAGRAM



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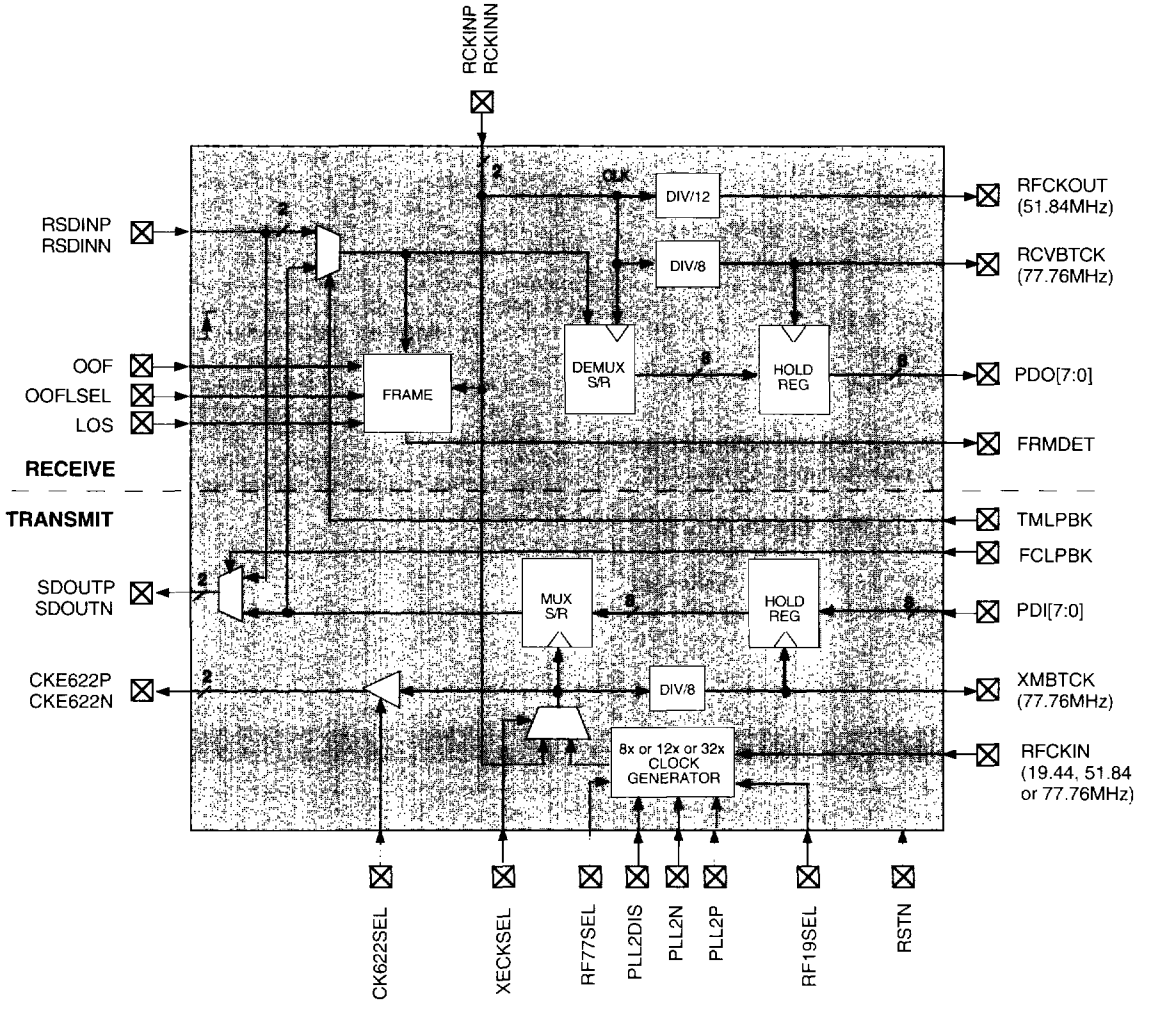
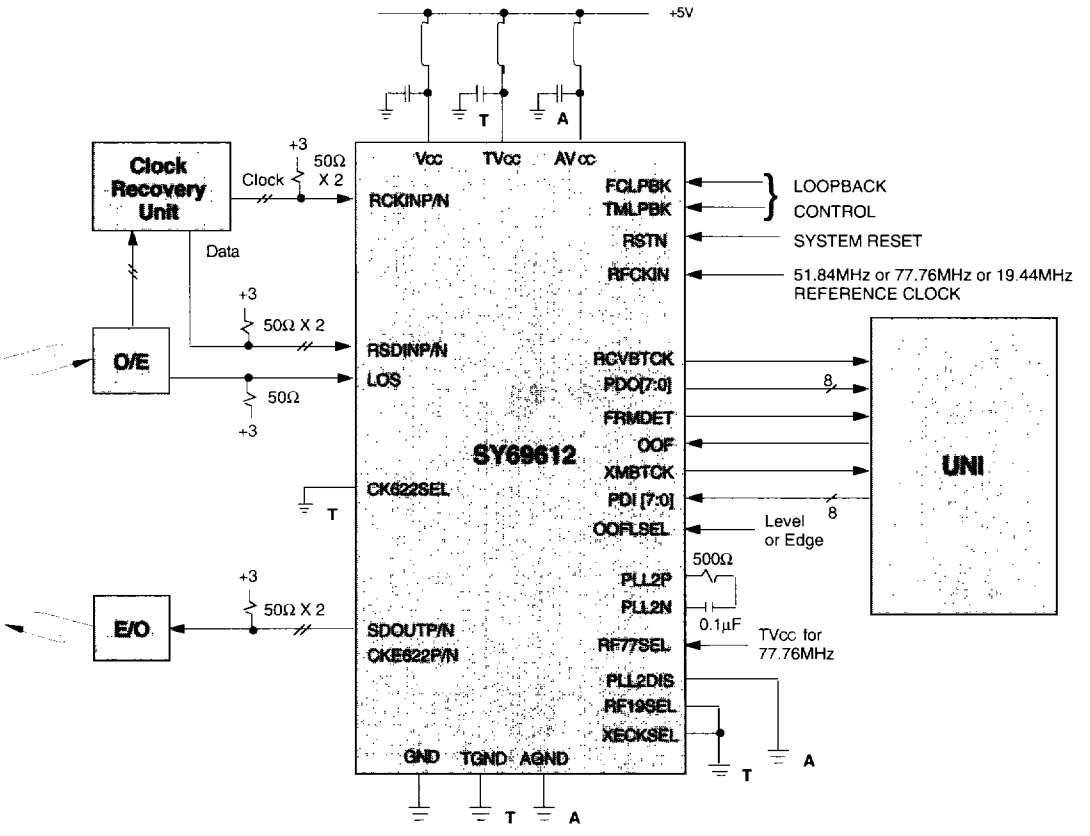
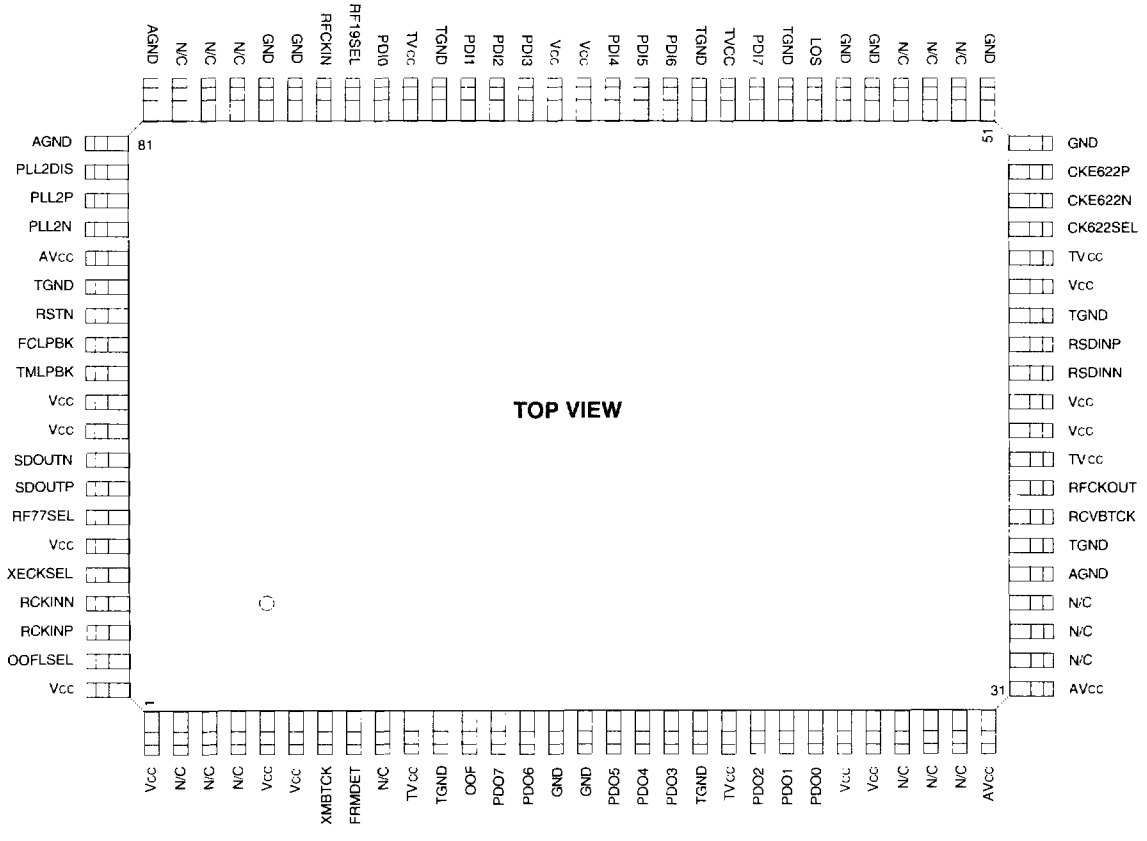
FUNCTIONAL BLOCK DIAGRAM



SYSTEM CONNECTION DIAGRAM



PINOUT



PIN NAMES

INPUTS

RSDINP, RSDINN [Serial Data Input] Differential PECL.
These pins are normally connected to the optical receiver module.

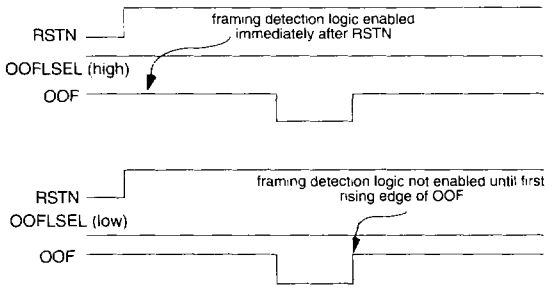
PDI[7:0] [Parallel Data Input] TTL.
A 77.76 Mbyte/s word aligned to the XMBTCK transmit byte clock. PDI7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PDI[7:0] is sampled on the rising edge of XMBTCK.

OOF [Out Of Frame Input] TTL.
Signal used to enable/disable the framing pattern detection logic. The framing pattern detection logic is enabled on the rising edge of OOF and remains enabled until frame boundary is detected. OOF is an asynchronous signal with a minimum pulse width of one RCVBTCK period. See OOFLSEL signal description.

OOFLSEL [Out Of Frame Level] TTL.
The purpose of this signal is to determine how the OOF (Out of Frame Input) is treated at power on. If OOFLSEL is held low while RSTN is asserted (active low), then the framing pattern detection logic will not be enabled until the first rising edge on OOF after RSTN has gone away (high).

PIN NAMES (contd.)

If OOFLSEL is held high while RSTN is asserted, then the framing pattern detection logic will be enabled as soon as OOF goes high. This means that if OOF is already high during RSTN and remains high (so no rising edge of OOF has occurred), the framing detection logic will still be enabled.



NOTE:

1. The OOFLSEL input only makes a difference at power on. Once the first rising edge of OOF has occured, the OOF input is treated in exactly the same manner from that point on (whether OOFLSEL is high or low). From that point on, the framing detection logic is enabled whenever a low-to-high transition occurs on OOF.

RFCKIN [Reference Clock Input] TTL/PECL.

Input normally used to generate the XMBTCK. This signal is also used to generate the 'training' frequency for the clock recovery circuit to keep it centered at 622.08MHz in the absense of data coming in on the RSDINP, RSDINN inputs. The RFCKIN can be either 19.44MHz, 51.84MHz (TTL) or 77.76MHz (PECL, single-ended) and can be selected with RF19SEL and RF77SEL.

RF77SEL [Reference Clock High Frequency Select Input] TTL.

A low lets the SY69612 default to the RF19SEL pin to determine if this input frequency is 19.44MHz or 51.84MHz. If this pin is high, then the SY69612 will be set for a 77.76MHz (PECL, single-ended) input frequency.

RF19SEL [Reference Clock Select Input] TTL.

Signal used to select the RFCKIN frequency. A high selects 19.44MHz as the Reference Clock and a low selects 51.84MHz as the Reference Clock. A 51.84MHz or 77.76MHz reference clock should be used in SONET applications.

LOS [Loss of Signal] PECL.

A single-ended active high input to be driven by the external optical receiver module to indicate a loss of received optical power. When LOS is high, the data on the Serial Data Input (RSDINP, RSDINN) pin will be internally forced to a constant low (zero). When LOS is low, data on the RSDINP, RSDINN pins will be processed normally.

TMLPBK [Terminal Loopback] TTL. (Active Low)

Selects terminal loopback diagnostic mode. When TMLPBK is low, the parallel data presented on PDI[7:0] is looped back via the serial receive side and presented back on the PDO[7:0] along with the recovered clock. Should be high for normal operation.

FCLPBK [Facility Loopback] TTL. (Active Low)

Selects facility loopback diagnostic mode. When FCLPBK is low, the serial data coming on the RSDINP, RSDINN pins is routed out via the SDOUTP, SDOUTN pins. Should be high for normal operation.

RSTN [Master Reset] TTL. (Active Low)

An active low signal that resets the device. Frame detection is disabled after master reset. RSTN must be low for 1 millisecond minimum. Should be HIGH for normal operation.

PLL2N, PLL2P [Loop Filter]

Loop filter pins for the clock synthesis PLL.

PLL2DIS [PLL Disable] TTL.

Normally connected to AGND this input can be used to disable the PLL for test purposes. A high on PLL2DIS will disable the clock synthesis PLL.

CK622SEL [622.08MHz Clock Out Select] TTL.

A high on this pin will present the external 622.08MHz clock on the CKE622P and CKE622N pins. A low disables the output and minimizes noise.

XECKSEL [Transmit External Clock Select] TTL.

A high on this pin allows the RCKINP and RCKINN inputs to be used as the 622.08MHz transmit clock. This is tied to TGND for normal (internal clock recovery) operation.

RCKINP, RCKINN [External 622.08MHz Clock Input]
Differential PECL.

These pins are normally connected to the optical receiver module that has on-board clock recovery, or an external clock recovery device.

OUTPUTS

SDOUTP, SDOUTN [Serial Data Output] Differential PECL.

These pins are normally connected to the optical transmitter module.

PDO[7:0] [Parallel Data Output] TTL.

A 77.76 Mbyte/s word aligned to the RCVBTCK receive byte clock. PDO7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PDO[7:0] is updated on the falling edge of RCVBTCK.

PIN NAMES (contd.)

OUTPUTS (Continued)

RFCKOUT [Reference Clock Output] TTL.
A 51.84MHz clock provided as a reference clock.

RCVBTCK [Receive Byte Clock] TTL.
A 77.76MHz clock that is aligned to the PDO[7:0] parallel data output. It is a nominally 50% duty cycle clock.

XMBTCK [Transmit Byte Clock] TTL.
A 77.76MHz reference clock generated from the RFCKINP, RFCKINN pins. It is to be used to coordinate byte transfers for serial transmission. PDI7-0 is sampled on the rising edge of XMBTCK.

FRMDET [Frame Detect] TTL.
Indicates SONET frame boundaries in the incoming data stream (RSDINP, RSDINN). If the framing pattern detection is enabled, with OOF input, FRMDET pulses high for one RCVBTCK cycle when a 48-bit sequence matching the framing pattern is detected on the RSDINP, RSDINN inputs. FRMDET is updated on the falling edge of RCVBTCLK.

CKE622P, CKE622N [622.08 MHz Transmit Clock Output]
Differential PECL.
These pins provide the 622.08MHz transmit clock depending on the state of the CK622SEL pin. When CK622SEL is low the CKE622P will remain high (PECL) and CKE622N will remain low (PECL). These pins can be connected to optical transmit modules that require both data and clock inputs.

OTHER

V_{CC}	ECL +5V
AVcc	Analog +5V
GND	ECL Ground
AGND	Analog Ground
TVcc	TTL +5V
TGND	TTL Ground
N/C	No Connect[1]

NOTE:
1. N/C pins are recommended to be tied to GND (ECL Ground).

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter		Rating	Unit
V_{CC}, TVcc, AVcc	Power Supply (GND, TGND, AGND = 0V)		0 to +7	V
V_I	Input Voltage (GND, TGND, AGND = 0V)		0 to V_{CC}	V
I_{OUT}	Output Current	Continuous	50	mA
		Surge	100	
T_j	Junction Temperature Range		0 to +125	°C
Tstore	Storage Temperature Range		-65 to +150	°C

NOTE:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS[1], [2], [3]

V_{CC} = +5V ±5%; V_{EE} = GND = 0V, T_j = 0°C to +125°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{EE}	Internal Operating Current	—	488	—	mA	
I_{OUT}	Termination Output Current	—	11	—	mA	50Ω to Vcc -2, 50% duty cycle

NOTES:
1. To calculate total power supply current into the V_{CC} pins: $I_{CC} = (n * I_{OUT})$; where n = number of ECL output pins used (ie, terminated).
2. To calculate total device power dissipation: $P_D = [I_{EE} * (V_{CC} - V_{EE})] + [n * I_{OUT} * 1.33]$[3].
3. Average ECL output voltage is calculated as $V_{OAVG} = (V_{OH(MAX)} + V_{OH(MIN)} + V_{OL(MAX)} + V_{OL(MIN)}) /4 = 1.33V$.

PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = TV_{CC} = AV_{CC} = 4.75V to 5.25V; GND, TGND, AGND = 0V, T_j = 0°C to +125°C

Symbol	Parameter	T_j = 0°C		T_j = +25°C		T_j = +65°C		T_j = +125°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} -1.112	V_{CC} -.897	V_{CC} -1.077	V_{CC} -.862	V_{CC} -1.025	V_{CC} -.810	V_{CC} -.947	V_{CC} -.732	V
V_{OL}	Output LOW Voltage	V_{CC} -1.920	V_{CC} -1.656	V_{CC} -1.920	V_{CC} -1.644	V_{CC} -1.920	V_{CC} -1.620	V_{CC} -1.920	V_{CC} -1.584	V
V_{IH}	Input HIGH Voltage[1]	V_{CC} -1.209	V_{CC} -.888	V_{CC} -1.172	V_{CC} -.858	V_{CC} -1.125	V_{CC} -.810	V_{CC} -1.045	V_{CC} -.738	V
V_{IL}	Input LOW Voltage[1]	V_{CC} -1.920	V_{CC} -1.604	V_{CC} -1.920	V_{CC} -1.567	V_{CC} -1.920	V_{CC} -1.520	V_{CC} -1.920	V_{CC} -1.140	V
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	0.3	—	µA

NOTE:

1. Forcing one input at a time. Apply V_{IH} (max) or V_{IL} (min) to all other inputs.

TTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = TV_{CC} = AV_{CC} = 4.75V to 5.25V; GND, TGND, AGND = 0V, T_j = 0°C to +125°C

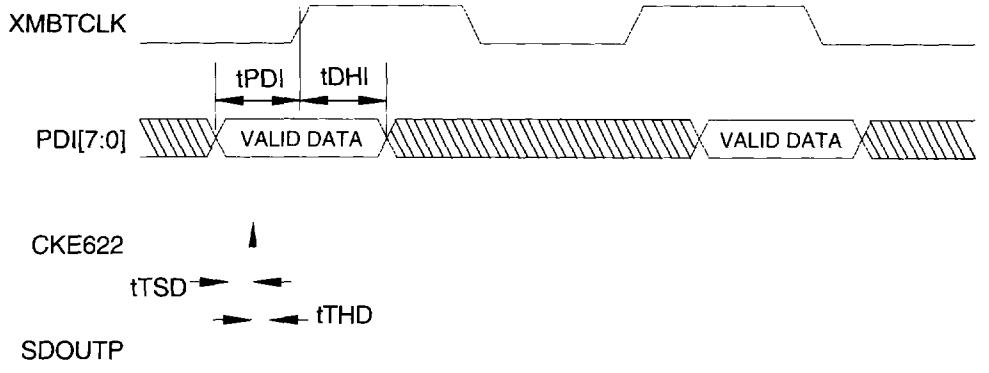
Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.4	—	V	I_{OH} = –2mA
V_{OL}	Output LOW Voltage	—	0.5	V	I_{OL} = 4mA
I_{OS}	Output Short Circuit Current	–150	–60	mA	V_{OUT} = 0V
V_{IH}	Input HIGH Voltage	2.0	—	V	—
V_{IL}	Input LOW Voltage	—	0.8	V	—

AC ELECTRICAL CHARACTERISTICS

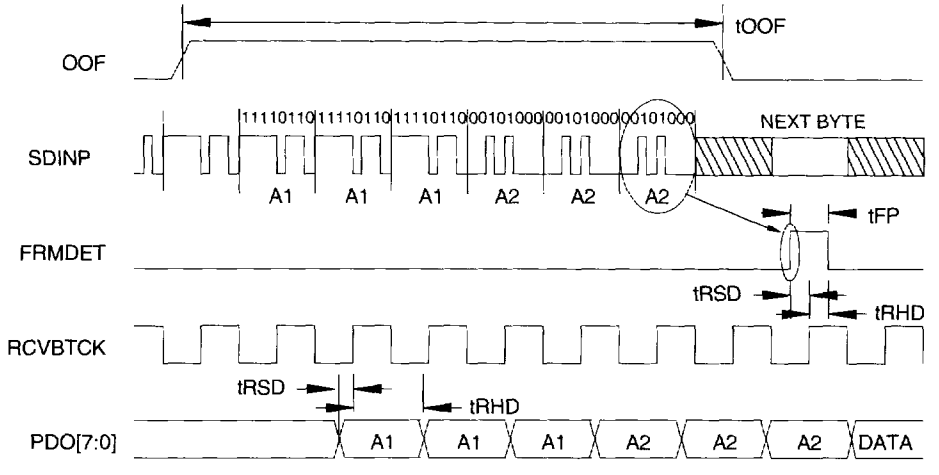
V_{CC} = TV_{CC} = AV_{CC} = 4.75V to 5.25V; GND, TGND, AGND = 0V, T_j = 0°C to +125°C

Parameter	Min.	Typ.	Max.	Units	Condition
VCO Center Frequency		622.08 ±12%		MHz	Nominal
Reference Clock (RFCKIN) Frequency Tolerance	— — —	±20 ±20 ±10	— — —	ppm ppm ppm	77.76MHz 51.84MHz 19.44MHz
Reference Clock (RFCKIN) Input Duty Cycle	45	—	55	% of UI	
Reference Clock (RFCKOUT) Output Duty Cycle	40	—	60	% of UI	15pF load
TTL Output Rise/Fall Time	—	—	4	ns	10% to 90% of amplitude, 15pF load
PECL Output Rise/Fall Time	—	—	500	ps	10% to 90%, 50Ω load, 5pF cap
tPDI : PDI[7:0] set-up with respect to XMBTCK	1.8	—	—	ns	15pF load
tDHI : PDI[7:0] hold time with respect to XMBTCK	1	—	—	ns	15pF load
tOOF : OOF pulse width	12.86	—	—	ns	
tRSD : PDO[7:0] & FRMDET valid before RCVBTCK	4	—	—	ns	15pF load
tRHD : PDO[7:0] & FRMDET valid after RCVBTCK	4	—	—	ns	15pF load
XMBTCK & RCVBTCK Duty Cycle	40	—	60	% of UI	
CKE622 Output Duty Cycle	45	—	55	% of UI	
tTSD : SDOUTP valid before CKE622	0.30	—	—	ns	
tTHD : SDOUTP valid after CKE622	0.30	—	—	ns	
tRST : RSTN pulse width	1	—	—	msec	

TRANSMIT TIMING WAVEFORMS



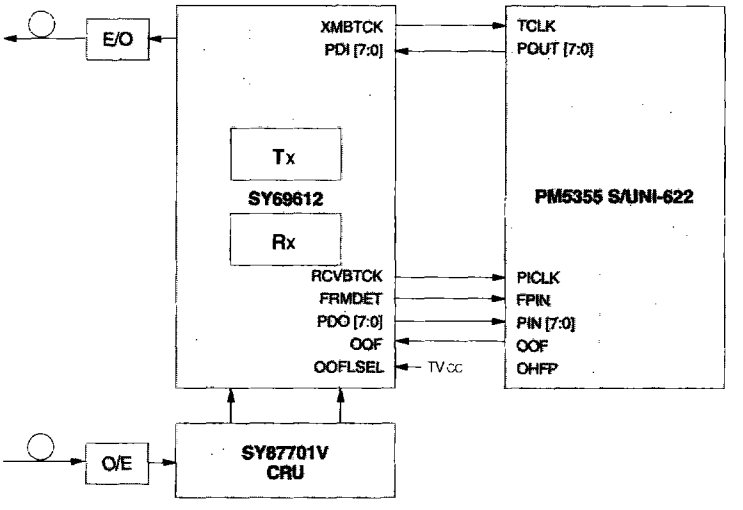
RECEIVE TIMING WAVEFORMS(1)



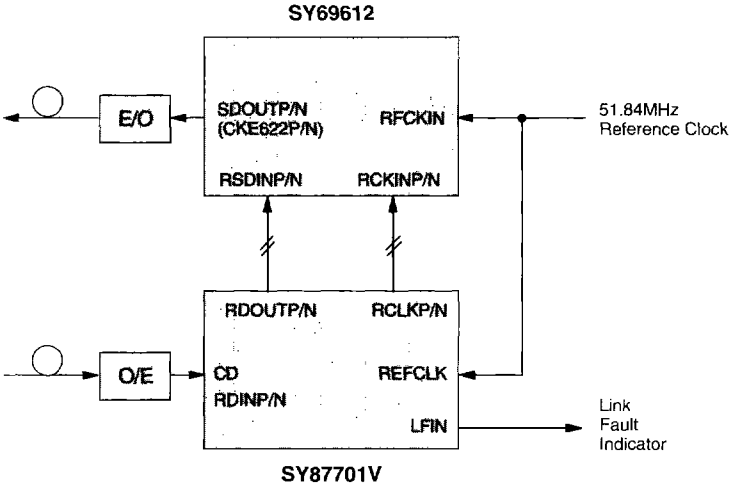
NOTES:
1. The example shown above is for a partial OC-12 framing sequence.

APPLICATION EXAMPLE

SY69612 interface with S/UNI–622



SY69612 interface with SY87701V Clock Recovery Unit



PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY69612BC	B100-1	Commercial
SY69612QC	Q100-1	Commercial