FAIRCHILD
A Schlumberger Company

μA198/298/398 Monolithic Sample and Hold Amplifiers

Data Acquisition Products

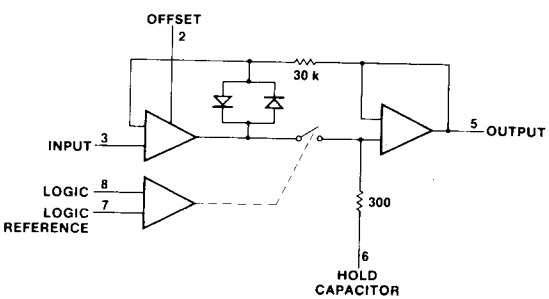
General Description

The μA198/298/398 are Monolithic Sample and Hold Amplifiers which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is typically 4 μs to 0.1%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the μA198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\ \Omega$ allows high source impedances to be used without degrading accuracy.

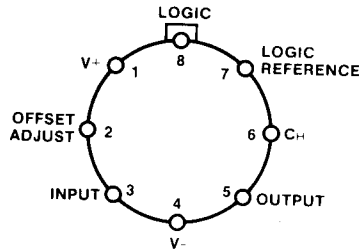
P-channel junction FETs are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 μF hold capacitor. The JFETs have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees excellent feedthrough rejection from input to output in the hold mode even for input signals equal to the supply voltages.

- **OPERATES FROM ±5 V TO ±18 V SUPPLIES**
- **ACQUISITION TIME TO .1% TYPICALLY 4 μs**
- **TTL, PMOS, CMOS COMPATIBLE LOGIC INPUT 1.4 V DIFFERENTIAL THRESHOLD**
- **0.5 mV TYPICAL HOLD STEP AT C_H = 0.01 μF**
- **LOW INPUT OFFSET**
- **0.002% GAIN ACCURACY**
- **LOW OUTPUT NOISE IN HOLD MODE**
- **HIGH SUPPLY REJECTION RATIO IN SAMPLE OR HOLD**
- **WIDE BANDWIDTH**

Functional Diagram



Connection Diagram
8-Pin Metal Package

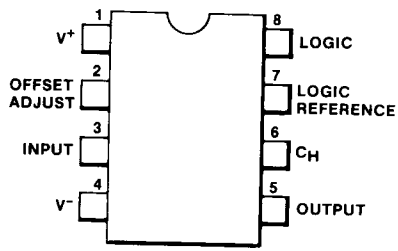


(Top View)

Order Information

Type	Package	Code	Part No.
μA198	Metal	5W	μA198HM
μA298	Metal	5W	μA298HC
μA398	Metal	5W	μA398HC

Connection Diagram
8-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA198	Molded	6T	μA198RM
μA298	Molded	6T	μA298RC
μA398	Molded	6T	μA398RC

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Absolute Maximum Ratings

Supply Voltage	± 18 V	Storage Temperature Range	−65°C to +150°C
Power Dissipation (Package Limitation) (Note 1)	500 mW	Input Voltage	Equal to Supply Voltage
Operating Ambient Temperature Range		Logic-to-Logic Reference Differential Voltage (Note 2)	+7 V, −30 V
μA198	−55°C to +125°C	Output Short Circuit Duration	Indefinite
μA298	−25°C to +85°C	Hold Capacitor Short Circuit Duration	10 s
μA398	0°C to +70°C	Pin Temperature (Soldering, 10 s)	300°C

μA198/μA298/μA398
Electrical Characteristics

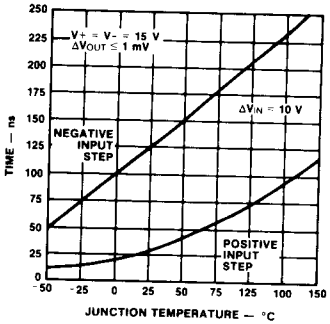
Characteristic	Conditions (Note 3)	μA198/μA298 Min	μA198/μA298 Typ	μA198/μA298 Max	μA398 Min	μA398 Typ	μA398 Max	Unit
Input Offset Voltage (Note 6)	T_J = 25°C Full Temperature Range		1	3 5		2	7 10	mV mV
Input Bias Current (Note 6)	T_J = 25°C Full Temperature Range		5	25 75		10	50 100	nA nA
Input Impedance	T_J = 25°C		10^{10}			10^{10}		Ω
Gain Error	T_J = 25°C, R_L = 10 k Full Temperature Range		0.002	0.005 0.02		0.004	0.01 0.02	% %
Feedthrough Attenuation Ratio at 1 kHz	T_J = 25°C, C_H = 0.01 μF V7 = V8 = 0 V	86	96		80	90		dB
Output Impedance	T_J = 25°C, "HOLD" mode Full Temperature Range		0.5	2 4		0.5	4 6	Ω Ω
"HOLD" Step (Note 4)	T_J = 25°C, C_H = 0.01 μF, V_{OUT} = 0		0.5	2.0		1.0	2.5	mV
Supply Current (Note 6)	$T_J \geq$ 25°C		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	T_J = 25°C		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	T_J = 25°C (Note 5) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	ΔV_{OUT} = 10 V, C_H = 1000 pF		4			4		μs
	C_H = 0.01 μF		20			20		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT}$ = 2 V		5			5		mA
Supply Voltage Rejection Ratio	V_{OUT} = 0	80	110		80	110		dB
Differential Logic Threshold	T_J = 25°C	0.8	1.4	2.4	0.8	1.4	2.4	V

Notes

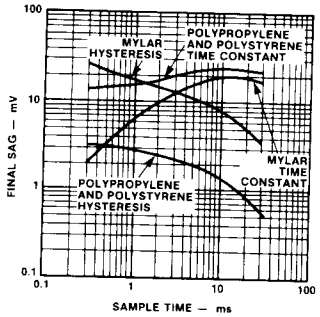
1. The maximum junction temperature of the μA198 is 150°C, for the μA298 is 115°C, and for the μA398 is 100°C. When operating at elevated ambient temperature, the TO-5 package must be derated based on a thermal resistance (Θ_{ja}) of 150° C/W and the R package at (Θ_{ja}) of 130° C/W.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2 V below the positive supply and 3 V above the negative supply.
3. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, V_S = ± 15 V, T_J = 25°C, −11.5 V ≤ V_{IN} ≤ +11.5 V, C_H = 0.01 μF, and R_L = 10 kΩ. Logic reference voltage = 0 V and logic voltage = 2.5 V.
4. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5 V logic swing and a 0.01 μF hold capacitor. Magnitude of the hold step is inversely proportional to capacitor value.
5. Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
6. These parameters guaranteed over a supply voltage range of ± 5 to ± 18 V.

Typical Performance Curves

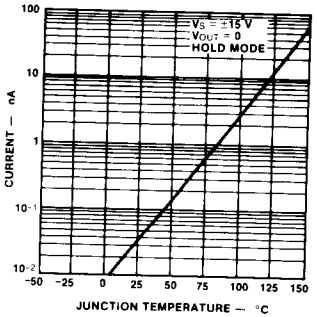
Aperture Time



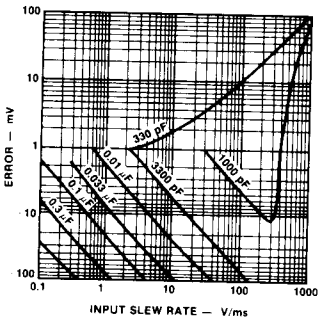
Capacitor Hysteresis



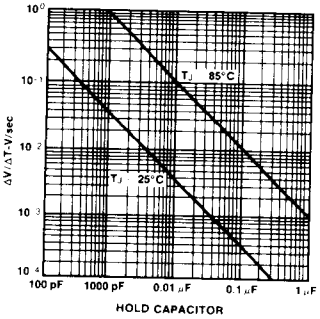
Leakage Current Into Hold Capacitor



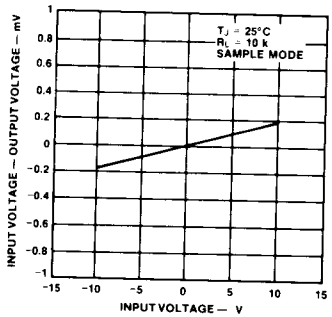
Dynamic Sampling Error



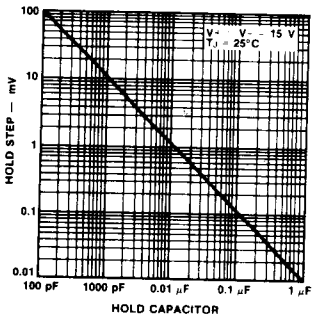
Output Droop Rate



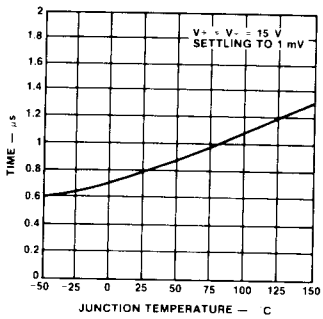
Gain Error



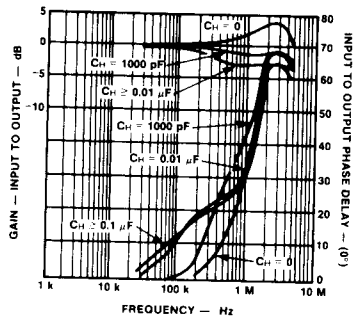
Hold Step



"Hold" Settling Time



Phase and Gain (Input to Output, Small Signal)



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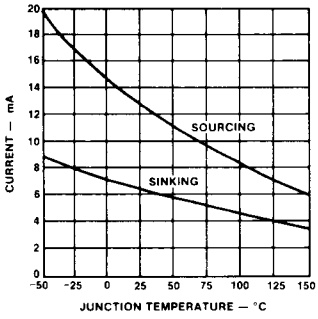
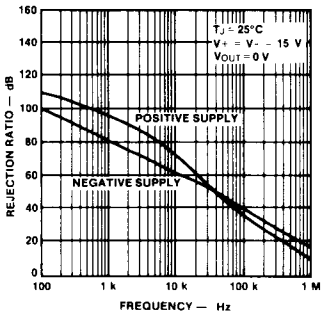
Typical Performance Curves (Cont.)

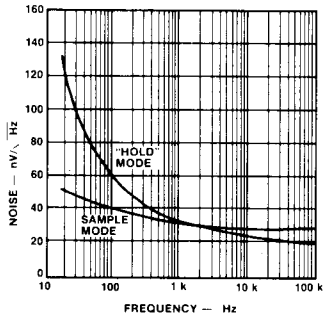
Output Short-Circuit Current



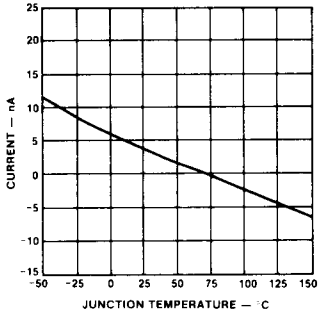
Power Supply Rejection



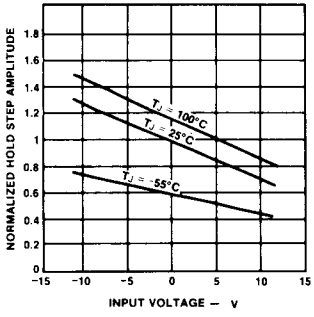
Output Noise



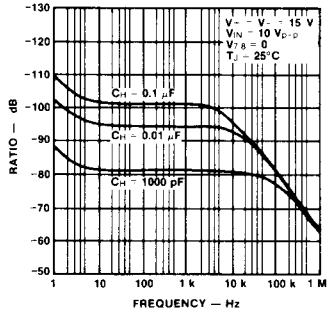
Input Bias Current



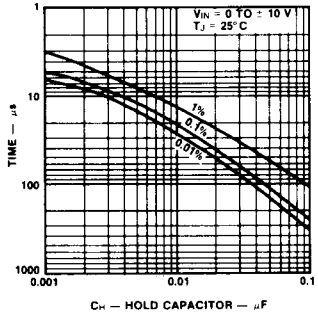
Hold Step vs Input Voltage



Feedthrough Rejection Ratio (Hold Mode)

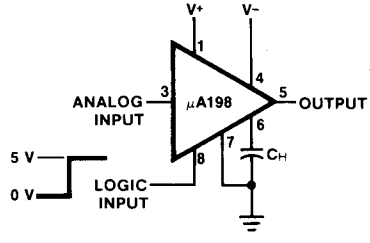


Acquisition Time



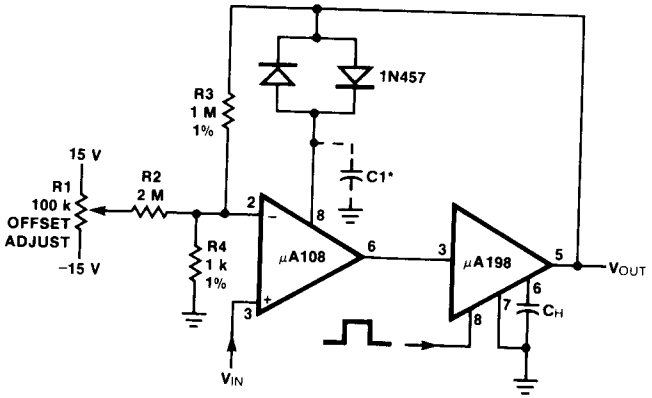
Typical Applications

X1 Sample and Hold



Typical Applications (Cont.)

X1000 Sample and Hold

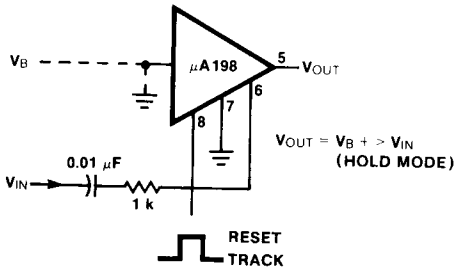


Notes

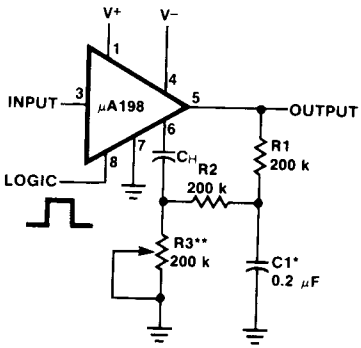
For lower gains, the μA108 must be frequency compensated

Use $\approx \frac{100}{A_V}$ pF from comp 2 to ground

Sample and Difference Circuit (Output Follows Input in Hold Mode)



Capacitor Hysteresis Compensation

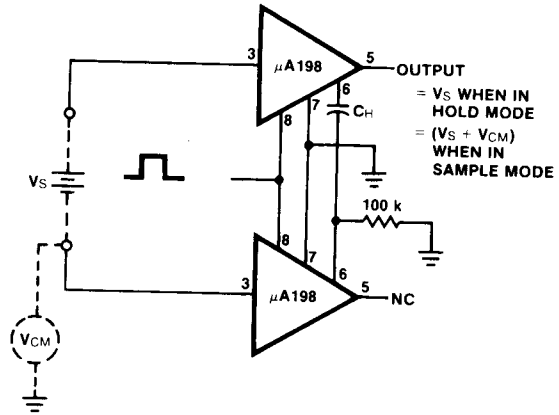


Notes

*Select for time constant C1 $\approx \frac{\tau}{100\text{ k}}$

**Adjust for amplitude

Differential Hold



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