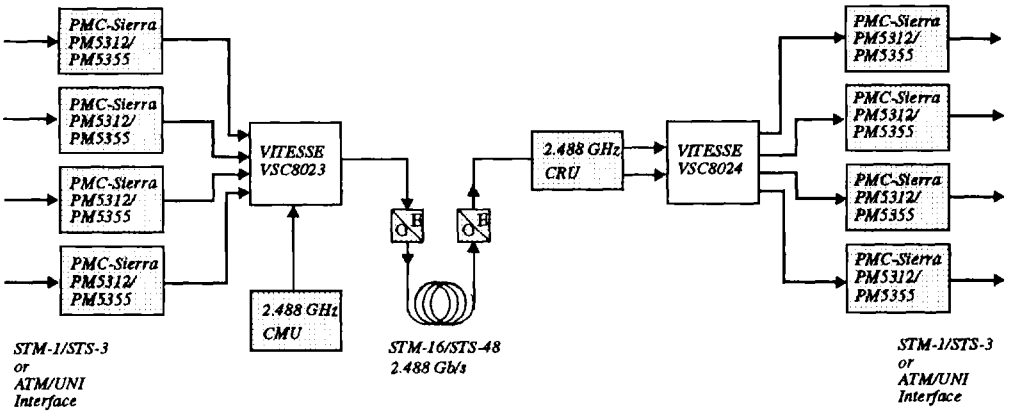
Preliminary Datasheet

2.488 Gbits/sec SDH/SONET STM-16/STS-48 Mux/Demux and Section Terminator IC Chipset

Features

- Interfaces with PMC-Sierra's PM5312/5355
- Supports STS-48c Mode (User Controlled)
- Optionally Combines Four STM-4/STS-12 Data Streams into One Serial STM-16/STS-48 Data Stream According to the SDH/SONET Spec for Intermediate-level Byte Interleaving
- Optionally Separates One Serial STM-16/STS-48 Data Stream into Four STM-4/STS-12 Data Streams According to the SDH/SONET Spec for Intermediate-level Byte De-interleaving
- Optionally Performs Frame Synchronous Scrambling and Descrambling
- Optionally Modifies J0 and Z0 Bytes (Mux)
- Supports Both Contra & Co-directional Interface Modes
- Optionally Calculates and Inserts the Bit-interleaved Parity-error Detection Code B1 into the Transmit Stream (Mux)
- Compares the B1 for the Receive Stream and Declares Errors (Demux)
- Frame Error and SEF Declaration (Demux)
- LOF Declaration for SDH or SONET Systems (Demux)
- Los Control Input (Demux)
- Provides Equipment And Facility Loopbacks
- High-speed Differential ECL I/O
- Dual Supply Operation -2, +3.3 Volts
- 192 TBGA Package

System Block Diagram



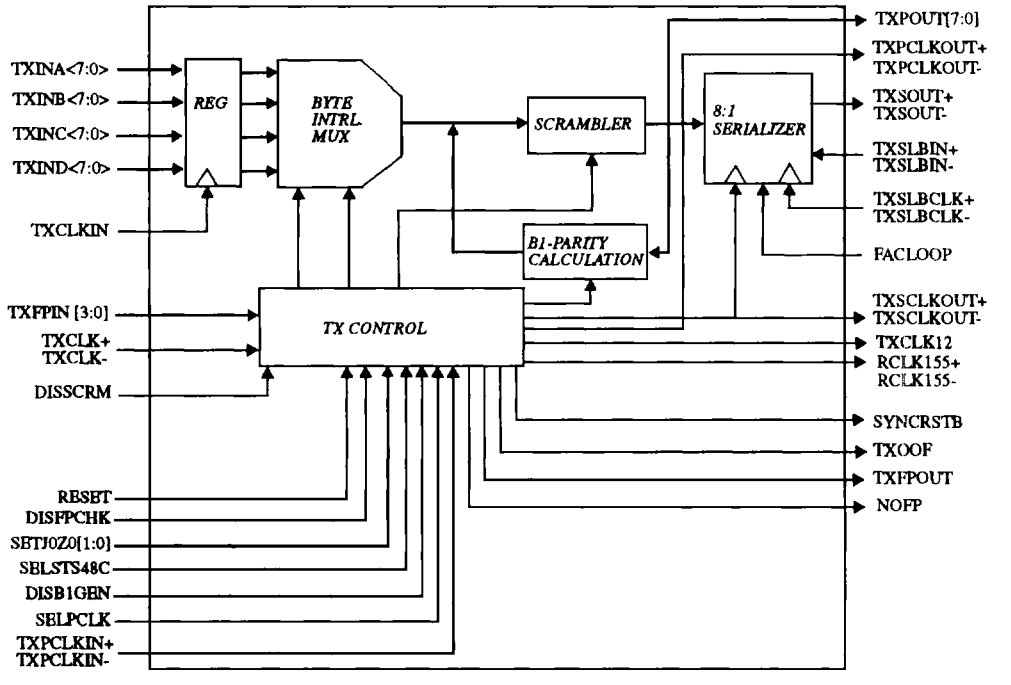
General Description

The VSC8023/VSC8024 chipset is designed to provide a SDH/SONET compliant interface between the PM5312 STTX (STM-1/STS-3 to STM-3/STS-12 mux/demux) or the PM5355 S/UNI-622 User Network Interface device and a SDH/SONET compliant 2.488 Gb/s interface, as depicted in the system block diagram above. This chipset allows one to create an ATM-UNI or STM-1/STS-3 to STM-16/STM-48 link. Both the mux (VSC8023) and the demux (VSC8024) are packaged in a 192TBGA for optimum high-speed package performance. The VSC8023/VSC8024 chipset provides an integrated solution for ATM physical layers, SDH/SONET transmission systems, digital-video distribution systems, and SDH/SONET test equipment.

VSC8023 Functional Description

The VSC8023 byte interleaves four 8-bit parallel STM-4/STS-12 data streams at 77.76MHz (from four PM5312s or four PM5355s) into a serial STM-16/STS-48 data stream at 2.488 Gb/s, consistent with the existing requirements for SONET intermediate-level multiplexing. (In order to support STS-48c, where no byte-interleaving is required, the byte-interleaver can be bypassed (straight forward muxing will occur instead) by holding the asynchronous SELSTS48C input high).

Figure 1: VSC8023 Functional Block Diagram

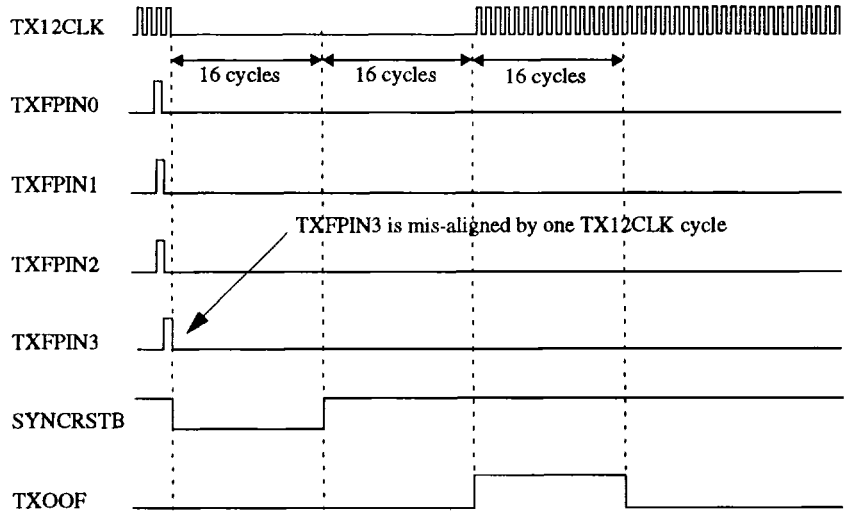


The part is clocked by a 2.488 GHz clock, which has to be provided by an external PLL. The VSC8023 is equipped with a 155.52 MHz differential ECL output clock, RCLK155+ and RCLK155-, to facilitate the creation of the external PLL circuit. The block diagram in Figure 1 shows the major functional blocks associated with the VSC8023.

Byte-wide data is presented to the TXINA<7:0>, TXINB<7:0>, TXINC<7:0>, and TXIND<7:0> input pins and is clocked into the part on the rising edge of TXCLKIN, as depicted in Figure 3. The four PM5312s or the four PM5355s each output a frame pulse aligned to the first payload byte of every frame, as shown in the functional timing diagram, Figure 3. The byte-interleave mux will be reset on the occurrence of the first valid frame pulse on TXFPIN[3:0] (active high). A valid frame pulse will only be detected if all four TXFPIN[3:0] inputs

are high at the same time. Therefore, if the four PM5312s or four PM5355s are not exactly byte aligned SYNCRSTB will be asserted low for sixteen 77.76 MHz (TXCLK12) clock cycles. TXCLK12 will be held low during these sixteen cycles and for an additional sixteen cycles thereafter. TXOOF will be held high for sixteen TXCLK12 cycles after the TXCLK12 clock starts running again to indicate that the CPU needs to reload the registers in the four PM5312s or four PM5355s. The frame-pulse check circuitry can be disabled by asserting the DISFPCHK input high. When the asynchronous DISFPCHK input is high, the output NOFP will be held high while no valid frame pulse can be detected. Please refer to Figure 2 for the Synchronous Reset timing. In Co-directional mode TXCLK12 is not connected to TXCLKIN.

Figure 2: Synchronous Reset Timing



The output of the byte-interleave mux is scrambled with the SDH/SONET scrambling polynomial $1 + x^6 + x^7$. The SDH/SONET scrambler can be disabled (on a frame wide basis only) by setting DISSCRM high. The value on the DISSCRM input is latched-in once every frame at the occurrence of the frame pulse. A logic '1' latched-in during the current frame will result in a non-scrambled current frame, and the frames thereafter.

The bit-interleaved parity byte B1 is calculated over the entire scrambled frame and inserted into the B1 location of the next frame before scrambling. This B1 generation can be disabled by setting the DISB1GEN input high. The value on this input is latched-in once every frame at the occurrence of the frame pulse. A logic '1' latched-in during the current frame will result in the B1 byte in the current frame, and in the frames thereafter, being passed on transparently.

The section-trace bytes (J0/Z0) can optionally be set to an increasing binary number from 01\hex to 30\hex by setting the SETJ0Z0[1:0] to '01'. A non-zero value on the SETJ0Z0[1:0] bus latched-in during the current

frame will result in a change of the J0/Z0 bytes in the next frame and the frames thereafter if the value on the SETJ0Z0[1:0] bus is not changed. When SETJ0Z0[1:0] is held at '00', the J0/Z0 bytes will be passed on transparently. Since the first section-trace byte, J0, could carry a section-trace message it can be passed on transparently while the Z0 bytes are set to an increasing binary number from 02\hex to 30\hex by setting SETJ0Z0[1:0] to '10'.

TXPOUT[7:0] is a parallel byte-wide STM-16/STS-48 output which can be used for an Equipment Loopback (see Figure 19) or to feed a STM-64/STS-192 MUX circuit. TXFPOUT contains a frame pulse synchronized with the parallel STM-16/STS-48 data rate. This frame pulse is aligned with the first payload byte in every STM-16/STS-48 frame. Data on TXPOUT[7:0] and TXFPOUT is clocked out on the falling edge of TXPCLKOUT+ (rising TXPCLKOUT-). When the VSC8023 is used to feed a STM-64/STS-192 MUX circuit (with byte wide data), the VSC8023 does not have to be supplied with a 2.488 GHz clock since the serial output mux is not used. Instead, a 311.04 MHz clock can be provided on the TXPCLKIN differential ECL input pins. The asynchronous SELPCLK input needs to be held high to select the TXPCLKIN.

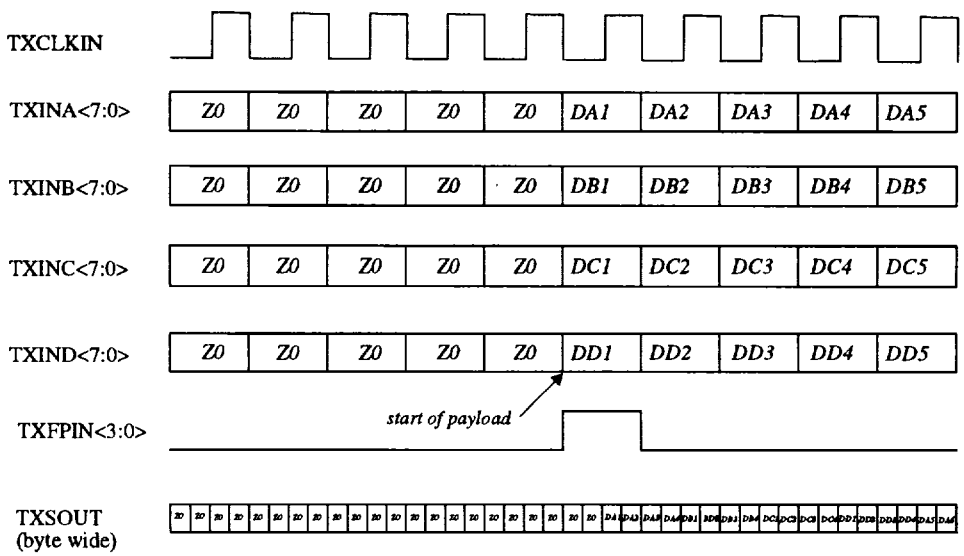
The serial STM-16/STS-48 data stream is presented at the differential TXSOUT output on the rising edge of TXSCLKOUT. To create a Facility Loopback, a high-speed clock (TXSLBCLK) and data (TXSLBIN) input have been provided. When the asynchronous FACLOOP input is held high, the data on TXSLBIN is clocked out through TXSOUT on the rising edge of the TXSLBCLK clock. Please refer to Figure 19 for a detailed Facility Loopback circuit diagram.

In order to support STS-48c, where no byte-interleaving is required, the byte-interleaver will multiplex one byte (from every STM-4/STS-12 data stream) at a time, instead of four bytes, by holding the SELSTS48C input high.

Table 1: Section-trace Byte Select Settings

SETJ0Z0[1]	*SETJ0Z0[0]*	*Function*
0	0	Transparent
0	1	J0 Transparent, Z0:02-30/hex
1	0	01-30/hex
1	1	Undefined

Figure 3: VSC8023 Functional Timing Diagram



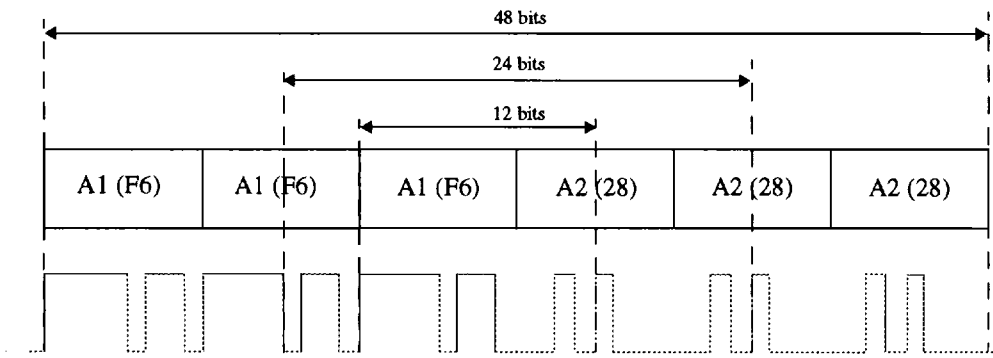
Notes:

(1) The correct latency between the TXIN data-stream inputs and the TXSOUT data-stream output is NOT shown.
(2) MSB leads on TXSOUT; MSB is bit 7 on the TXINA, TXINB, TXINC and TXIND data busses.

VSC8024 Functional Description

The VSC8024 deserializes a 2.488 Gb/s data stream into a byte-wide data stream and recovers the SDH/SONET frame boundary. The SDH/SONET frame boundary is found by detecting the inner-most 24 bits of the last two A1 bytes and the first two A2 bytes in each frame or three A1 bytes and three A2 bytes, as shown in figure 4, when the SELFRDET[1:0] input signals are held low. The frame recovery is initiated when FRDETEN is held high. This control signal is level-sensitive and the VSC8024 will continually perform frame detection as long as FRDETEN is held high.

Figure 4: Frame Boundary Detection Bits



A frame detect based on these 24 bits will result in a SEF (Severely Errored Frame) detect at an average of no more than once every 6 minutes assuming a BER of 10^{-3} as specified by the SONET Bellcore spec. As an option, one can also base the frame-boundary detect on either the three innermost A1 and the three innermost A2 bytes (48 bits) or on the last A1 byte and the first four bits of the first A2 byte (12 bits), based on the SELFRDET[1:0] settings shown in Table 2. A frame detect based on 48 or 12 bits will result in a mean time between SEF detects of 0.43 and 103 minutes, respectively. The frame-detection and recovery circuit can be disabled by holding both asynchronous SELFRDET[1:0] inputs high. In this mode, data is muxed to the output (scrambling, B1 insertion, B1 calculation, and error detection functions are disabled).

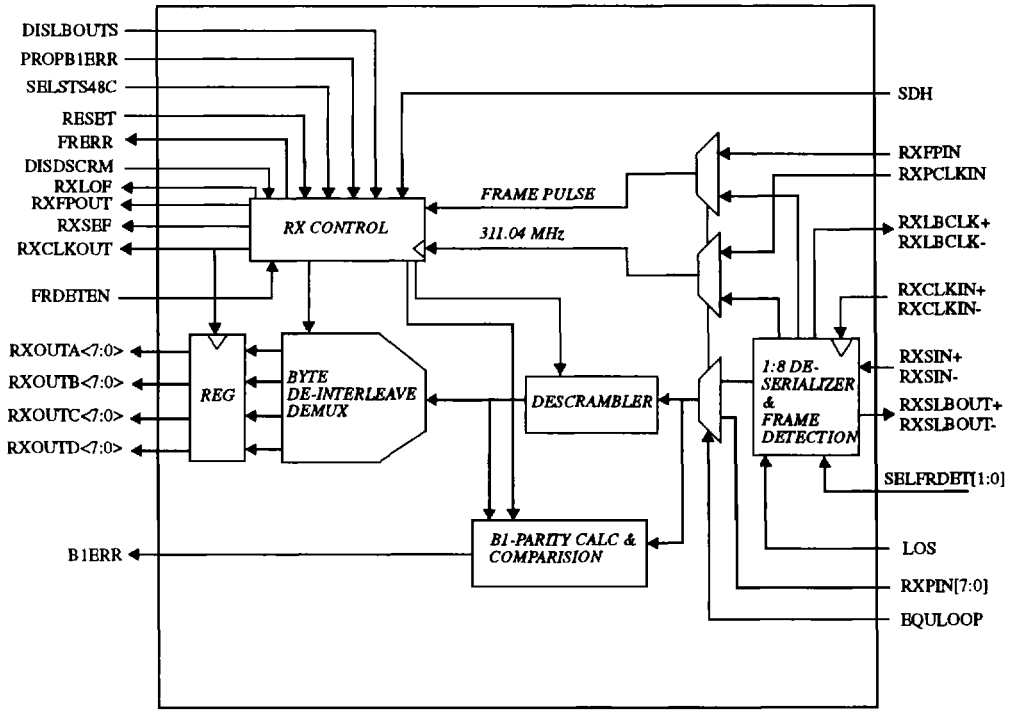
Table 2: Frame-detect Select Settings

Function	*SELFRDET1*	*SELFRDET0*
24 bits	1	0
48 bits	0	1
12 bits	0	0
Frame detection disabled	1	1

After the 1:8 Demux, the 8-bit parallel STM-16/STS-48 data stream at 311.04 MHz is byte de-interleaved into four 8-bit parallel STM-4/STS-12 data streams at 77.76 MHz (to four PM5312s or four PM5355s), consistent with the existing requirements for SDH/SONET intermediate level de-multiplexing. (In order to support STS-48c where no byte de-interleaving is required, the byte de-interleaver can be bypassed (straight forward demuxing will occur instead) by holding the asynchronous SELSTS48C input high). The part is clocked by a 2.488 GHz clock from the Clock and Data Recovery Unit (CRU). The block diagram in Figure 5 shows the major functional blocks associated with the VSC8024.

Serial STM-16/STS-48 data is presented at the differential RXSIN input on the rising edge of RXSCLKIN+; refer to Figure 12. In order to create a Facility Loopback the registered RXSIN data and the RXSCLKIN are brought out of the chip (RXSLBOUT and RXSLBCLK). These two signals should be connected to the TXSLBIN and TXSLBCLK inputs on the VSC8023 in order to create a Facility Loopback. RXSLBOUT and RXSLBCLK outputs were added to minimize the loading on the high-speed clock and data lines coming from the RX optics module. In order to minimize the jitter on the RXSIN and RXSCLKIN inputs during normal operation, the RXSLBOUT and RXSLBCLK outputs can be disabled by holding the asynchronous input DISHSOUTS high. Please refer to Figure 19 for a detailed Facility Loopback circuit diagram.

Figure 5: VSC8024 Functional Block Diagram



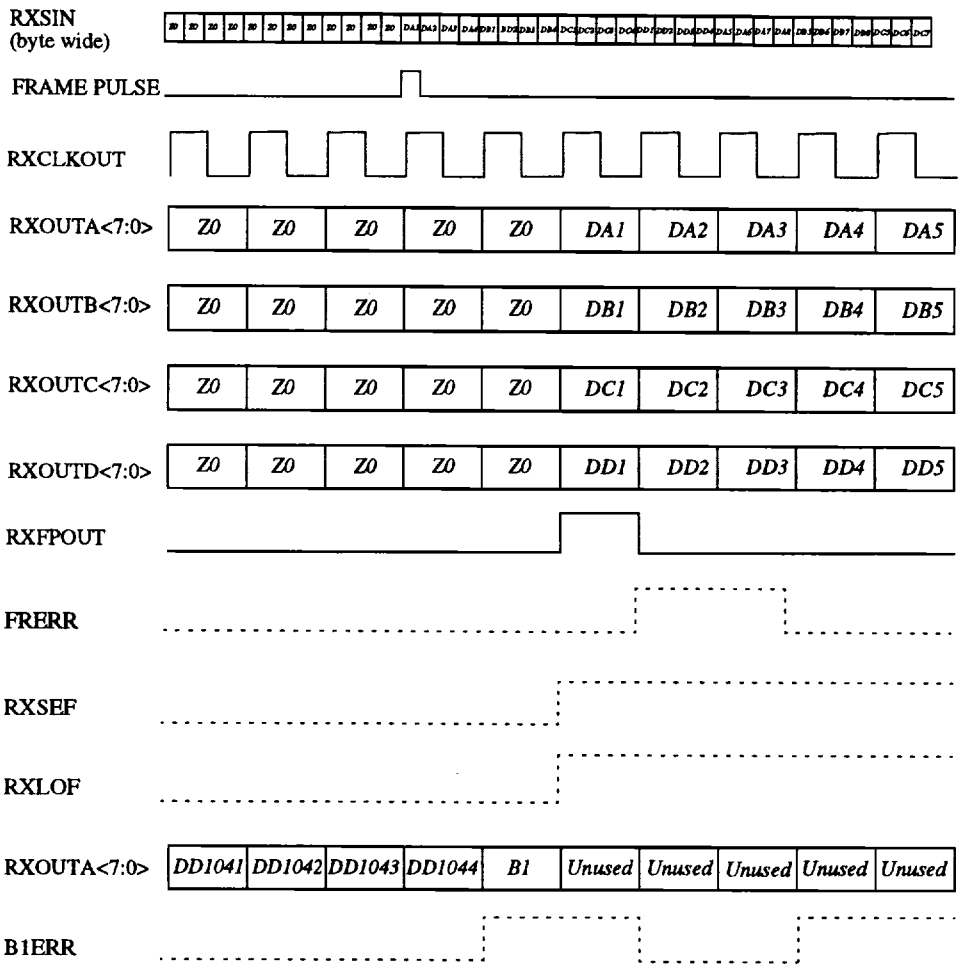
The incoming data is optionally descrambled with the SDH/SONET scrambling polynomial and byte de-interleaved into four byte-wide parallel data streams and presented on the RXOUTA<7:0>, RXOUTB<7:0>, RXOUTC<7:0>, and RXOUTD<7:0> output pins at the rising edge of RXCLKOUT; refer to Figure 6 for the functional timing of the receive circuit. The SDH/SONET de-scrambler is disabled (on a frame-wide basis only) by asserting DISDSCRM high. The value on the DISDSCRM input is latched-in once every frame at the occurrence of the frame pulse. If DISDSCRM is set high and latched in during the current frame, the current frame and all subsequent frames will remain scrambled until DISDSCRM is set low. On system reset, the chip will start off in the severely errored frame (SEF) state; RXSEF will be high. The byte de-interleaver will be reset on the occurrence of the first frame pulse from the SDH/SONET frame-detection circuit. The SEF will be removed when two consecutive error-free frames have been received. When errored frames are being received, SEF will be set high after four consecutive errored frames. Again, the SEF will be removed when two consecutive error-free frames have been received. The FRERR output will show a 25.72 ns wide pulse once every frame if the 12, 24 or 48 bits in the A1 and A2 frame ID bytes (used to recover the SDH/SONET frame boundary) contain one or more bit errors.

LOF (loss-of-frame) is declared (RXLOF output) after the chip has been in the SEF state for 3 ms (24 frames), for both SDH and SONET. The LOF state is cleared 1ms after terminating SEF Detect when in the SONET mode, or after only two good consecutive frames, when in the SDH mode. SDH mode is set by asserting the SDH input high. For loss-of-signal (LOS) conditions, the VSC8024 is equipped with a LOS control input. Asserting this input high will result in the propagation of all zeroes down-stream. In this mode, the VSC8024 is clocked by RXPCLKIN.

The bit-interleaved parity byte B1 will be recalculated before descrambling and compared to its extracted value after descrambling. The B1 bit errors will be presented on the B1ERR output as 25.72 ns wide pulses (up to 8 pulses per frame) and aligned at the start of the B1 byte of the current frame. Besides calculating the B1 over the entire STM-16/STS-48 frame, the VSC8024 optionally calculates the B1 based on the first STM-4/STS-12 frame interleaved into the STM-16/STS-48 frame when the PROPB1ERR input is held high. The value on the PROPB1ERR input is latched-in once every frame at the occurrence of the frame pulse. A logic '1' latched-in during the current frame will result in a non-modified $B1_{STS\text{-}12\#1}$ in the current frame and in the ones thereafter if PROPB1ERR remains high. This calculated $B1_{STS\text{-}12\#1}$ is XORed with the error-mask derived from XORing the extracted $B1_{STS\text{-}48}$ with the calculated $B1_{STS\text{-}48}$ over the entire STM-16/STS-48 frame. The result is inserted into the B1 byte position of the outgoing STM-4/STS-12 data stream RXOUTA[7:0]. This will make the B1 error count on the B1ERR output identical to the B1 error count in the first PM5312.

The VSC8024 can also receive byte-wide STM-16/STS-48 data from a STM-64/STS-192 Demux Circuit (or for loopback purposes from the VSC8023 byte-wide STM-16/STS-48 output) on the RXPIN[7:0] data bus. When SELPARIN is asserted high, the 1:8 Demux and the frame recovery circuit are bypassed. An external frame pulse aligned with the first payload byte in every frame has to be provided on the RXFPIN input. Data on RXPIN[7:0] and on RXFPIN is clocked into the VSC8024 on the rising edge of RXPCLKIN.

Figure 6: VSC8024 Functional Timing Diagram

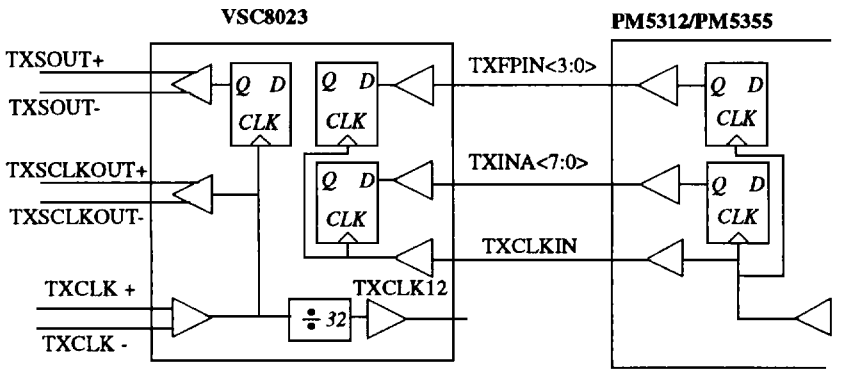


Notes:

(1) The correct latency between the RXSIN data-stream input and the RXOUT data-stream outputs is NOT shown.

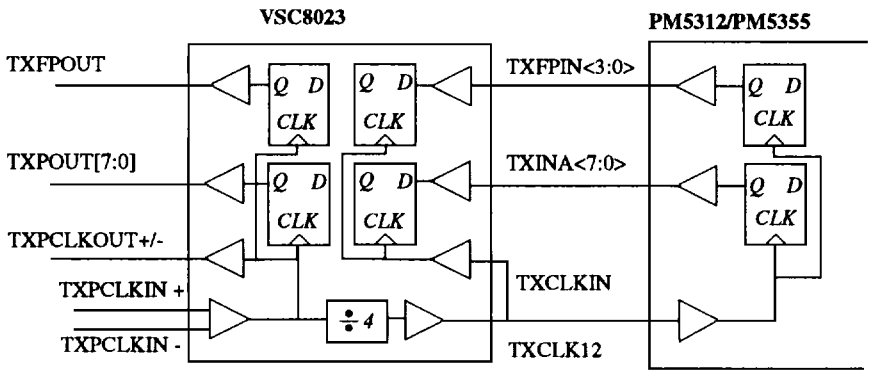
VSC8023 AC Timing Characteristics

Figure 7: VSC8023 Data and Clock Block Diagram (Serial Transmit & Co-directional Mode)



Note: TXINB<7:0>, TXINC<7:0>, and TXIND<7:0> inputs have been omitted for simplicity.

Figure 8: VSC8023 Data and Clock Block Diagram (Parallel Transmit & Contra-directional Mode)



Note: TXINB<7:0>, TXINC<7:0>, and TXIND<7:0> inputs have been omitted for simplicity.

Figure 9: VSC8023 Data Input Timing Diagram

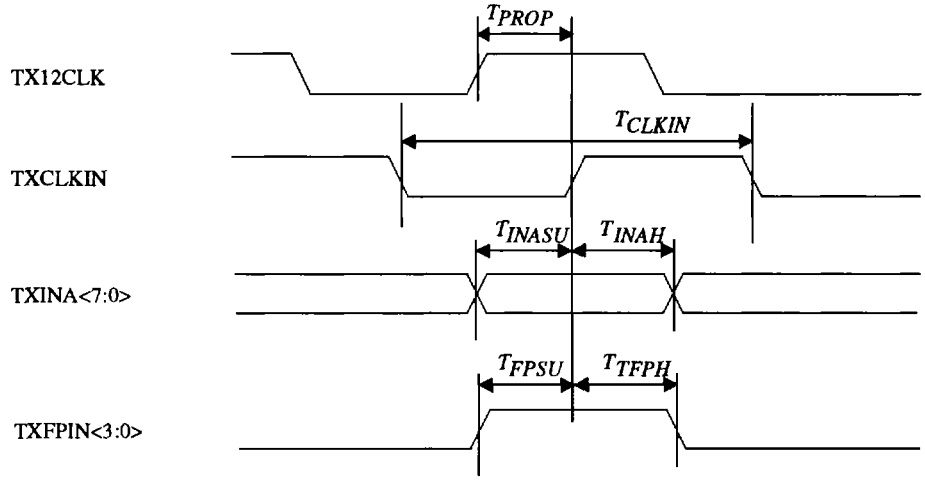
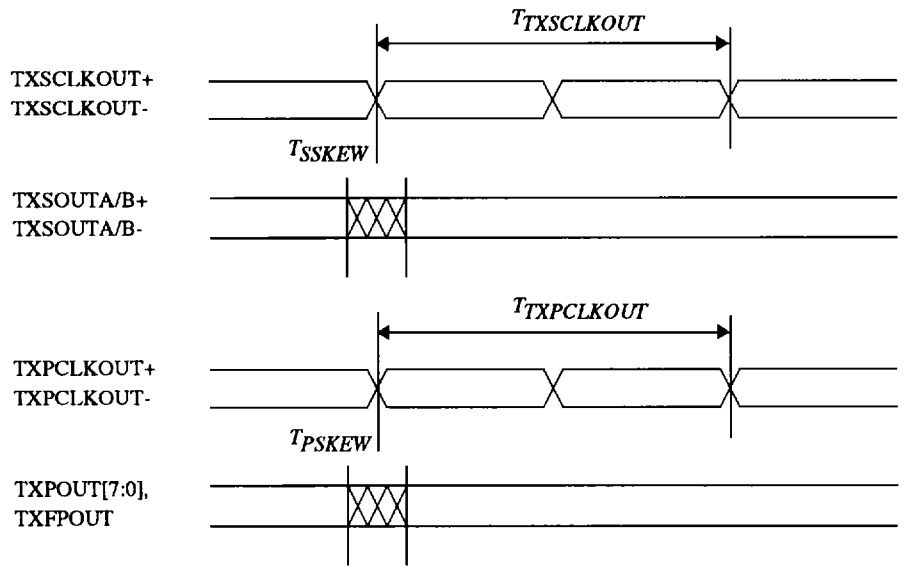


Table 3: VSC8023 Data Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{TXCLK}	VSC8023 high-speed input clock period		401.9		ps
$T_{TXCLKIN}$	Transmit data input byte clock period	-	12.86	-	ns
$D_{TXCLKIN}$	Transmit data input byte clock duty cycle	TBD	50	TBD	%
T_{INASU}	TXINA<7:0> data setup time with respect to TXCLKIN	TBD	-	-	ns
T_{INAH}	TXINA<7:0> data hold time with respect to TXCLKIN	TBD	-	-	ns
T_{INBSU}	TXINB<7:0> data setup time with respect to TXCLKIN	TBD	-	-	ns
T_{INBH}	TXINB<7:0> data hold time with respect to TXCLKIN	TBD	-	-	ns
T_{INCSU}	TXINC<7:0> data setup time with respect to TXCLKIN	TBD	-	-	ns
T_{INCH}	TXINC<7:0> data hold time with respect to TXCLKIN	TBD	-	-	ns
T_{INDSU}	TXIND<7:0> data setup time with respect to TXCLKIN	TBD	-	-	ns
T_{INDH}	TXIND<7:0> data hold time with respect to TXCLKIN	TBD	-	-	ns
T_{FPSU}	TXFPIN<3:0> data setup time with respect to TXCLKIN	TBD	-	-	ns
T_{FPAH}	TXFPIN<3:0> data hold time with respect to TXCLKIN	TBD	-	-	ns
T_{PROP}	Maximum allowable propagation delay for connecting TX12CLK to TXCLKIN	-	-	TBD	ns

Figure 10: VSC8023 Serial and Parallel Data Output Timing Diagram



Note: TXSCLKOUT and TXPCLKOUT have not been drawn to scale.

Table 4: VSC8023 Serial and Parallel Data Output Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{TXSCLKOUT}$	Serial Transmit clock period	-	401.9	-	ps
T_{SSKEW}	Skew between the falling edge of TXSCLKOUT and valid data on TXSOUTA/B	-	-	TBD	ps
$T_{TXPCLKOUT}$	Parallel Transmit clock period	-	3.215	-	ns
T_{PSKEW}	Skew between the falling edge of TXPCLKOUT and valid data on TXPPOUT[7:0] and on TXFPOUT	-	-	TBD	ps

Note: Duty cycle for TXSCLKOUT and for TXPCLKOUT is 50% +/- 5% worse case.

Figure 11: VSC8023 Facility Loopback Input Timing Diagram

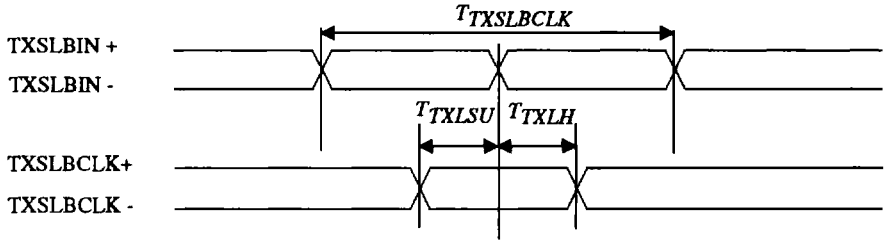


Table 5: VSC8023 Facility Loopback Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{TXSLBCLK}$	Serial loopback clock period	-	401.9	-	ps
T_{TXLSU}	Serial loopback input data setup time with respect to rising edge of TXSLBCLK+	TBD	-	-	ps
T_{TXLSH}	Serial loopback input data hold time with respect to rising edge of TXSLBCLK+	TBD	-	-	ps

VSC8024 AC Timing Characteristics

Figure 12: VSC8024 Data and Clock Block Diagram (Serial Receive Mode)

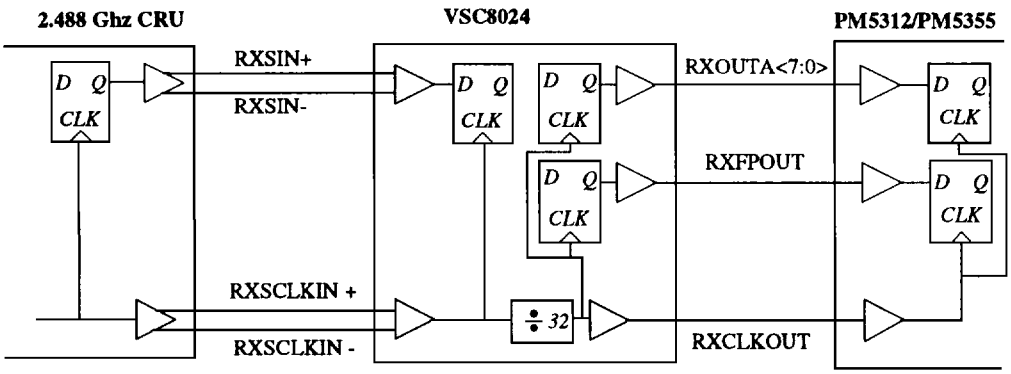


Figure 13: VSC8024 Data and Clock Block Diagram (Parallel Receive Mode)

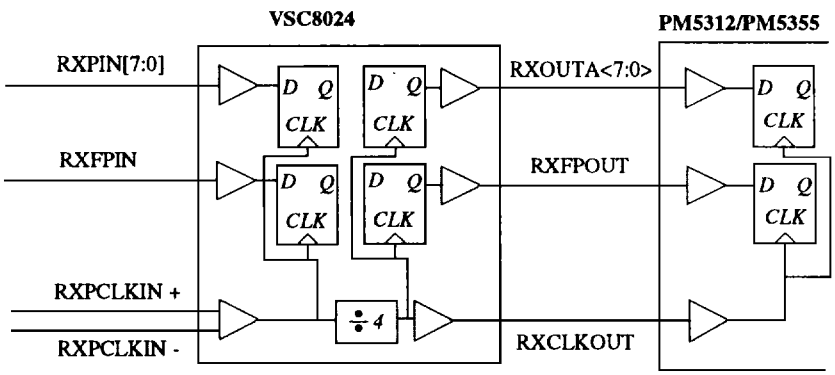
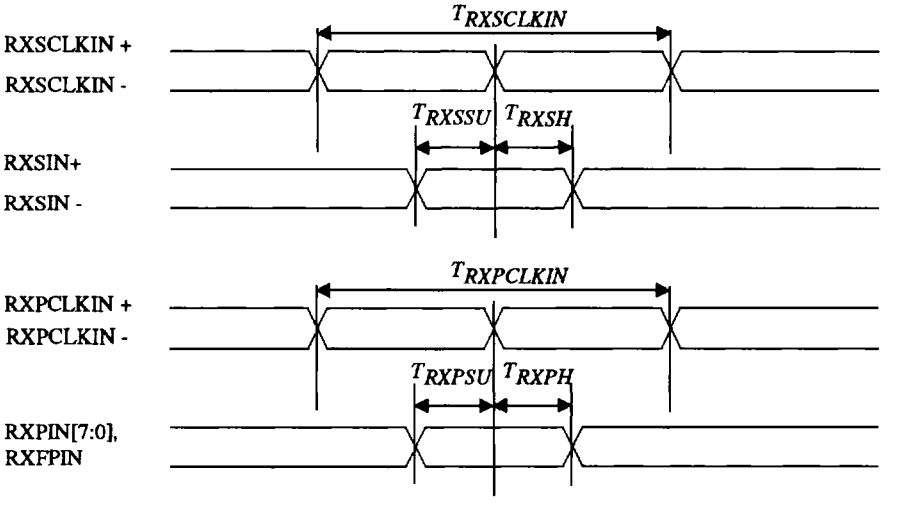


Figure 14: VSC8024 Serial and Parallel Data Input Timing Diagram

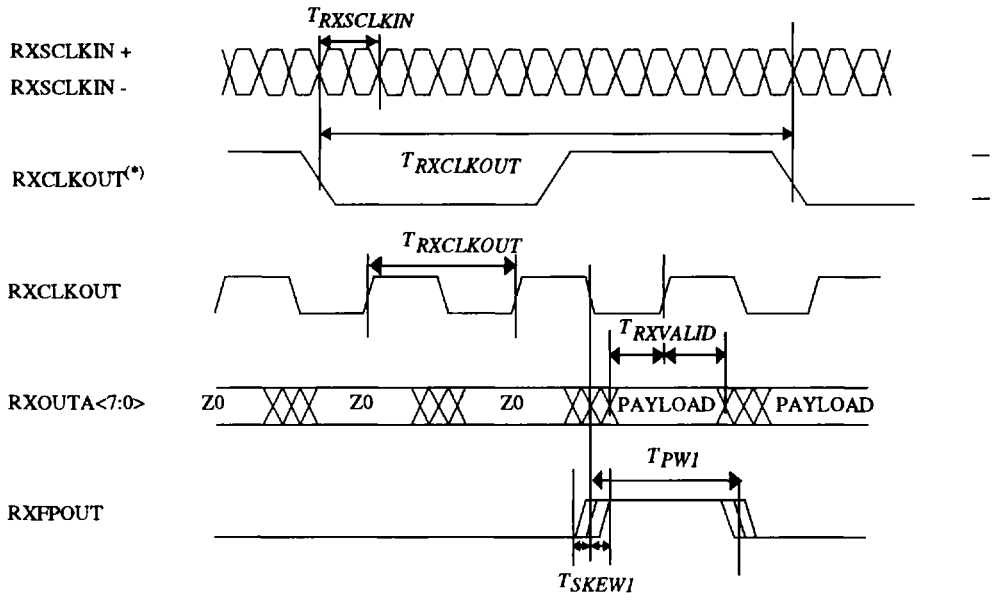


Note: RXSCLKIN and RXPCLKIN have not been drawn to scale.

Table 6: VSC8024 Serial and Parallel Data Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXSCLKIN}$	Serial Receive clock period	-	401.9	-	ps
T_{RXSSU}	Serial Receive input data setup time with respect to rising edge of RXSCLKIN+	TBD	-	-	ps
T_{RXSH}	Serial Receive input data hold time with respect to rising edge of RXSCLKIN+	TBD	-	-	ps
$T_{RXPCLKIN}$	Parallel Receive clock period	-	3.215	-	ns
T_{RXPSU}	Parallel Receive input data setup time with respect to rising edge of RXPCLKIN+	TBD	-	-	ns
T_{RXPH}	Parallel Receive input data hold time with respect to rising edge of RXPCLKIN+	TBD	-	-	ns

Figure 15: VSC8024 Data Output Timing Diagram

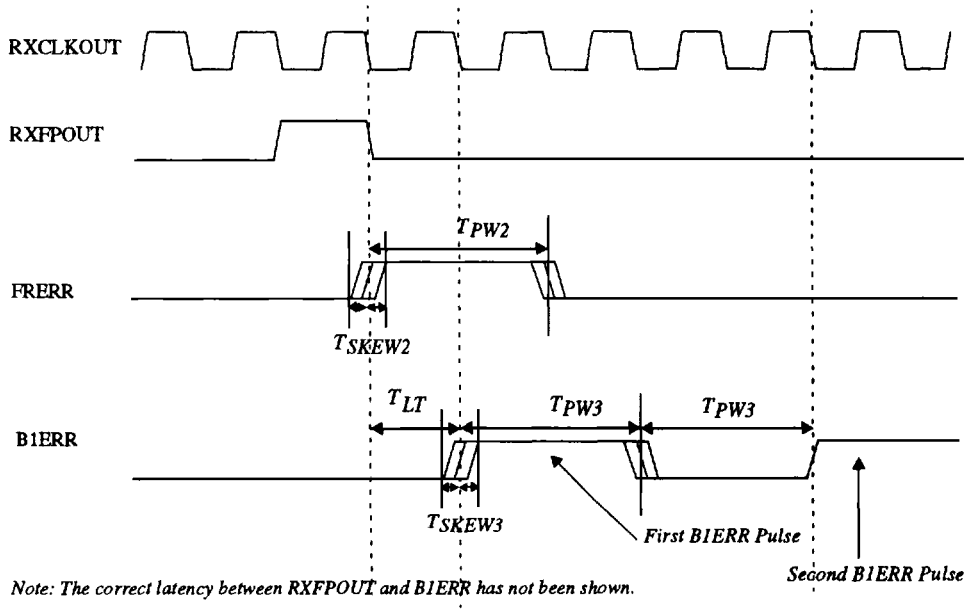


Note: RXSCLKIN and RXCLKOUT(*) have not been drawn to scale compared to the signals below them.

Table 7: VSC8024 Data Output Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXSCLKIN}$	Serial Receive clock period	-	401.9	-	ps
$T_{RXCLKOUT}$	Receive data output byte clock period	-	12.86	-	ns
T_{SKEW1}	Range in which the rising edge of RXFPOUT will appear in relation to the falling edge of RXCLKOUT	-	-	TBD	ns
$T_{RXVALID}$	Time data on RXOUTA<7:0>, RXOUTB<7:0>, RXOUTC<7:0> and RXOUTD<7:0> is valid before and after the rising edge of RXCLKOUT	TBD	-	-	ns
T_{PW1}	Pulse width of frame detection pulse RXFPOUT	-	12.86	-	ns

Figure 16: VSC8024 Error Data Output Timing Diagram



Note: The correct latency between RXFPOUT and B1ERR has not been shown.

Table 8: VSC8024 Error Data Output Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{SKEW2}	Range in which the rising edge of FRERR will appear in relation to the falling edge of RXCLKOUT	-	-	TBD	ns
T_{PW2}	Pulse width of frame error pulse FRERR	-	25.72	-	ns
T_{LT}	Latency between the rising edge of RXFPOUT and the rising edge of a B1ERR pulse	13.82	-	14.00	µs
T_{SKEW3}	Range in which the rising edge on B1ERR will appear in relation to the falling edge of RXCLKOUT	-	-	TBD	ns
T_{PW3}	Pulse width of B1 error pulse B1ERR	-	25.72	-	ns

Figure 17: VSC8024 Facility Loopback Output Timing Diagram

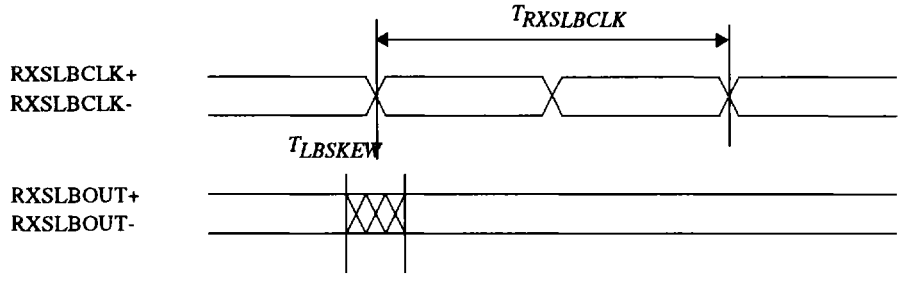


Table 9: VSC8024 Facility Loopback Output Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXSLBCLK}$	Serial loopback clock period	-	401.9	-	ps
T_{LBSKEW}	Skew between the falling edge of RXSLBCLK and valid data on RXSLBOUT	-	-	TBD	ps

Absolute Maximum Ratings(1)

Power Supply Voltage (V_{TT}) Potential to GND ..... -2.5 V to +0.5 V
Power Supply Voltage (V_{TTL}) Potential to GND ..... -0.5 V to +4.3 V
TTL Input Voltage Applied ..... -0.5 V to + 5.5V
ECL Input Voltage Applied ..... +0.5 V to V_{TT} -0.5 V
Output Current (I_{OUT}) ..... 50 mA
Case Temperature Under Bias (T_C) ..... -55° to + 125°C
Storage Temperature (T_{STG}) ..... -65° to + 150°C

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{TT}) ..... -2.0 V±5 %
Power Supply Voltage (V_{TTL}) ..... +3.3 V±5 %
Commercial Operating Temperature Range* (T) ..... 0° to 70°C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8023 and VSC8024 are rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

DC Characteristics

Table 10: ECL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-	-700	mV	50 ohm to V_{TT}
V_{OL}	Output LOW voltage	-2000	-	-1620	mV	50 ohm to V_{TT}
V_{IH}	Input HIGH voltage	-1165	-	-700	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	-2000	-	-1475	mV	Guaranteed LOW signal for all inputs
I_{IH}	Input HIGH current	-	-	200	uA	$V_{IN}=V_{IH}$ (max)
I_{IL}	Input LOW current	-50	-	-	uA	$V_{IN}=V_{IL}$ (min)
V_{DIFF}	Input Voltage Differential	200	-	-	mV	
V_{CM}	Common Mode Voltage	-1.5	-	-0.5	V	

Note: Differential ECL output pins must be terminated identically.

Table 11: High-Speed Differential ECL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OD}	Output differential voltage	450	-	800	mV	
V_{OCM}	Output common-mode voltage	-1600	-	-1200	mV	
R_O	Output Impedance	3	-	7	ohms	Guaranteed, not tested.
V_{ID}	Input differential voltage	200	-		mV	
V_{ICM}	Input common-mode voltage	-1.5	-	-0.5	V	
V_{IT}	Input threshold matching	-25	-	25	mV	
V_{DIFF}	Input Voltage Differential	200	-	-	mV	
R_{IN}	Input resistance	40	-	60	ohms	

Table 12: TTL Inputs and Outputs

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	2.4	-	-	V	$V_{IN} = V_{IH}$ (max) or V_{IL} (min) I_{OH}=-2.4 mA
V_{OL}	Output LOW voltage	0	-	0.4	V	$V_{IN} = V_{IH}$ (max) or V_{IL} (min) I_{OL}=16 mA
V_{IH}	Input HIGH voltage	2.0	-	5.5	V	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	0	-	0.8	V	Guaranteed LOW signal for all inputs
I_{IH}	Input HIGH current	-	-	50	uA	$V_{IN}=V_{IH}$ (max)
I_{IL}	Input LOW current	-500	-	-	uA	$V_{IN}=V_{IL}$ (min)
I_{OZH}	3-State Output OFF current HIGH	-	-	200	uA	V_{OUT}=2.4 V
I_{OZL}	3-State Output OFF current LOW	-200	-	-	uA	V_{OUT}=0.5 V

Power Dissipation

Table 13: VSC8023 Power Supply Currents

Parameter	*Description*	*(Max)*	*Units*
I_{TT}	Power supply current from V_{TT}	TBD	mA
I_{TTL}	Power supply current from V_{TTL}	TBD	mA
P_D	Power dissipation	TBD	W

Note: Specified with outputs open circuit. The combined maximum currents (I_{TT} I_{TTL}) for any part will not exceed TBD Watts.

Table 14: VSC8024 Power Supply Currents

Parameter	*Description*	*(Max)*	*Units*
I_{TT}	Power supply current from V_{TT}	TBD	mA
I_{TTL}	Power supply current from V_{TTL}	TBD	mA
P_D	Power dissipation	TBD	W

Note: Specified with outputs open circuit. The combined maximum currents (I_{TT} I_{TTL}) for any part will not exceed TBD Watts.

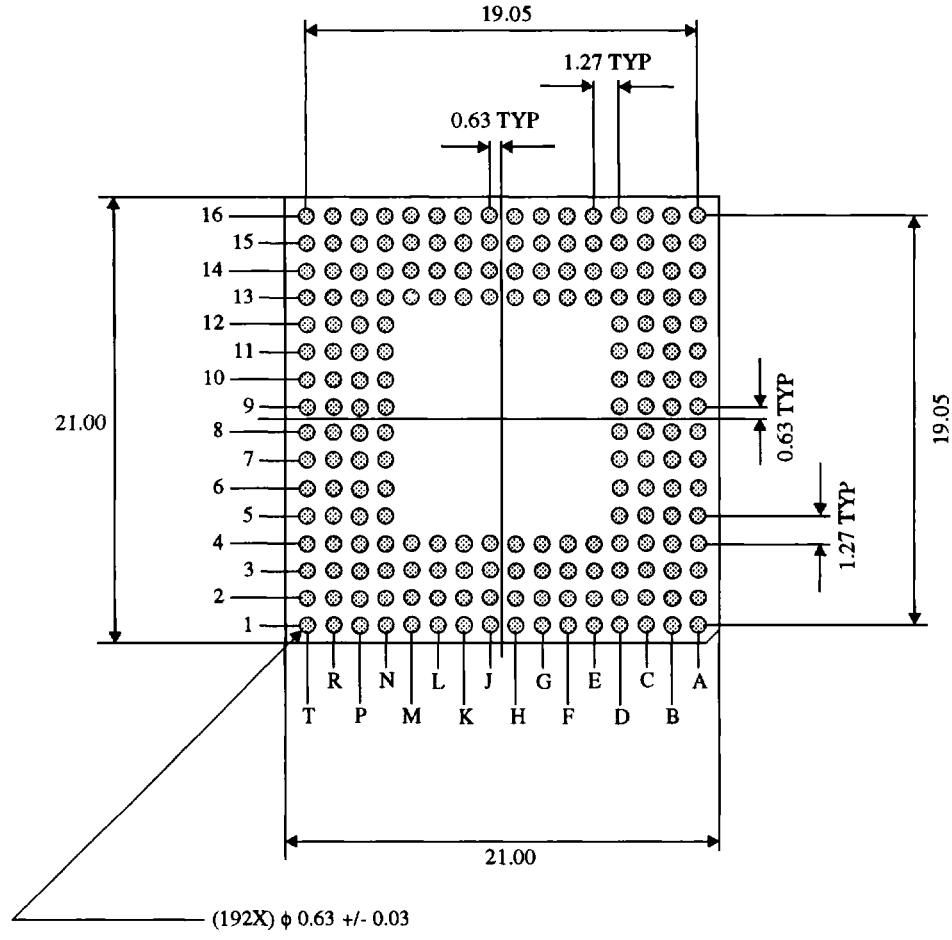
VSC8023 Package Pin Description

Table 15: TBD

VSC8024 Package Pin Description

Table 16: TBD

Figure 18: 192TBGA Package Drawing (Bottom View)



Notes:
(1) Drawings not to scale.
(2) All units in millimeters.

Application Notes

The byte clock (TXCLK12 and TXCLKIN) on the VSC8023 has been brought off-chip to allow as much flexibility in system-level clocking schemes as possible. Refer to figures 7 & 8 for connection examples.

Interconnecting the VSC8023 Byte Clocks (TXCLK12 and TXCLKIN)

Contra-Directional Connection:

In this mode, the byte clock (TXCLK12) clocks both the VSC8023 and the PMC devices. It is important to pay close attention to the routing of this signal. The PMC devices are CMOS parts which can have very wide spreads in timing (1 ns-11 ns clock in to parallel data out for the PM5355) which utilizes most of the 12.86 ns period (at 77.76 MHz), leaving little for the trace delays and set-up times required to interconnect the devices. The recommended way of routing this clock is to daisy chain it to the PMC device pins and then route it back to the VSC8023 along with the byte data. This eliminates the 1-way trace delay that would otherwise be encountered between the data and clock and thus leaves 1.86 ns for the VSC8023 setup time and for variations in trace delays and rise times between clock and data. The trace delay must be kept under 2 ns (allowing an additional 1 ns for variations in rise times and skews) to ensure proper muxing of parallel input data into the VSC8023; reference Table 2.

Co-Directional Connection:

In the co-directional mode an internal data synchronizing circuit is used to optimize the phase relationship between a supplied TXCLKIN and internal clocks. The TXCLKIN signal needs only to meet setup and hold timing relative to the data stream and frame pulses.

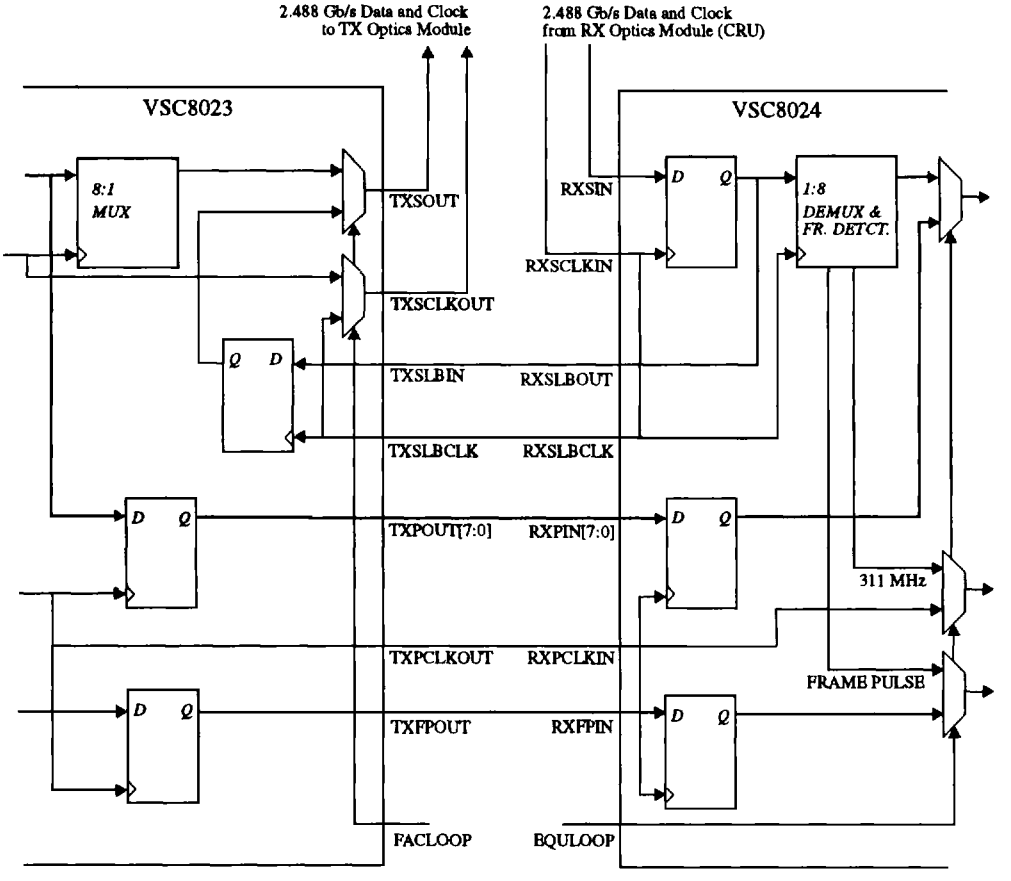
Equipment and Facility Loopbacks

In order to create an Equipment Loopback, the EQULOOP VSC8024 input is held high. The byte-wide STM-16/STS-48 data on the VSC8023 TXPOUT[7:0] outputs is clocked into the VSC8024 RXPIN[7:0] inputs with the TXPCLKOUT clock. A frame pulse aligned with the first payload byte on the TXPOUT[7:0] databus is provided to assure proper alignment. Both the Facility and the Equipment Loopbacks can be enabled simultaneously. It is possible to disable (hold at a logic low) the serial high-speed outputs on the VSC8024 by holding the DISLBOUTS input high.

Equipment and Facility Loopbacks

The diagram below (Figure 19) shows how an Equipment and a Facility Loopback are created. When in Facility Loopback mode (FACLOOP is held high) the serial 2.488 Gb/s data and clock from the RX optics module is first clocked into the VSC8024 and then fed back into the VSC8023 through TXSLBIN and TXSLBCLK. The FACLOOP input (held high) selects the data from the VSC8024 instead of the data from the 8:1 Mux. The result is a line loopback from the RX optics module back out to the TX optics module.

Figure 19: Serial Loopback Mode Block Diagram



Notes:
(1) All signals drawn as single ended instead of differential.
(2) Disable High-Speed VSC8024 Outputs Control Signal DISLBOUTS NOT shown.

Preliminary Datasheet

2.488 Gbits/sec SDH/SONET STM-16/STS-48 Mux/Demux and Section Terminator IC Chipset

Notice

This document contains information on products that are in the preproduction phase of development. The information contained in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing orders.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.