

### 1.1 Scope.

This specification covers the detail requirements for a 12-bit resolution A/D converter with complete microprocessor interface and a high performance buried Zener reference.

### 1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number <sup>1</sup>
-1	AD574AS(X)/883B
-2	AD574AT(X)/883B
-3	AD574AU(X)/883B

#### NOTE

<sup>1</sup>See paragraph 1.2.3 for package identifier.

### 1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin DIP
E	E-28A	28-Pin LCC

### 1.3 Absolute Maximum Ratings. ( $T_A = +25^\circ\text{C}$ unless otherwise noted)

$V_{CC}$ to Digital Common . . . . .	+ 16.5V
$V_{EE}$ to Digital Common . . . . .	- 16.5V
$V_{LOGIC}$ to Digital Common . . . . .	+ 7V
Analog Common to Digital Common . . . . .	$\pm 1V$
Control Inputs ( $\overline{CE}$ , $\overline{CS}$ , $A_0$ , $12/\overline{8}$ , $R/\overline{C}$ ) to Digital Common . . . . .	- 0.5V to $V_{LOGIC} + 0.5V$
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$ ) to Analog Common . . . . .	$\pm 16.5V$
$20V_{IN}$ to Analog Common . . . . .	$\pm 24V$
REF OUT . . . . .	Indefinite Short to Common Momentary Short to $V_{CC}$
Power Dissipation . . . . .	1000mW
Storage Temperature Range . . . . .	- 65°C to + 150°C
Lead Temperature (Soldering 10sec) . . . . .	+ 300°C

### 1.5 Thermal Characteristics.

Thermal Resistance  $\theta_{JC} = 25^\circ\text{C}/\text{W}$  for D-28 or E-28A  
 $\theta_{JA} = 60^\circ\text{C}/\text{W}$  for D-28 or E-28A

# AD574A—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition <sup>1</sup>	Units
Power Dissipation	P <sub>D</sub>	-1, 2, 3	725	725			Tristated Outputs	mW max
Input Resistance	R <sub>IN</sub>	-1, 2, 3	3	3			10V Span	kΩ min
			7	7				kΩ max
			6	6			20V Span	kΩ min
			14	14				kΩ max
Internal 10V Reference Output Voltage Error	V <sub>REF</sub>	-1, 2	± 20	± 20			Bipolar 1.5mA External Load	mV
		-3	± 10	± 20		± 10		
Logic Input High <sup>2</sup> CE, $\overline{CS}$ , R/ $\overline{C}$ , A <sub>O</sub>	V <sub>IH</sub>	-1, 2, 3	2.0	2.0				+ V min
			5.5					+ V max
Logic Input Low <sup>2</sup> CE, $\overline{CS}$ , R/ $\overline{C}$ , A <sub>O</sub>	V <sub>IL</sub>	-1, 2, 3	0.5					- V min
			0.8	0.8				+ V max
Logic Input Current CE, $\overline{CS}$ , R/ $\overline{C}$ , A <sub>O</sub>	I <sub>LIN</sub>	-1, 2, 3	20	20	20		V <sub>IH</sub> = 5.0V V <sub>IL</sub> = 0.0V	± μA max
Logic Output High DB11-DB0	V <sub>OH</sub>	-1, 2, 3	2.4	2.4	2.4		I <sub>SOURCE</sub> = 500μA	+ V min
Logic Output Low DB11-DB0, STS	V <sub>OL</sub>	-1, 2, 3	0.4	0.4	0.4		I <sub>SINK</sub> = 1.6mA	+ V max
Three-State Output Leakage DB11-DB0	I <sub>OLT</sub>	-1, 2, 3	20	20	20		Outputs Tristated V <sub>IH</sub> = 5.0V	± μA max
Power Supply Current	I <sub>L</sub> I <sub>CC</sub> I <sub>EE</sub>	-1, 2, 3	40	40			Outputs Tristated	mA max
		-1, 2, 3	5	5				
		-1, 2, 3	30	30				
Full-Scale Calibration Drift	TCA <sub>E</sub>	-1			20			± LSB max
		-2			10			
		-3			5			
Linearity	LE	-1	1	1	1		10V Unipolar, 20V Bipolar Major Transitions	± LSB max
		-2, 3	1/2	1	1	1/2		
Differential Nonlinearity <sup>3</sup>	DNL	-1	11	11	11		All Codes Tested	Bits min
		-2, 3	12	11	12	12		
Power Supply Rejection Ratio <sup>4</sup>	PSRR	-1	2	2			See Note 5	± LSB max
		-2, 3	1	2		1		
	PSRR	-1, 2, 3	1/2	1/2			See Note 6	
	PSRR	-1	2	2			See Note 7	
		-2, 3	1	2		1		
Unipolar Offset Error	V <sub>OSE</sub>	-1	2	2	4			± LSB max
		-2, 3	1	2	2	1		
Unipolar Offset Drift	TC <sub>VOS</sub>	-1 -2, 3			2 1			± LSB max
Bipolar Offset Error	B <sub>POE</sub>	-1	4	4	8		Bipolar 20V Span	± LSB max
		-2	4	4	6			
		-3	2	4	3	2		
Bipolar Offset Drift	TCB <sub>POE</sub>	-1			4		Bipolar 20V Span	± LSB max
		-2			2			
		-3			1			
Full-Scale Error	A <sub>B</sub>	-1, 2	0.25	0.25			Bipolar 20V Span	± %/FSR max
		-3	0.125	0.25		0.125		
	A <sub>U</sub>	-1, 2	0.25				Unipolar 10V Span	± %/FSR max
		-3	0.125					

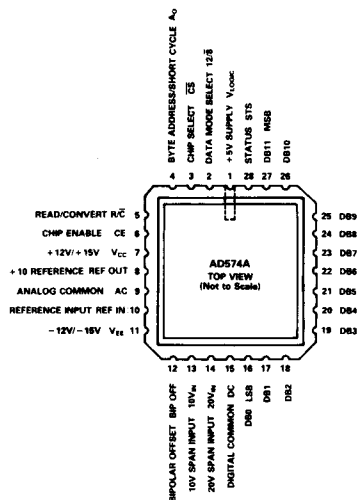
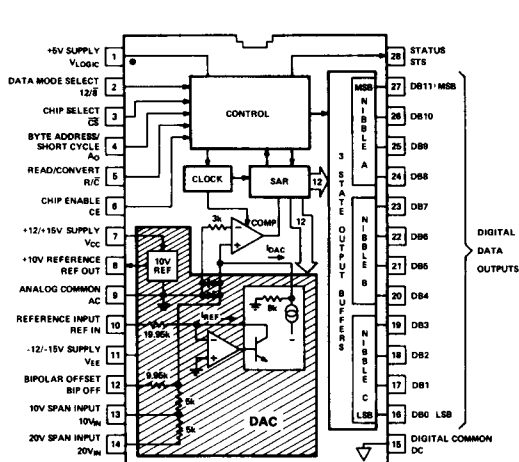
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Test Condition <sup>1</sup>	Units
<b>Full-Control Mode<sup>1</sup></b>								
STS Delay from CE	$t_{DSC}$	- 1, 2, 3	400			350	Timing Per Figure 1	ns max
CE Pulse Width	$t_{HEC}$	- 1, 2, 3	300			300	Timing Per Figure 1	ns min
Access Timing (from CE) <sup>8</sup>	$t_{DD}$	- 1, 2, 3	200			200	Timing Per Figure 2	ns max
Output Float Delay	$t_{HL}$	- 1, 2, 3	100			100	Timing Per Figure 2	ns max
Data Valid After CE Low	$t_{HD}$	- 1, 2, 3	25			25	Timing Per Figure 2	ns min
<b>Stand-Alone Mode<sup>1</sup></b>								
Low R/C Pulse Width	$t_{HRL}$	- 1, 2, 3	250			250	Timing Per Figure 3	ns min
STS Delay from R/C	$t_{DS}$	- 1, 2, 3	600			600	Timing Per Figure 3	ns max
Data Access Time <sup>8</sup>	$t_{DDR}$	- 1, 2, 3	250			250	Timing Per Figure 3	ns max
Data Valid After R/C Low	$t_{HDR}$	- 1, 2, 3	25			25	Timing Per Figure 3	ns min
Conversion Time	$t_C$	- 1, 2, 3	35			35	To 12 Bits	$\mu s$ max
			24			24	To 8 Bit	

- NOTES**
- $V_{CC} = +15V$ ,  $V_{EE} = -15V$ ,  $V_{LOGIC} = +5V$ ,  $12/\bar{8}$  connected to  $V_{LOGIC}$ ,  $A_0$  and  $\overline{CS}$  at logic "0", CE at logic "1." 10V unipolar configuration unless otherwise noted. 10V Unipolar: 50 $\Omega$  resistor Pin 8 to Pin 10, 50 $\Omega$  resistor Pin 12 to ground, analog input to Pin 13.
  - 20V Bipolar: 50 $\Omega$  resistor Pin 8 to Pin 12, 50 $\Omega$  resistor Pin 8 to Pin 10, analog input to Pin 14.
  - See Figures 1, 2, and 3 for timing information.
  - $V_{IH} = 2.0V$  min and  $V_{IL} = 0.8V$  max, guaranteed design limits  $-55^\circ C$  to  $+125^\circ C$ .
  - Minimum resolution for which no missing codes are guaranteed.
  - Change in unipolar 10V span with full-scale (Code 4095) transition voltage.
  - Test Conditions for PSRR:
    - $13.5V \leq V_{CC} \leq 16.5V$ ,  $V_{LOGIC} = 5V$ ,  $V_{EE} = -15V$
    - $11.4V \leq V_{CC} \leq 12.6V$ ,  $V_{LOGIC} = 5V$ ,  $V_{EE} = -12V$
    - $4.5V \leq V_{LOGIC} \leq 5.5V$ ,  $V_{CC} = 15V$ ,  $V_{EE} = -15V$
  - $-16.5 \leq V_{EE} \leq -13.5V$ ,  $V_{LOGIC} = 5V$ ,  $V_{CC} = 15V$
  - $-12.6V \leq V_{EE} \leq -11.4V$ ,  $V_{LOGIC} = 5V$ ,  $V_{CC} = 12V$
  - See Figure 4.

### 3.2.1 Functional Block Diagram and Terminal Assignments.

**D Package (DIP)**

**E Package (LCC)**



# AD574A

## 3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

### 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

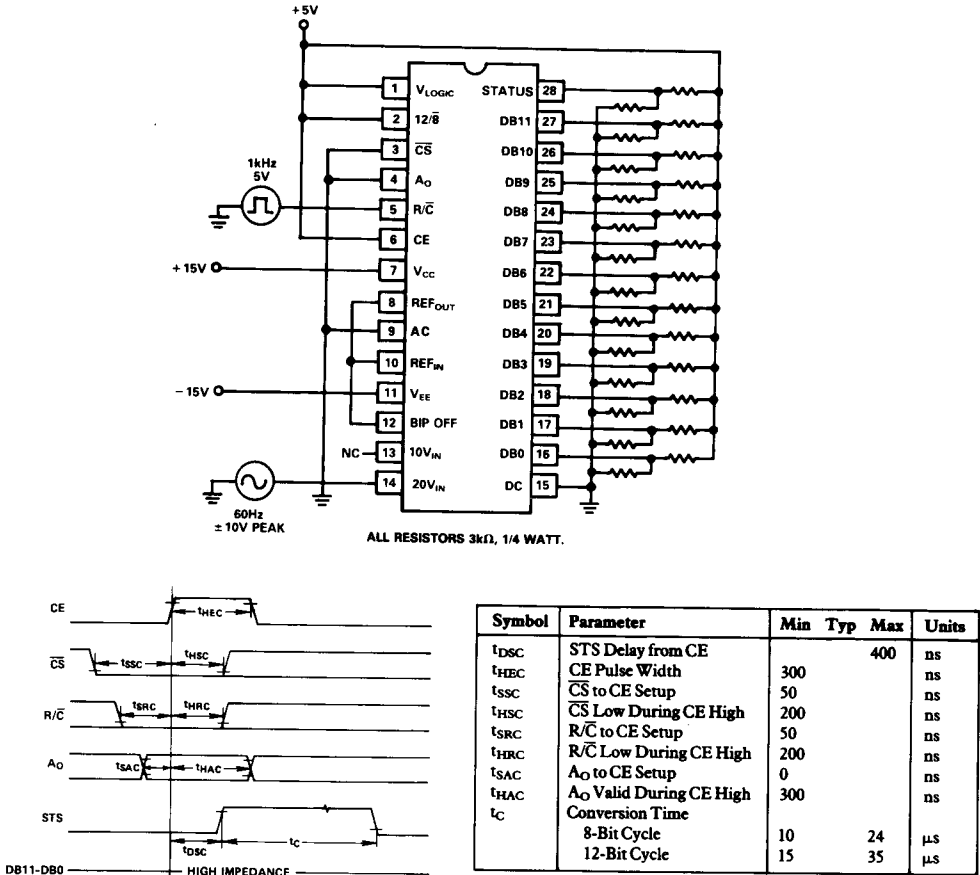
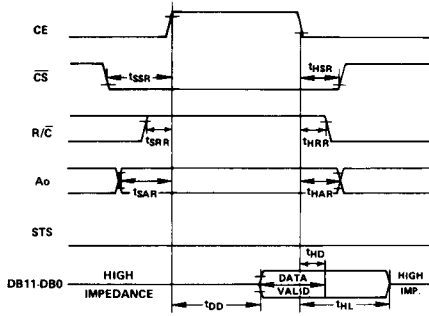


Figure 1. Convert Start Timing

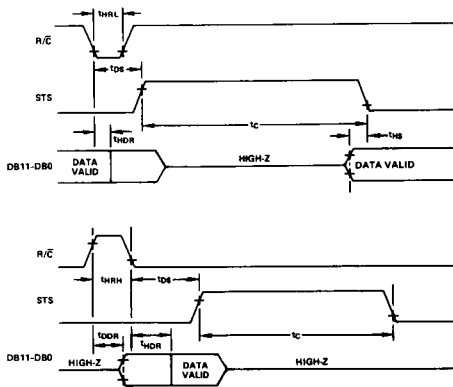


Symbol	Parameter	Min	Typ	Max	Units
$t_{DD}^1$	Access Time (from CE)		200		ns
$t_{HD}$	Data Valid after CE Low	25			ns
$t_{HL}^2$	Output Float Delay		100		ns
$t_{SSR}$	$\overline{CS}$ to CE Setup	150			ns
$t_{SRR}$	R/C to CE Setup	0			ns
$t_{SAR}$	$A_0$ to CE Setup	150			ns
$t_{HSR}$	$\overline{CS}$ Valid After CE Low	50			ns
$t_{HRL}$	R/C High After CE Low	0			ns
$t_{HAR}$	$A_0$ Valid After CE Low	50			ns

<sup>1</sup> $t_{DD}$  is measured with the load circuit of Figure 4 and defined as the time required for an output to cross 0.4V to 2.4V.

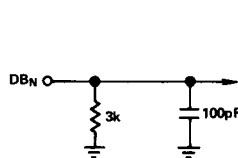
<sup>2</sup> $t_{HL}$  is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 5.

Figure 2. Read Timing

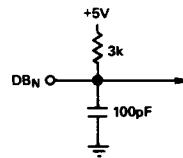


Symbol	Parameter	Min	Typ	Max	Units
$t_{HRL}$	Low R/C Pulse Width	250			ns
$t_{DS}$	STS Delay from R/C		600		ns
$t_{HDR}$	Data Valid After R/C Low	25			ns
$t_{HS}$	STS Delay After Data Valid	300	1000		ns
$t_{HRH}$	High R/C Pulse Width	300			ns
$t_{DDR}$	Data Access Time		250		ns

Figure 3. Stand-Alone Mode Timing

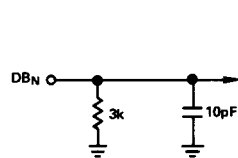


a. High-Z to Logic 1

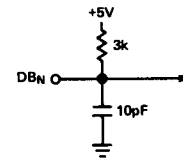


b. High-Z to Logic 0

Figure 4. Load Circuit for Access Timing Test



a. Logic 1 to High-Z



b. Logic 0 to High-Z

Figure 5. Load Circuit for Output Float Delay Test