AN3192-1.2 December 1991

MA805

FUNCTION AND TIMING INFORMATION

INTRODUCTION

Scope

This guide is intended to supplement the MA805 Data Sheet (DS3043-1) and explains only the standard 1553B functions.

Section 1	Describes INITIALISATION of the MA805 and the two modes of RESET HARD and SOFT.
Section 2	Describes the sequences that govern the transfer of data to and from the SUBSYSTEM; the concept of the STATUS MODIFIER word; the significance of GTB and the treatment of ERRORS. Timing diagrams for all control signals are provided.
Section 3	Details the set up and hold times required for all HIGHWAY words to and from the SUBSYSTEM.
Section 4	Gives the RESPONSE time of the MA805.
Section 5	Explains the effect of overriding commands and its effect on the handshake control signals. Also explains handshake operation.
Section 6	Explains access to MA805 registers.
Section 7	Describes the MA805's ability to read the BIT word from the SUBSYSTEM (EXTERNAL) and the interaction of other mode codes.
APPENDIX A	Provides a useful reference to 1553B formats and mode codes.
APPENDIX B	Example of Memory Map for the MA805.

PRINCIPLES OF OPERATION

The MA805 RT is INITIALISED under SUBSYSTEM control by reading the INITWORD from the HIGHWAY (H0: H 15). The RT address is contained in the INITWORD and is continually checked during operation for ODD parity. If this should ever be corrupted the MA805 will be forced into a RESET condition and wait for the SUBSYSTEM to provide the INITWORD. This is normally a 16 bit word but can be reduced if not all functions are required. It is also possible for the SUBSYSTEM to clear internal flags and registers without providing the INITWORD (SOFT-RESET).

All valid words are transferred to the SUBSYSTEM over a 16 BIT 3 STATE HIGHWAY (H0:H15), under SUBSYSTEM control using a hard wired HANDSHAKE protocol. All transfer sequences start with a control word (CONTWORD). This CONTWORD can be used to MAP the data to user memory.

All transfers are governed by fixed sequences which are under MA805 control. These are referred to as COMMAND OUT DATAOUT, DATAIN. This time structured control avoids the possibility of the SUBSYSTEM contravening 1553B protocol. During the COMMAND OUT sequence, the COMMAND word is tranferred to the SUBSYSTEM and the SUBSYSTEM must then provide a STATMOD word. This gives the SUBSYSTEM control over the ALLOWING of RESERVED mode codes or the setting of any bits in the STATUS word, e.g. ME. DATAOUT and DATAIN sequences control the transfer of DATAWORDS to and from the SUBSYSTEM.

Completion of ERROR free transfers between the terminal and subsystem are indicated by the pulsing of a dedicated pin (GTB). This signal is synchronised with the termination of HREQB.

The SUBSYSTEM has access to the internal registers: INITWORD, STATUS, BITWORD and LAST COMMAND, upon demand or automatically after every VALID command. This can provide valuable diagnostic information. This function is controlled by a dedicated pin (IRWB). For this register transfer GTB is not applicable and is therefore not pulsed.

The SUBSYSTEM can select the source of the BIT word to be from the SUBSYSTEM itself instead of from the MA805 internal register. This selection is made during INITIALISATION. Its function could be to interchange bit positions within the BIT word for system compatability with other vendors.

Finally, OWN transmissions from the MA805 to the 1553B bus are checked by a LOOPTEST, and transmissions greater than 33 words are terminated by operation of a timeout counter.

Throughout this document the convention used in naming signals is to use a B suffix to indicate active low signal, e.g. HACKB = Highway ACKnowledge. The absence of the suffix indicates an active high signal.

1. INITIALISATION + RESET

1. Power on Reset.
2. Mode Code Reset.
3. Subsystem Initiated Reset.
   (i) HARD (+ INITWORD)
   (ii) SOFT (NO INITWORD)

1.1 POWER ON RESET

Ref. FIG 1.1
Outputs HREQB
RESETB
Inputs HACKB
HO:H15 (INITWORD)
CK: CLOCK

Operation:
The MA805 powers up with HREQB=0 and RESETB = 0. The internal POR period T-POR must then elapse. The MA805 then reads the INITWORD once only after the SUBSYSTEM has driven HACKB = 0. The INITWORD is then checked for ODD parity in the RT ADDRESS field (ADDO: ADD4, PARITY). If this is not true then the cycle repeats after Time T-INIT (refer to table 1) has elapsed, (without the POR period T-POR), i.e., HREQB and RESETB are SET=0 by the MA805. The terminal is available to the Bus Controller only after time T-INIT has elapsed. The address is continually monitored for ODD parity. SOFT reset is NOT available at power up.

N.B. There is no timeout on the handshake for this sequence. The user is only limited by 1553B protocol that requires the RESET to be completed within 5mS.

1.2 MODE CODE RESET

Ref. FIG 1.2
Outputs HREQB
RESETB
Inputs HACKB
H0:H15 (INITWORD)

Operation:
Normal COMMAND servicing is first completed as indicated by GTB = O.

The RESET sequence is then started as for power up reset except the internal POR timer is not used.

TA = -55°C to 125°C VDD = 5V+10%, CL = 50pf and ITTL load.

Symbol	Definition	Limits			Units
		Min	Typ	Max	
T-POR	Power on Reset	40		100	us
T-RESET	Reset Cycle		1.2	1.5	us
T-INIT	805 held in initialised State		7.5	8.0	us
T-VAL	Initword valid on highway		1.2	1.5	ns
T-HK-VAL	Delay from HACKB to supplying valid initword	0		500	ns
T-RES-HRH	Delay from RESETB going inactive to HREQB going inactive			150	ns
T-RES-HRL	Delay from RESETB going active to H R EQB going active			150	ns
T-LATCH	Overlap to ensure 805 latches RESETB = 0	500			ns
T-HR-GT (Reset)	HREQB to GTB		24		us
T-GT-HR	GTB to HREQB		500		ns
T-HR	HREQB pulse width following MODE CODE Reset		500		ns

Table 1: AC Electrical Characteristics

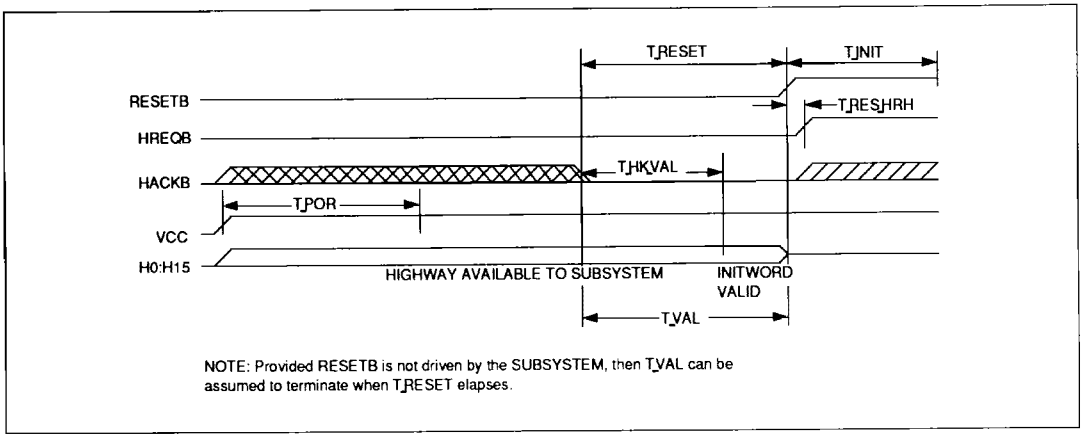


Figure 1.1: Power on Reset

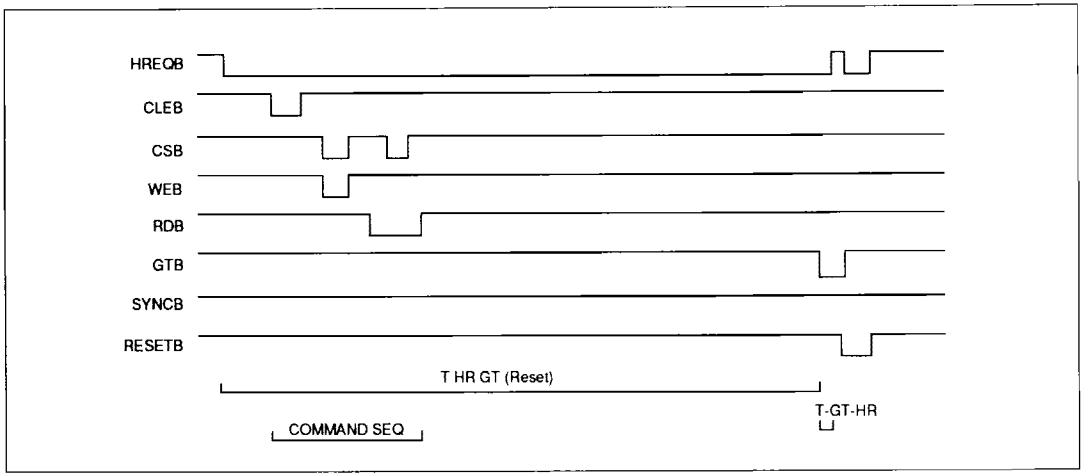


Figure 1.2a: Reset

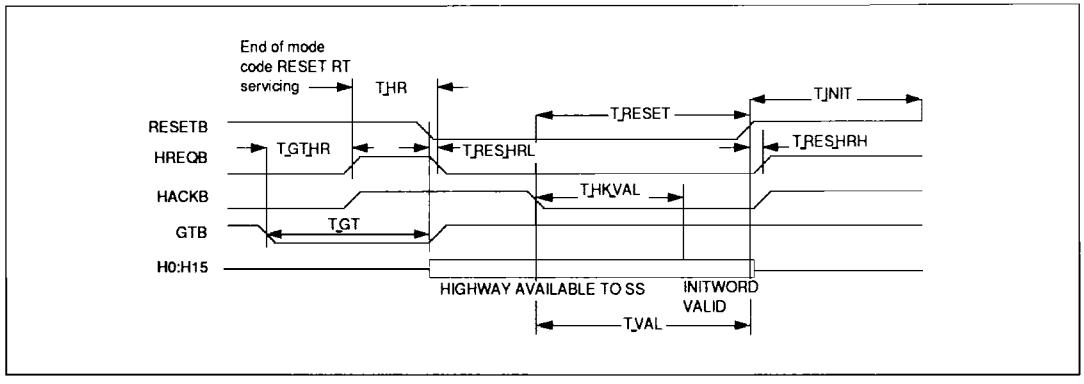


Figure 1.2b: Mode Code Reset (after Mode Code Reset RT servicing)

1.3 SUBSYSTEM INITIATED RESET

(i) With INIT Word (HARD RESET)
Ref. FIG 1.3
Outputs HREQB
RESETB
Inputs HACKB
RESETB
H0:H15 (INITWORD)

Operation:
At any time the SUBSYSTEM is able to force the MA805 RT into the RESET state by driving RESETB=0. The MA805 remains in this state until the SUBSYSTEM drives HACKB=0.

The MA805 will then latch the RESETB signal and itself drive RESETB =0 for a further time T-RESET. The MA805 will then read the INITWORD from the HIGHWAY (H0:H15).

HACKB must remain Set=0 until time T-RESET has elapsed.

(ii) Without INIT Word (SOFT RESET) The SUBSYSTEM is able to clear the internal registers (except INITWORD) and flags (e.g., TF, ME) by pulsing RESETB, minimum pulse width = 100ns, and driving HACKB=1.

The SUBSYSTEM does not set HACKB.

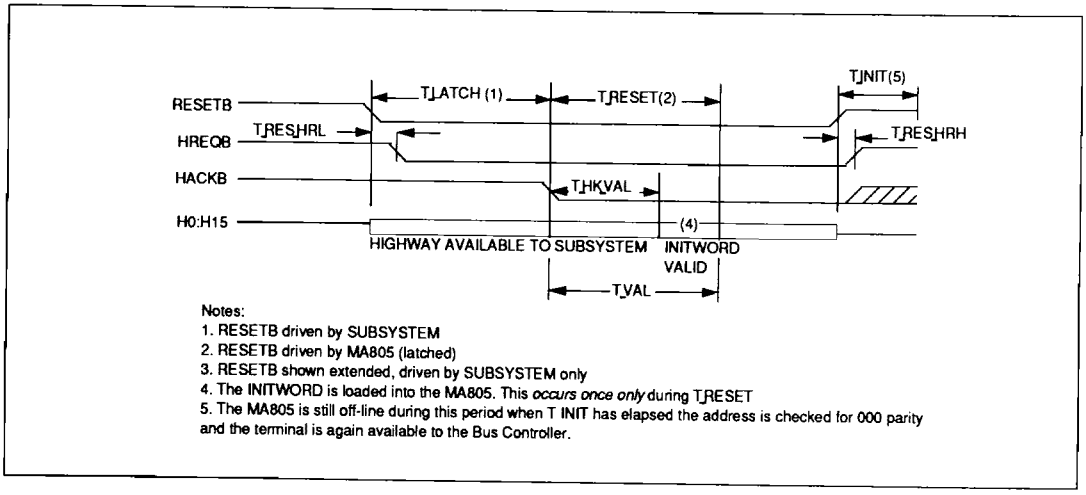


Figure 1.3: Subsystem Initiated Reset

SUBSYSTEM INTERFACE

2. SUBSYSTEM TRANSFERS

The 1553 bus messages are of the form shown in Appendix A. Figures 2.1 to 2.12 show examples of the subsystem waveforms in response to these messages and assume that HREQB and HACKB provide a normal handshake.

There is a direct relationship between the command word and data words of the 1553 bus message and subsystem sequences. The command word of the 1553 message causes the subsystem Command sequence (Figure 2.1). Data words of a Receive message give subsystem "Data Out" sequences (Figure 2.2). Data words of a transmit message cause subsystem "Data In" sequences (Figure 2.3).

Various errors (e.g Manchester encoding errors, handshake failure) cause the subsystem sequences to terminate immediately.

The format for the 1553 bus words are shown in Appendix A.

NB. The terminal will ignore messages that have any error in the command word.

Note that for transmit last status, and transmit last command mode codes there is no communication at all with the subsystem.

Subsystem Command Sequence (Figure 2.1)

The command sequence has three parts:
1) Control Word
2) Command Word
3) Status Modifier

1) The control word provides essential information about the message and is timed by CLEB. CLEB can be used to load external control latches with the control word. (See data sheet for the interpretation of individual bits). The latched word can then be used to control the addressing for the command sequence, or processing of the message by decoding the top 5 BITS of the control word.

2) The command word is then sent (CSB with WEB). This word is made available for the subsystem user to be able to take particular action for different commands if required.

3) The status modifier is requested from the subsystem. This adds flexibility and permits the subsystem to influence the status response of the remote terminal. The detail for each bit is given in the data sheet.

Note that SETMEB and SETBUSYB both shorten the message by preventing data transfers. When ALLOWB is inactive (i.e. the mode code is not being recognised by the MA805 or its subsystem) the associated data word transfer for reserved mode codes with data are also prevented.

Subsystem Data In Sequence (Figure 2.3)

The "Data In" sequence obtains data from the subsystem for transmission and has two parts:

1) Control Word
2) Data

The sequence is repeated for each data word transferred.

The control word is timed by the CLEB pulse. The control word contains the subaddress and Data word count information. The data word count field has an incrementing value from zero up to the number of words to be transferred less one. The control word is latched by the subsystem and the subaddress field concatenated with the incrementing word count provide 10 BIT memory addressing.

The data word is timed by CSB and RDB pulses.

Subsystem Data Out Sequence (Figure 2.2)

The "Data Out" sequence passes data from a received command to the subsystem and has two parts:

1) Control Word
2) Data

The sequence is repeated for each data word transferred.

The control word is timed by the CLEB pulse. The control word contains the subaddress and Data word count information. The data word count field has an incrementing value from zero up to the number of words to be transferred less one. The control word is latched by the subsystem and the subaddress concatenated with the incrementing word count field provide 10 BIT memory addressing.

The data word is timed by CSB and WEB pulses.

Good Transaction

At the end of a message a signal GTB is pulsed low if the transfers to or from the subsystem have been completed without error.

The timing of GTB is such that the rising edge of HREQB can be used to strobe GTB into a latch. The latched GTB signal can then be used to initiate further subsystem activity as required.

GTB will be absent for the following reasons:

a) Failed word or message validation (including reserve mode codeswwithout ALLOWB).
b) SETMEB or SETBUSYB BIT set in subsystem status modifier word.
c) Failed subsystem handshake.
d) Overriding commands terminating a previous command prematurely.

Memory Mapping

The subaddress field (5 BITS) contained in the command word is forwarded as part of the control word for data transfers to the subsystem. This subaddress field can be used to select a 32 word block of memory. The word count field of the control word (5 BITS) is used to select an address within the 32 word block (Figure 2.0).

If the read signal is also used as part of the address (giving a total of 11 BITS) all data transfers will have their own specific area of memory.

The data transfers associated with mode codes also have special addresses.

A subaddress field of 00 or 1F indicates a mode code. For mode codes with data, the subaddress field in the control word for the data transfer is always made 1F (HEX). The word count field for the data transfer contains the mode code number. Mode codes with data are in the the range of 10-1F (HEX) (see assigned Mode Code List - Appendix A).

All messages can therefore be mapped into memory.
(See Appendix B)

TIMING DIAGRAMS

The possible 1553B messages and their corresponding subsystem sequences are summarised below:

RECEIVE COMMAND
(INCLUDING BROADCAST) (Figure 2.4)
(a) Command Sequence
(b) Data Out (repeated)

TRANSMIT COMMAND (Figure 2.5)
(a) Command Sequence
(b) Data In (repeated)

RECEIVE COMMAND RT-RT
(INCLUDING BROADCAST) (Figure 2.6)
(a) Command Sequence
(b) Data Out (repeated)

TRANSMIT COMMAND RT-RT (Figure 2.7)
(a) Command Sequence
(b) Data In (repeated)

TRANSMIT MODE CODE (NO DATA) (Figure 2.8)
(a) Command Sequence
(b) RESET See Section 1

TRANSMIT MODE CODE+DATA (Figure 2.9)
(a) Command Sequence
(b) Data In

TRANSMIT INTERNAL BIT WORD (Figure 2.10)
(a) Command Sequence

RECEIVE MODE CODE + DATA (Figure 2.11)
(a) Command Sequence
(b) Data Out Sequence

RESET MODE CODE (Figure 2.12)
(a) Command Sequence
(b) Reset (See Section 1.2)

Timings

The timing signal names are derived from shortened mnemonics of the full signal name. Additionally R(receive), T(transmit), RT(RT-RT transfers), COM(command sequence), DI(Data In sequence) DO(Data Out sequence) are used.

Timings between active low pulses are from leading edge to leading edge.

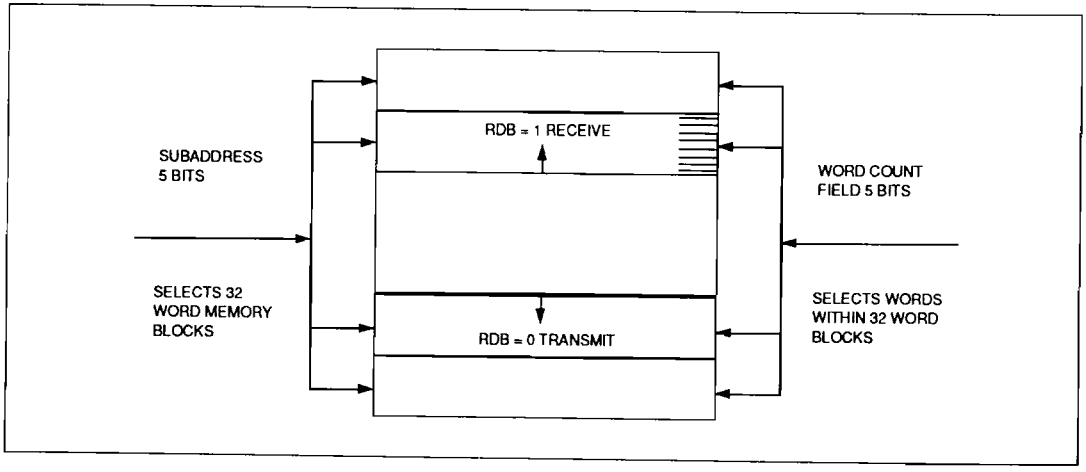


Figure 2.0

TA = - 55°C to 125°C, VDD = +10%, CL = 50pf and ITTL load.

	Symbol	Definition	Time	Units
			T Typical	
PULSE WIDTHS	T-CL	Width CLEB	1	us
	T-CS	Width CSB	1	us
	T-GT	Width GTB	1	us
	T-RD	Width RDB	2	us
	T-SYNC	Width SYNCB	1	us
	T-WE	Width WEB	1	us
	T- RESET	Width RESETB	1.2	us
COMMAND SEQUENCE	T-HR-CL	HREQB to CLEB in Command Sequence	2	us
	T-CL-CS	CLEB to CSB in Command Sequence	2	us
	T-CS-CS	CSB to CSB in Command Sequence	2.5	us
	T-CS-RD	CSB to RDB in Command Sequence	2	us
COMMAND SEQUENCE TO DATA TRANSFER	T-R-COM-DO	Receive: Command CLEB to Data Out CLEB	19*	us
	T-T-COM-DI	Transmit: Command CLEB to Data In CLEB	18*	us
	T-R-RT-COM-DO	Receive: Command to Data Out CLEB for RT- RT transfer	61.5*	us
	T-T-RT-COM-DO	Transmit: Command CLEB to Data In CLEB for RT- RT transfer	18*	us
DATA OUT SEQUENCE	T- R - DO- DO	CLEB to CLEB Data Sequence	20*	us
	T-R-CL-CS	CLEB to CSB in Data Sequence	2	us
	T- R - CS - GT	CSB to GTB for Last Data Out Sequence	3	us
DATA IN SEQUENCE	T-T-DI-DI	CLEB to CLEB in Sequence	20*	us
	T-T-CL-CS	CLEB to CSB in Data In Sequence	2.5	us
	T-RD-CS	RDB to CSB in Data In Sequence	0.5	us
	T-T-CS-GT	CSB to GTB for Last Data In Sequence	3	us
GOOD TRANSACTION	T-GT-HR	GTB TO HREQB at end of sequence	0.5	us

The above times may have a spread of ±20ns.

* These timings are affected by the 1553 bus timing of words.

Table 2: AC Electrical Characteristics

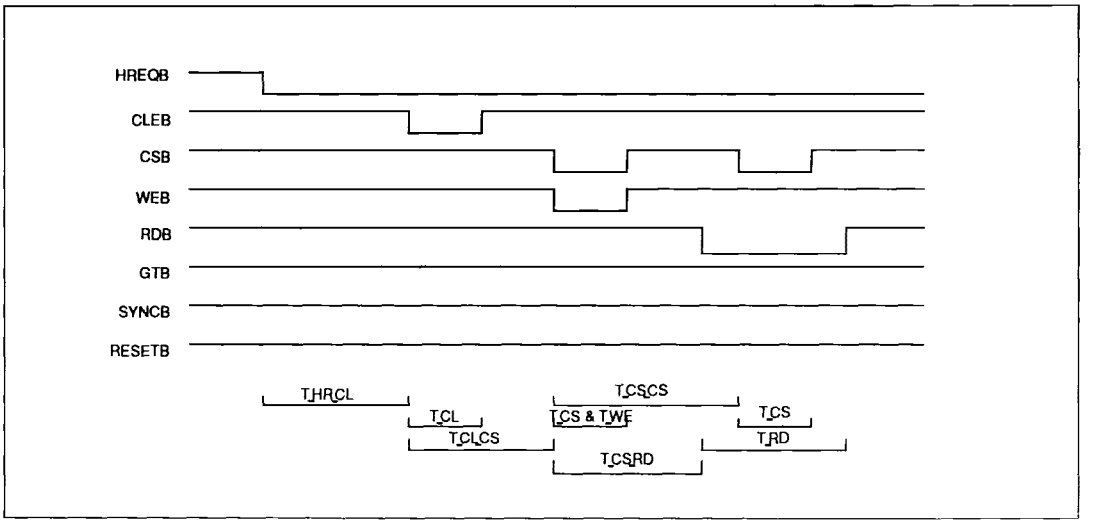


Figure 2.1: Command

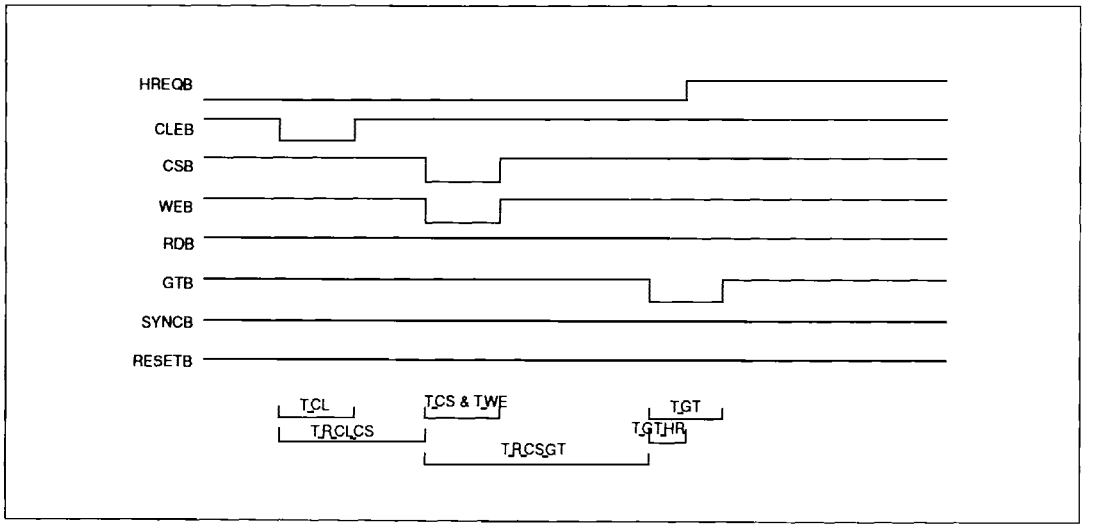


Figure 2.2: Data Out

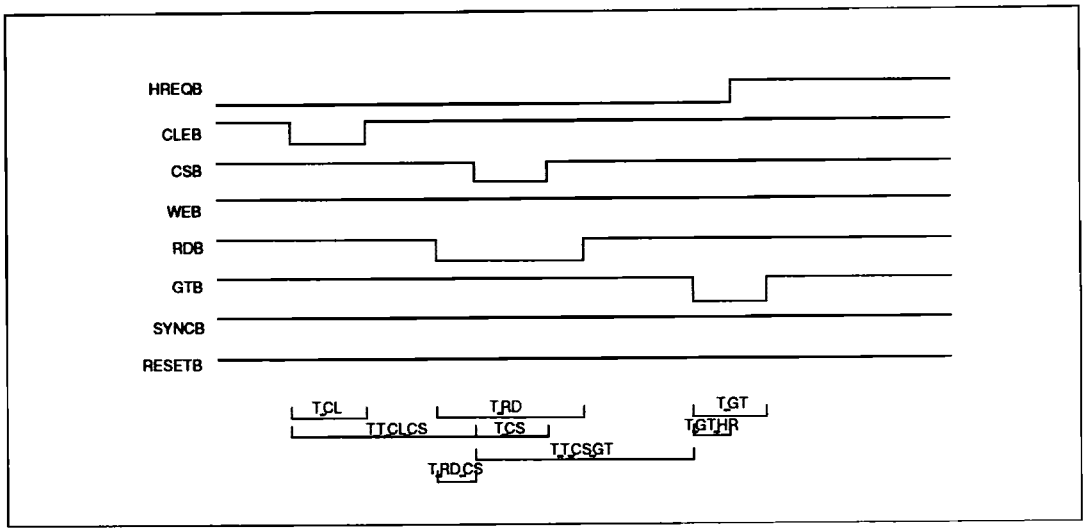


Figure 2.3: Data In

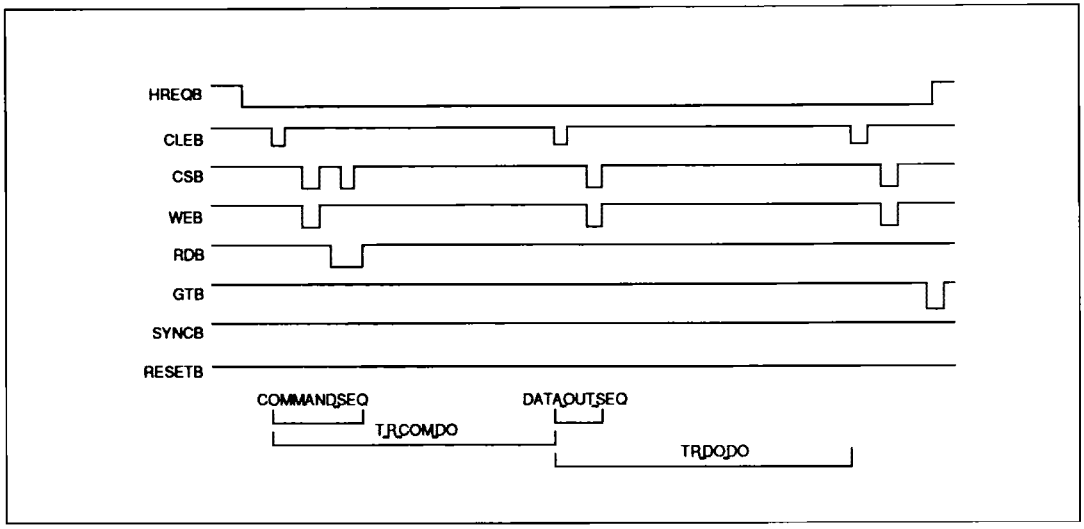


Figure 2.4: Receive Commands (including Broadcast)

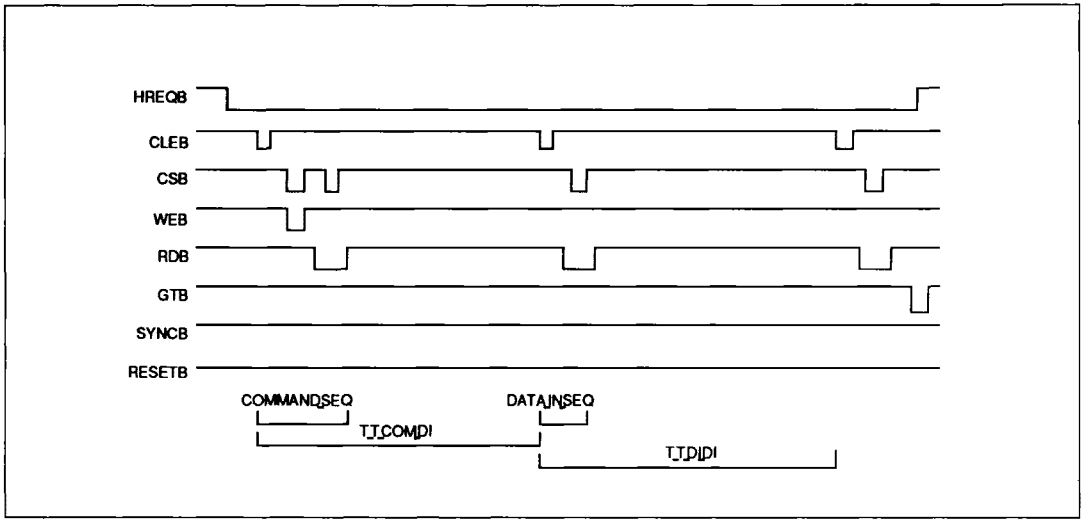


Figure 2.5: Transmit Commands

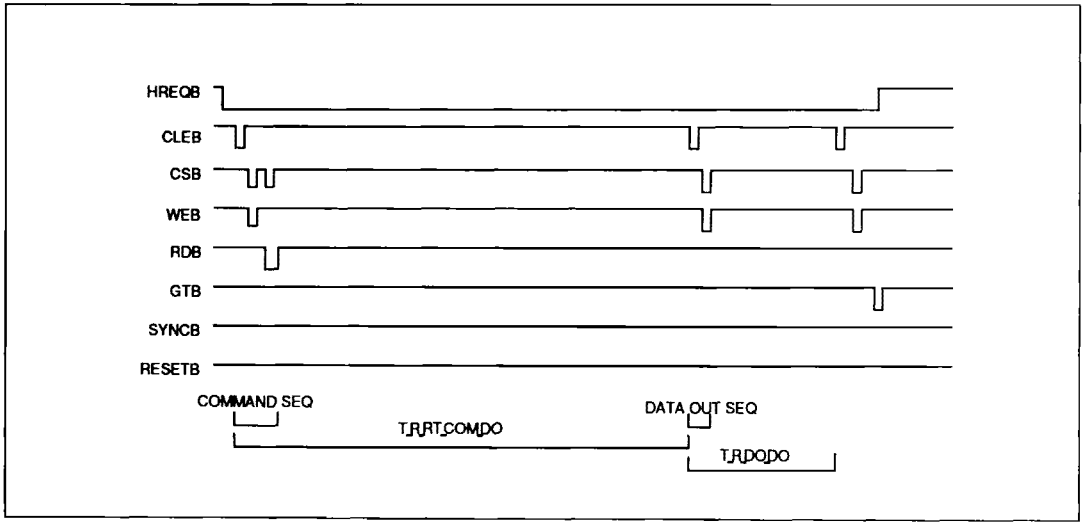


Figure 2.6: Receive Command RT-RT

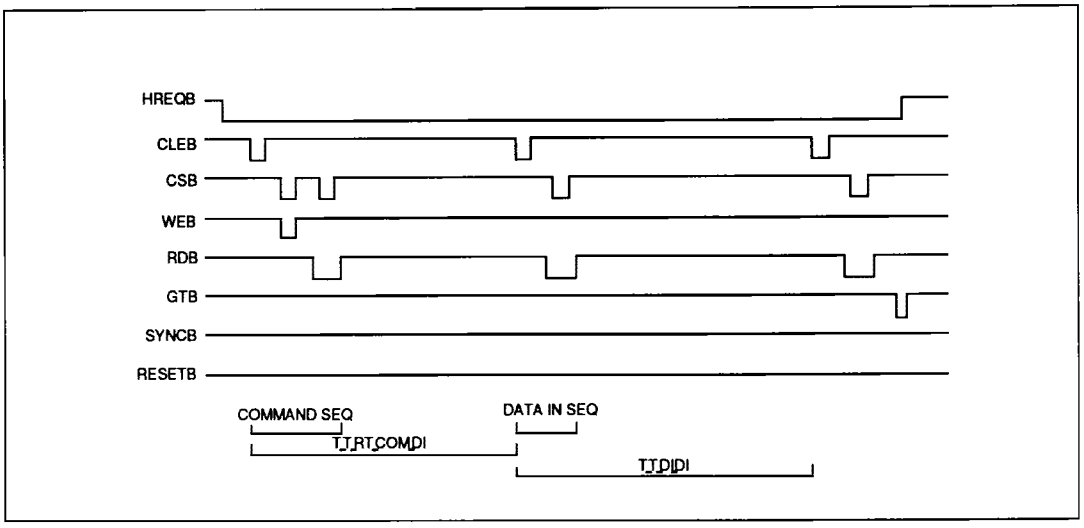


Figure 2.7: Transmit Command RT-RT

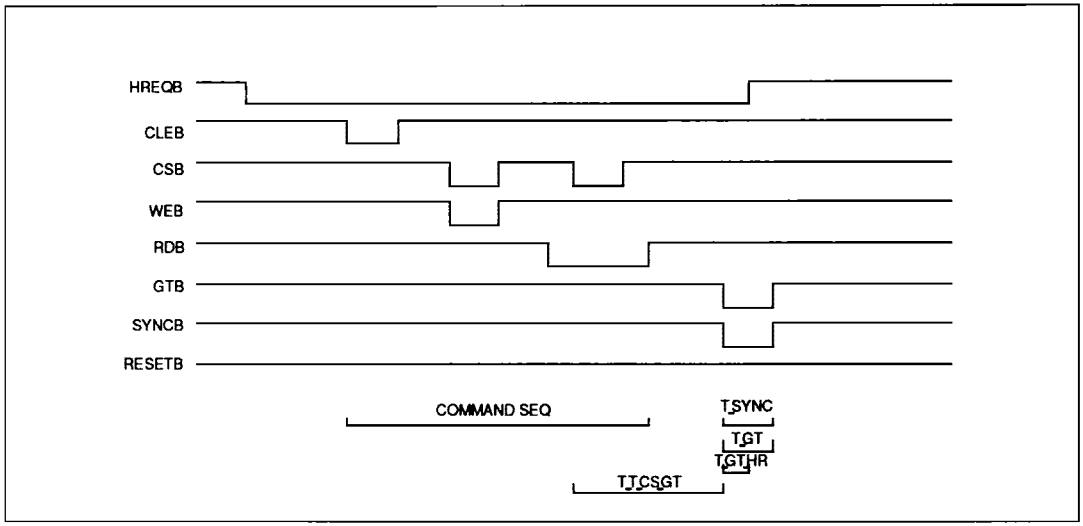


Figure 2.8: Transmit Mode (No Data)

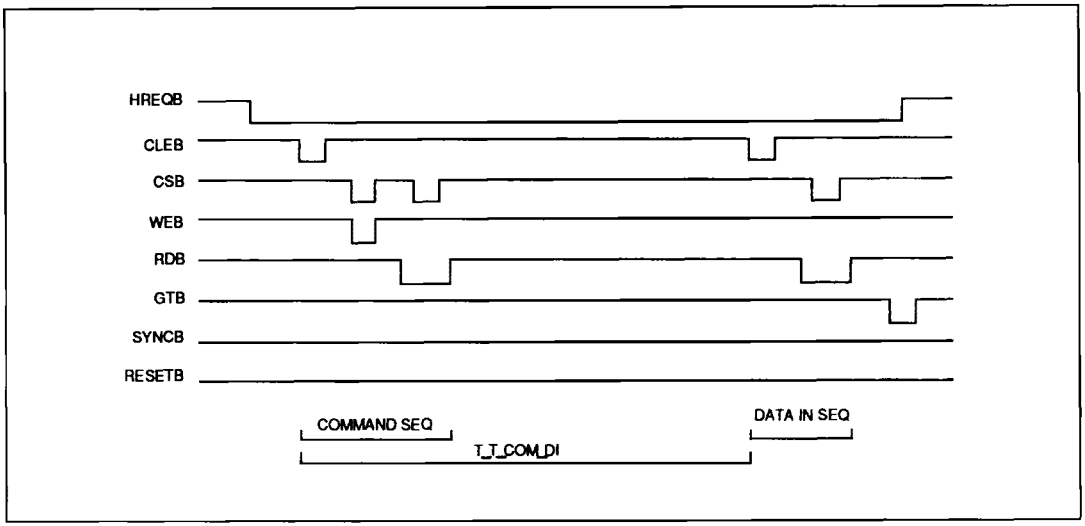


Figure 2.9: Transmit Mode Code + Data

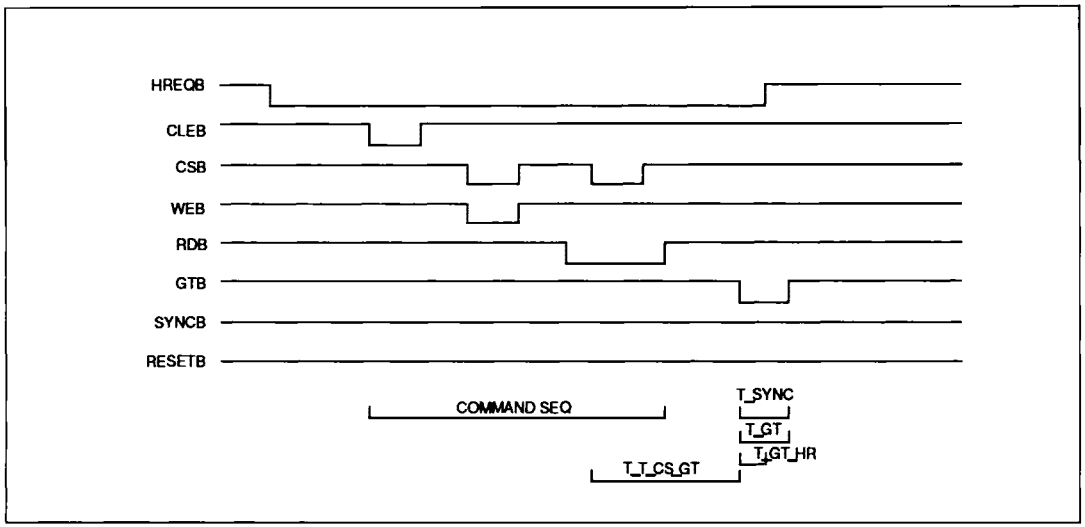


Figure 2.10: Transmit Internal Bit Word

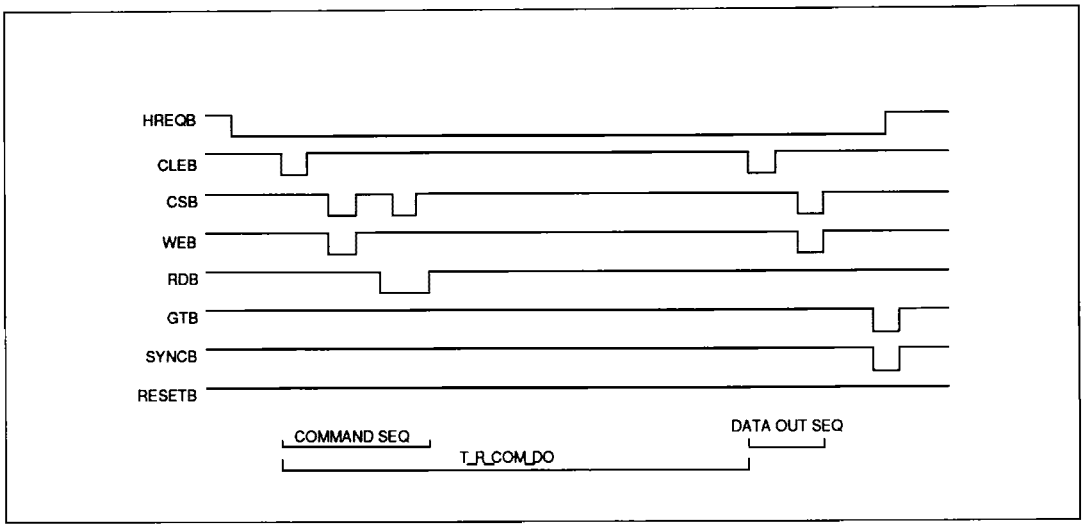


Figure 2.11: Receive Mode Code + Data

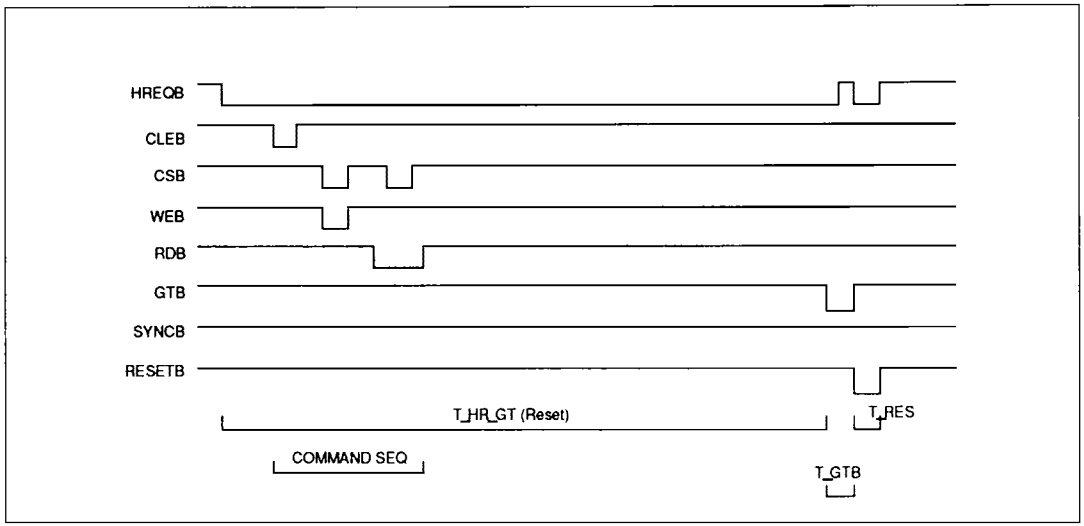


Figure 2.12: Reset

3. HIGHWAY TIMINGS

TA = -55°C to 125°C, VDD = ±10%, CL = 50pf and ITTL load.

Symbol	Definition	Limits			Units
		Min	Typ	Max	
WRITE CYCLE					
T-DRIV	Highway driven from H1Z			500	ns
THW-VAL	Highway data valid		200		ns
THW-HOLD	Highway hold time	500			ns
T- H1Z	Highway to H1Z from driven			na	ns
READ CYCLE					
THR - SET	Highway set up time	500			ns
THR-HOLD	Highway hold time	0			ns

Table 3.1: Electrical Characteristics

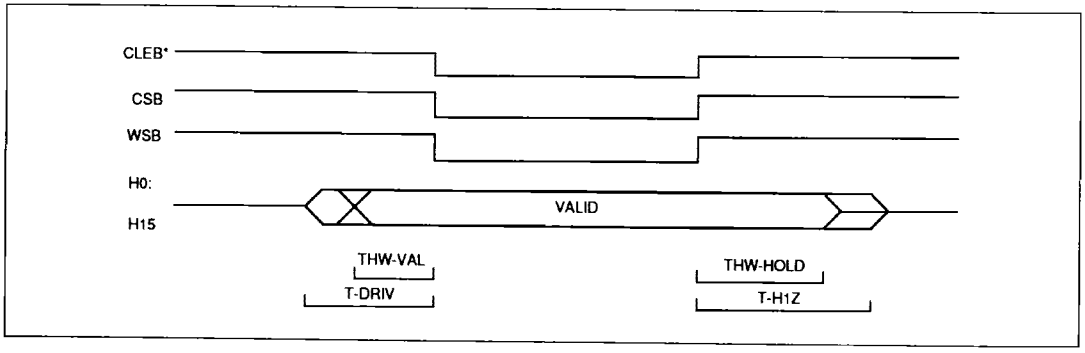


Figure 3.1: Write Cycle

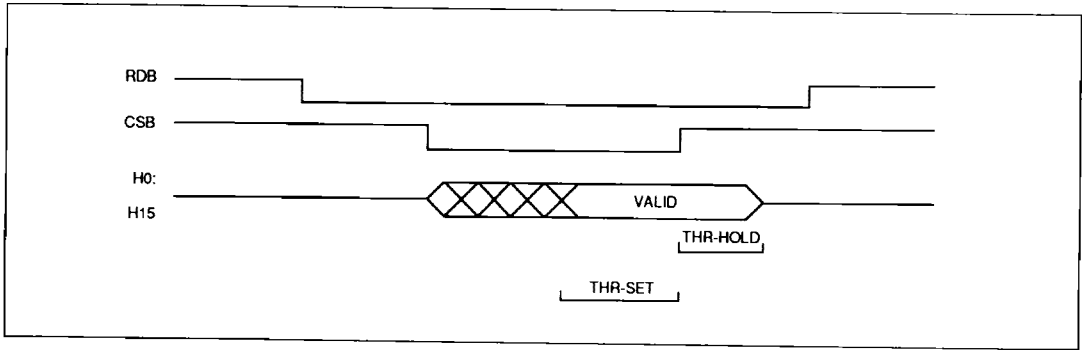


Figure 3.2: Read Cycle

4. RESPONSE TIME

The typical response time of the MA805 chip to messages is between 10 and 10.5µsecs. The measurement is from the mid-point of the parity bit of the last word of the command message (RXDATAO Pin of MA805) and the mid-point of the status response (TXDATAO Pin of MA805).

Delayed Status

An option DELSTATB is provided in the initialisation word. When this Bit is active low the response from the MA805 is delayed by an extra 31.5µsecs. This is for use with those subsystems which need extra time before data can be provided. If RT-RT transfers are to be used as well then the TM1B, TMOB Bits of the initialisation word should be selected accordingly (See Note 3 of the INITWORD section of the Data Sheet).

5. OVERRIDING COMMAND

A command is said to be overriding when a valid command on one bus is terminated before completion, due to reception of a valid command on the other bus. The subsystem signals for the interrupt message are turned off immediately. The second message is then processed. HREQB switches off between the messages with a minimum off period of 1.5µsecs.

If the spacing between the commands is such that GTB starts, then it will be completed and straddle the HREQB rising edge as normal.

Handshake

The signals HREQB, HACKB and HBUSYB provide a handshake between the MA805 and the subsystem. On receipt of a bus message a request is made to the subsystem with HREQB. The subsystem must reply with either HACKB or HBUSYB within 1µsec, otherwise a handshake fail will be recorded. HACKB or HBUSYB must be held active until HREQB goes inactive, failure to do so will result in a handshake failure.

The response to HREQB does not affect the timing of the subsystem signals, (which are timed relative to the HREQB signal going active), but is a time window for a GO/handshake fail decision.

6. INITIATE REGISTER WRITE

Initiate Register Write is a selectable option (IRWB = 0). It transfers the contents of four MA805 registers to the subsystem. The registers are initialisation word, status word, BIT word and Last Command.

The IRW sequence has eight words. Each register word is preceded by a unique control word which can be used as an address (see data sheet).

The timings are fixed and there is no GTB (see Figure 6.1). The IRW sequence has low priority and will be aborted if the MA805 is required for command servicing.

There are two modes of operation:

1) Automatic (IRWB=0), (Figure 6.1 and 6.2).
2) On Request (IRWB pulsed low), (Figure 6.3).

1) Automatic (IRWB=0)

An IRW sequence is output to the subsystem following any 1553 Bus message with a valid command word for the RT.

The subsystem signals for the 1553 messages are as normal. After HREQB goes inactive at the end of the message, the IRW sequence normally starts after a delay of 1.5usecs. For Reset, self-test and internal BIT word mode codes (where there is extra MA805 activity after the subsystem transfer) there are larger delays before the IRW sequence is outputted.

2) On Request (IRWB pulsed low)

The subsystem initiates the IRW sequence from the MA805 internal registers by pulsing IRWB low 0.5usec minimum, provided that the terminal is not servicing a command (see Figure 6.3). If the terminal is busy then hold IRWB=0 until sequence is output.

	Symbol	Definition	Time	Units
			Typ	
PULSED INITIATE REGISTER WRITE	T- IRW- HR	IRW to HREQB going Active Low	2.5	us
	T-IRW-PULSED	IRW Pulse Width	0.5	us
DELAY IRW After Command (IRW=0)	T-IRW1	Normal HREQB inactive period (see T- RW2 to 4 for exceptions)	1.5	us
	T- IRW2	HREQB inactive period after Mode Code Reset	9.5	us
	T-IRW3	HREQB inactive period after Mode Code Internal Bit Word	21.5	us
	T-IRW4	HREQB inactive period after Mode Code Self-test	27.5	us
REGISTER WRITE SEQUENCE	T-HR-CL (IRW)	HREQB to first CLEB in register Write Sequence	2.5	us
	T-CL-CS (IRW)	CLEB to CSB in Register Write Sequence	2	us
	T- CS-CL (IRW)	CSB to CLEB in Register Write Sequence	2	us
	T-CS-HR (IRW)	Last CSB to HREQB in Register Write Sequence	1.5	us

The above times may have a spead of ±20ns.

Table 6.1: Electrical Characteristics

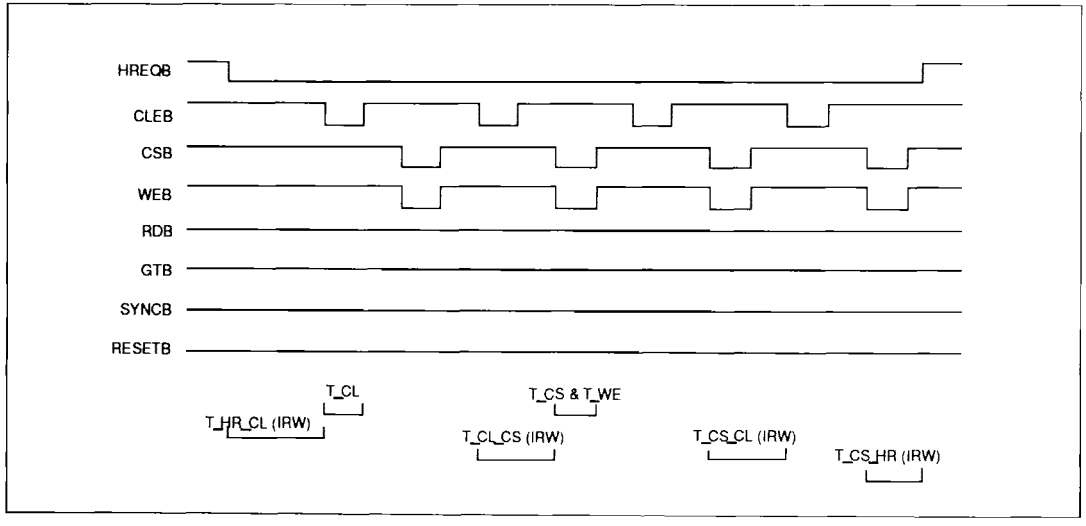


Figure 6.1: Register Write Sequence

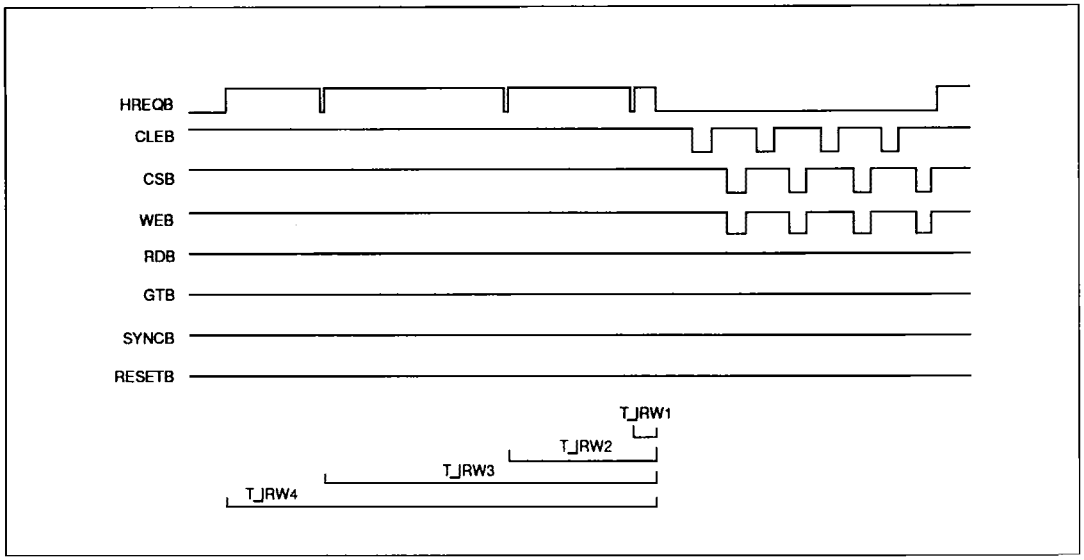


Figure 6.2: Register Write Output Times (IRW = 0)

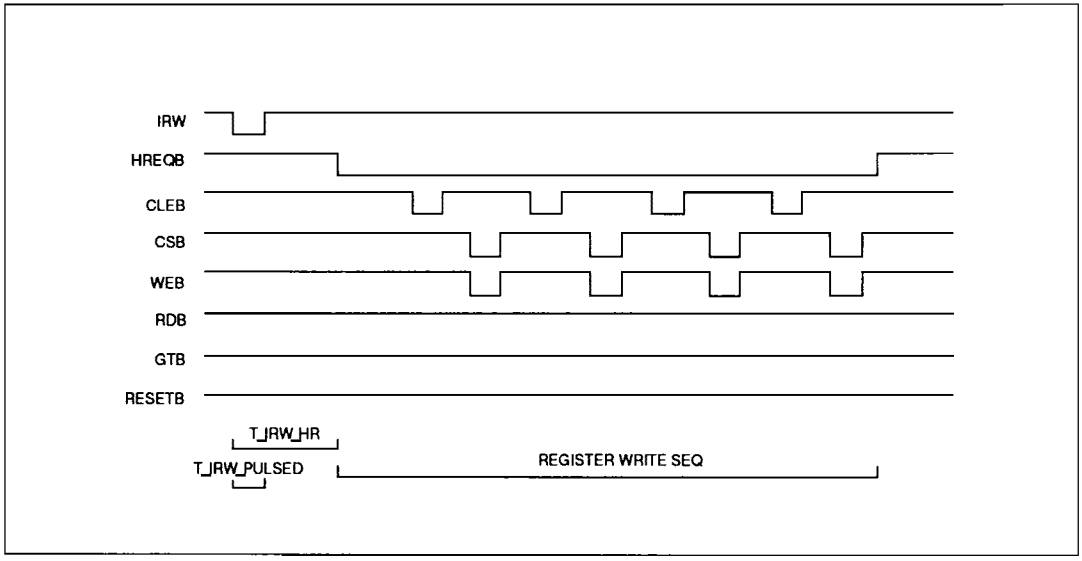


Figure 6.3: Register Write Time (IRW Pulsed Low)

7. Built-in-Test (BIT) Word Register

The MA805 contains a 16 bit register, called the BIT word register, which records message error and terminal status information supplementary to that given by the RT status word. There is an option (ABRB in the initialisation word) to select between this internal BIT word and an external BIT word.

7.1 Internal BIT word (ABRB = 1)

The internal BIT word is structured as shown in Figure 7.1. The BIT word contents will be reset to logic zero by a power up initialisation or subsystem initiated reset or a legal mode command to reset remote terminal, except for the broadcast inhibits which depend on the INITWORD. Additional reset conditions, if any, and the conditions for the setting of each bit are explained below:

BIT Word Reset Exceptions
The contents of the BIT word register shall not be altered by any of the following legal mode commands:

Transmit Status Word
Transmit Last Command
Transmit BIT Word

Transmitter Timeout Flag
This bit shall be set to logic one if a transmitter timeout occurs while the RT is transmitting. In addition, if the RT is issued with a legal Initiate Self Test mode command this bit shall be set if there is a fault in the transmitter timeout mechanism. The timeout mechanism within the transmitter is designed to operate after 680 us of terminal transmission.

Subsystem Handshake Failure
This bit shall be set to logic one if the subsystem does not acknowledge HREQB with either HACKB or HBUSYB within 1usec; or both are asserted; or the response (HACKB, HBUSYB) is removed before HREQB goes inactive.

Loop Test Failure
At all times while the terminal is transmitting the MA805 chip checks the terminal transmission for any sync, Manchester, parity or continuity error. This bit shall be set to logic one if any such error in the transmitted waveform is detected.

Mode T/R Bit Wrong
This bit shall be reset to logic zero by the reception of any valid command word with the exceptions as specified .

This bit shall be set to logic one if a valid mode command is received with a transmit/receive (T/R) bit opposite to that permitted by the Assigned Mode Code table in Appendix A.

Illegal Mode Command
This bit shall be reset to logic zero by the receptionoof any valid command word with the exceptions as specified.

This bit shall be set to logic one if either of the following two conditions arise:

0	TRANSMITTER TIMEOUT FLAG
1	SUBSYSTEM HANDSHAKE FAILURE
2	LOOP TEST FAILURE
3	MODE T/R BIT WRONG
4	ILLEGAL MODE COMMAND
5	WORD COUNT LOW
6	WORD COUNT HIGH
7	BROADCAST TRANSMIT DATA RECEIVED
8	BUS Ø SHUTDOWN
9	BUS 1 SHUTDOWN
10	SUBSYSTEM FLAG INHIBIT
11	TERMINAL FLAG INHIBIT
12	TRANSMITTER TIMEOUT ON BUS Ø
13	TRANSMITTER TIMEOUT ON BUS 1
14	BROADCAST INHIBIT BUS Ø
15	BROADCAST INHIBIT BUS 1

Figure 7.1

i) Reception of a valid mode command with the broadcast address, where this is not permitted.
ii) Reception of a valid mode command with a reserved mode command where this is not allowed by the subsystem.

Word Count Low
This bit shall be reset to logic zero by the reception of any valid command word with the exceptions as specified.

This bit shall be set to logic one if fewer valid data words are received than stipulated by the preceding valid command word.

Broadcast Transmit Data Received
This bit shall be reset to logic zero by the reception of any valid command word with the exceptions as specified.

This bit shall be set to logic one if a valid, non-mode command to transmit data words is received with the broadcast address.

Bus 0 Shutdown
This bit shall be set to logic one if bus 0 has been shutdown by one of the legal transmitter shutdown mode commands.

This bit shall be reset to logic zero if bus 0 is re-opened by one of the legal override transmitter shutdown mode commands.

Bus 1 Shutdown
This bit operates as bus 0 shutdown but relates to bus 1.

Subsystem Flag Inhibit
This bit shall be reset to logic zero if the INHSSFB bit in the STATMOD word is set to 1 except if the current command is transmit BIT word.

This bit shall be set to logic 1 if the INHSSFB bit in the STATMOD word is set to zero, except if the current command is transmit BIT word.

Terminal Flag Inhibit
This bit shall be reset to logic zero if the INHTFB bit in the STATMOD Word is set to 1 except if the current command is transmit BIT word.

This bit shall be set to logic one if the INHTFB bit in the STATMOD word is set to zero, except if the current command is transmit BIT word.

Transmitter Timeout on Bus 0
This bit shall be set to logic one if a transmitter timeout has occurred on bus 0.

Transmitter Timeout on Bus 1
This bit shall be set to logic one if a transmitter timeout has occurred on bus 1.

Broadcast Address recognition inhibited (Bus 0)
This bit shall be reset to logic zero after a reset if BCSTENO in the INITWORD is set to 1.

This bit shall be set to logic one after a reset if BCSTENO in the INITWORD is set to 0.

Broadcast Address recognition inhibited (Bus 1)
This bit shall be reset to logic zero after a reset if BCSTEN1 in the INITWORD is set to 1.

This bit shall be set to logic one after a reset if BCSTEN1 in the INITWORD is set to 0.

7.2 The BIT Word as a Expansion of the Status Word

Expansion of the Message Error Bit
Bits 3, 4, 5, 6 and 7 may be used to analyse the cause of the message error bit being set respectively into:

i) A mode command having being received with an incorrect T/R bit.
ii) A mode command having been received with a reserved mode code or an illegal broadcast address.
iii) Too few valid data words having been received.
iv) A message which was too long having been received.
v) A broadcast command to transmit data words having been received.

Expansion of the Subsystem Flag Bit
Bit 1 of the BIT word may be used to determine whether the Subsystem Flag is set due to an RT/Subsystem handshaking failure or due to the subsystem itself flagging a fault.

Expansion of the Terminal Flag Bit
Bits 0 and 2 of the BIT word may be used to analyse the cause of the Terminal Flag bit being set respectively into:

i) a transmitter timeout error having occurred.
ii) the terminal transmitting erroneous waveforms.

RT Self Test Results
If the RT fails its self test this will be reflected in the Status Word by the setting of the Terminal Flag bit.

The error source may be further analysed by presenting the RT with the following sequence of mode commands:

a) Reset Remote Terminal
b) Initiate Self Test
c) Transmit BIT Word

Bits 13, 12 and 0 of the BIT word may then be interpreted as follows:

Tx Timeout on Bus N	Tx Timeout Flag	
0	0	Self Test aborted due to superseding valid command
0	1	Transmitter timeout mechanism inoperative
1	0	Self Test good
1	1	Transmitter timeout mechanism operating incorrectly

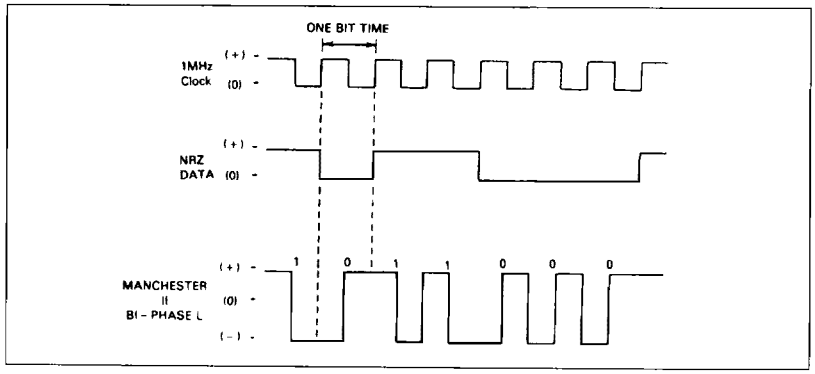
where N is the bus on which the self test command was issued.

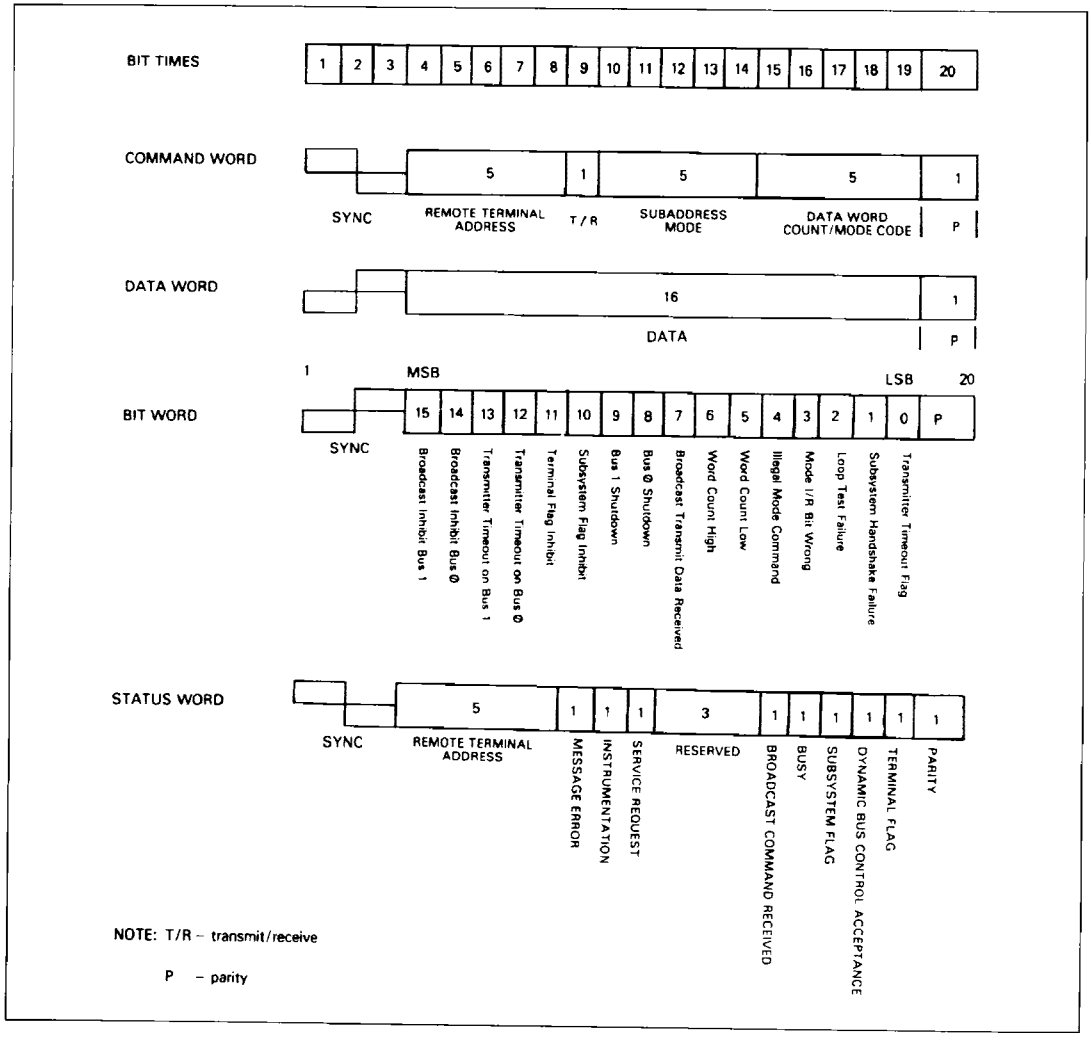
It should be noted that an RT self test forces the transmitter timeout mechanism to operate. The self test circuitry then checks:

a) that the mechanism does operate
and b) that the mechanism operates correctly.

7.3 External BIT Word (ABRB =0)
The BIT word is provided externally by the subsystem and is non-standard. It is an option to provide the subsystem designer with an alternative method of overall system monitoring.

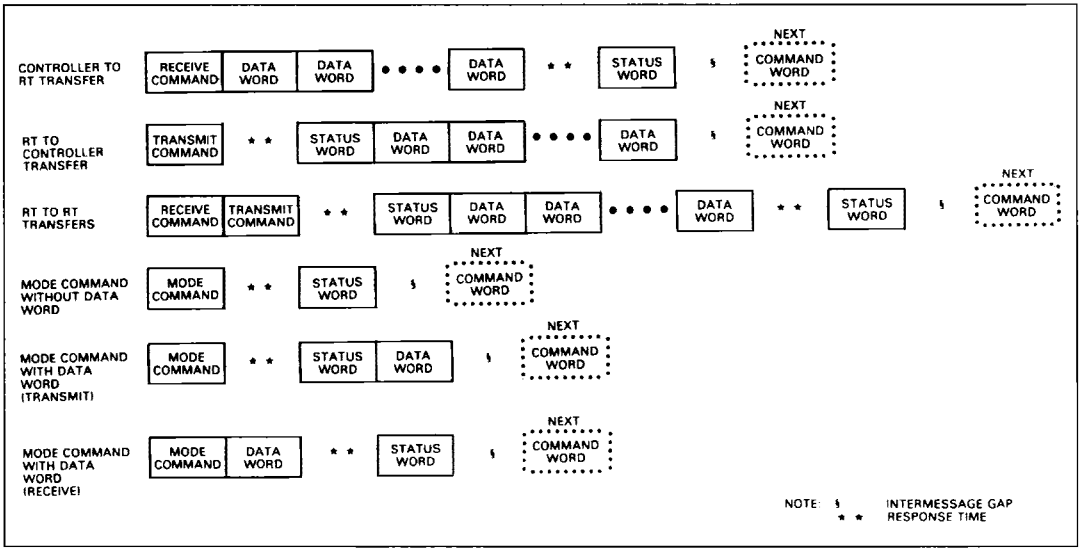
TRANSMISSION FORMATS





Appendix A.1: Data Encoding and Word Formats

TYPICAL MESSAGE FORMATS ASSIGNED MODE CODES



T/R Bit	Mode Code	Function	Associated Data Word	Broadcast Command Allowed
1	00000	Dynamic Bus Control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	No
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag Bit	No	Yes
1	00111	Override Inhibit Terminal Flag Big	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	01001	Reserved	No	TBD
↓	↓	↓	↓	↓
1	01111	Reserved	No	TBD
1	10000	Transmit Vector Word	Yes	No
0	10001	Synchronize	Yes	Yes
1	10010	Transmit Last Command	Yes	No
1	10011	Transmit BIT Word	Yes	No
0	10100	Selected Transmitter Shutdown	Yes	Yes
0	10101	Override Selected Transmitter Shutdown	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD
↓	↓	↓	↓	↓
1 or 0	11111	Reserved	Yes	TBD

NOTE: To be determined (TBD)

Appendix A.2: Typical Message Formats and Assigned Mode Codes

MEMORY MAP

For MA805 using a chip select at address 2000 HEX and read signal (RDB 1 line), Sub address (SA 5 lines), current word count (CWC 5 lines)

RAM ADDR						
RDB	SA	CWC	BADDR	WORDS	EADDR	FUNCTION
0	00	00	2000	1	2000	STATUS MODIFIER WORD
0	00	01	2001	1	2001	NOT USED
0	00	02	2002	1	2002	NOT USED
0	00	03	2003	1	2003	NOT USED
0	00	04	2004	1	2004	NOT USED
0	00	05-07	2005	3	2005-07	NOT USED
0	00	08	2008	1	2008	NOT USED
0	00	09-1F	2009	23	201F	NOT USED
0	01	00-1F	2020	32	203F	SUBADDRESS 01 DATA TO BE TRANSMITTED
0	02	00-1F	2040	32	205F	SUBADDRESS 02 DATA TO BE TRANSMITTED
0	03	00-1F	2060	32	207F	SUBADDRESS 03 DATA TO BE TRANSMITTED
0	04	00-1F	2080	32	209F	SUBADDRESS 04 DATA TO BE TRANSMITTED
0	05	00-1F	20A0	32	20BF	SUBADDRESS 05 DATA TO BE TRANSMITTED
0	06	00-1F	20C0	32	20DF	SUBADDRESS 06 DATA TO BE TRANSMITTED
0	07	00-1F	20E0	32	20FF	SUBADDRESS 07 DATA TO BE TRANSMITTED
0	08	00-1F	2100	32	211F	SUBADDRESS 08 DATA TO BE TRANSMITTED
0	09	00-1F	2120	32	213F	SUBADDRESS 09 DATA TO BE TRANSMITTED
0	0A	00-1F	2140	32	215F	SUBADDRESS 10 DATA TO BE TRANSMITTED
0	0B	00-1F	2160	32	217F	SUBADDRESS 11 DATA TO BE TRANSMITTED
0	0C	00-1F	2180	32	219F	SUBADDRESS 12 DATA TO BE TRANSMITTED
0	0D	00-1F	21A0	32	21BF	SUBADDRESS 13 DATA TO BE TRANSMITTED
0	0E	00-1F	21C0	32	21DF	SUBADDRESS 14 DATA TO BE TRANSMITTED
0	0F	00-1F	21E0	32	21FF	SUBADDRESS 15 DATA TO BE TRANSMITTED
0	10	00 1F	2200	32	221F	SUBADDRESS 16 DATA TO BE TRANSMITTED
0	11	00-1F	2220	32	223F	SUBADDRESS 17 DATA TO BE TRANSMITTED
0	12	00-1F	2240	32	225F	SUBADDRESS 18 DATA TO BE TRANSMITTED
0	13	00-1F	2260	32	227F	SUBADDRESS 19 DATA TO BE TRANSMITTED
0	14	00-1F	2280	32	229F	SUBADDRESS 20 DATA TO BE TRANSMITTED
0	15	00-1F	22A0	32	22BF	SUBADDRESS 21 DATA TO BE TRANSMITTED
0	16	00-1F	22C0	32	22DF	SUBADDRESS 22 DATA TO BE TRANSMITTED
0	17	00-1F	22E0	32	22FF	SUBADDRESS 23 DATA TO BE TRANSMITTED
0	18	00-1F	2300	32	231F	SUBADDRESS 24 DATA TO BE TRANSMITTED
0	19	00-1F	2320	32	233F	SUBADDRESS 25 DATA TO BE TRANSMITTED
0	1A	00-1F	2340	32	235F	SUBADDRESS 26 DATA TO BE TRANSMITTED
0	1B	00-1F	2360	32	237F	SUBADDRESS 27 DATA TO BE TRANSMITTED
0	1C	00-1F	2380	32	239F	SUBADDRESS 28 DATA TO BE TRANSMITTED
0	1D	00-1F	23A0	32	23BF	SUBADDRESS 29 DATA TO BE TRANSMITTED
0	1E	00-1F	23C0	32	23DF	SUBADDRESS 30 DATA TO BE TRANSMITTED
0	1F	00	23E0	1	23E0	MODE CODE 00 NO DATA NO S/S NOT USED
0	1F	01	23EI	1	23EI	MODE CODE 01 NO DATA NO S/S NOT USED
0	1F	02	23E2	1	23E2	MODE CODE 02 NO DATA NO S/S NOT USED
0	1F	03	23E3	1	23E3	MODE CODE 03 NO DATA NO S/S NOT USED
0	1F	04	23E4	1	23E4	MODE CODE 04 NO DATA NO S/S NOT USED
0	1F	05	23E5	1	23E5	MODE CODE 05 NO DATA NO S/S NOT USED
0	1F	06	23E6	1	23E6	MODE CODE 06 NO DATA NO S/S NOT USED
0	1F	07	23E7	1	23E7	MODE CODE 07 NO DATA NO S/S NOT USED
0	1F	08	23E8	1	23E8	MODE CODE 08 NO DATA NO S/S NOT USED
0	1F	09	23E9	1	23E9	MODE CODE 09 NO DATA NO S/S NOT USED
0	1F	0A	23EA	1	23EA	MODE CODE 10 NO DATA NO S/S NOT USED

Appendix B.1

RAM ADDR						
RDB	SA	CWC	BADDR	WORDS	EADDR	FUNCTION
0	1F	0B	23EB	1	23EB	MODE CODE 11 NO DATA NO S/S NOT USED
0	1F	0C	23EC	1	23EC	MODE CODE 12 NO DATA NO S/S NOT USED
0	1F	0D	23ED	1	23ED	MODE CODE 13 NO DATA NO S/S NOT USED
0	1F	0E	23EE	1	23EE	MODE CODE 14 NO DATA NO S/S NOT USED
0	1F	0F	23EF	1	23EF	MODE CODE 15 NO DATA NO S/S NOT USED
0	1F	10	23F0	1	23F0	MODE CODE 16 DATA FROM SS VECTOR WORD
0	1F	11	23F1	1	23F1	MODE CODE 17 NO DATA NOT USED
0	1F	12	23F2	1	23F2	MODE CODE 18 DATA FROM SS NO S/S NOT USED
0	1F	13	23F3	1	23F3	MODE CODE 19 DATA FROM SS BITWORD
0	1F	14	23F4	1	23F4	MODE CODE 20 NO DATA - NOT USED
0	1F	15	23F5	1	23F5	MODE CODE 21 NO DATA - NOT USED
0	1F	16	23F6	1	23F6	MODE CODE 22 RESERVED MODE DATA
0	1F	17	23F7	1	23F7	MODE CODE 23 RESERVED MODE DATA
0	1F	18	23F8	1	23F8	MODE CODE 24 RESERVED MODE DATA
0	1F	19	23F9	1	23F9	MODE CODE 25 RESERVED MODE DATA
0	1F	1A	23FA	1	23FA	MODE CODE 26 RESERVED MODE DATA
0	1F	1B	23FB	1	23FB	MODE CODE 27 RESERVED MODE DATA
0	1F	1C	23FC	1	23FC	MODE CODE 28 RESERVED MODE DATA
0	1F	1D	23FD	1	23FD	MODE CODE 29 RESERVED MODE DATA
0	1F	1E	23FE	1	23FE	MODE CODE 30 RESERVED MODE DATA
0	1F	1F	23FF	1	23FF	MODE CODE 31 RESERVED MODE DATA
1	00	00	2400	1	2400	COMMAND WORD
1	00	01	2401	1	2401	INIT WORD (IRWB SEQ)
1	00	02	2402	1	2402	STATUS (IRWB SEQ)
1	00	03	2403	1	2403	NOT USED
1	00	04	2404	1	2404	BIT WORD (IRWB SEQ)
1	00	05	2405	1	2405	NOT USED
1	00	06	2406	1	2406	NOT USED
1	00	07	2407	1	2407	NOT USED
1	00	08	2408	1	2408	LAST COMMAND (IRWB SEQ)
1	00	09-1F	2409	23	241 F	NOT USED
1	01	00-1F	2420	32	243F	SUBADDRESS 01 RECEIVED DATA
1	02	00-1F	2440	32	245F	SUBADDRESS 02 RECEIVED DATA
1	03	00-1F	2460	32	247F	SUBADDRESS 03 RECEIVED DATA
1	04	00-1F	2480	32	249F	SUBADDRESS 04 RECEIVED DATA
1	05	00-1F	24A0	32	24BF	SUBADDRESS 05 RECEIVED DATA
1	06	00-1F	24C0	32	24DF	SUBADDRESS 06 RECEIVED DATA
1	07	00-1F	24E0	32	24FF	SUBADDRESS 07 RECEIVED DATA
1	08	00-1F	2500	32	251F	SUBADDRESS 08 RECEIVED DATA
1	09	00-1F	2520	32	253F	SUBADDRESS 09 RECEIVED DATA
1	0A	00-1F	2540	32	255F	SUBADDRESS 10 RECEIVED DATA
1	0B	00-1F	2560	32	257F	SUBADDRESS 11 RECEIVED DATA
1	0C	00-1F	2580	32	259F	SUBADDRESS 12 RECEIVED DATA
1	0D	00-1F	25A0	32	25BF	SUBADDRESS 13 RECEIVED DATA
1	0E	00-1F	25C0	32	25DF	SUBADDRESS 14 RECEIVED DATA
1	0F	00-1F	25E0	32	25FF	SUBADDRESS 15 RECEIVED DATA
1	10	00-1F	2600	32	261F	SUBADDRESS 16 RECEIVED DATA
1	11	00-1F	2620	32	263F	SUBADDRESS 17 RECEIVED DATA

Appendix B.2

RAM ADDR						
RDB	SA	CWC	BADDR	WORDS	EADDR	FUNCTION
1	12	00-1F	2640	32	265F	SUBADDRESS 18 RECEIVED DATA
1	13	00-1F	2660	32	267F	SUBADDRESS 19 RECEIVED DATA
1	14	00-1F	2680	32	269F	SUBADDRESS 20 RECEIVED DATA
1	15	00-1F	26A0	32	26BF	SUBADDRESS 21 RECEIVED DATA
1	16	00-1F	26C0	32	26DF	SUBADDRESS 22 RECEIVED DATA
1	17	00-1F	26E0	32	26FF	SUBADDRESS 23 RECEIVED DATA
1	18	00-1F	2700	32	271F	SUBADDRESS 24 RECEIVED DATA
1	19	00-1F	2720	32	273F	SUBADDRESS 25 RECEIVED DATA
1	1A	00-1F	2740	32	275F	SUBADDRESS 26 RECEIVED DATA
1	1B	00-1F	2760	32	277F	SUBADDRESS 27 RECEIVED DATA
1	1C	00-1F	2780	32	279F	SUBADDRESS 28 RECEIVED DATA
1	1D	00-1F	27A0	32	27BF	SUBADDRESS 29 RECEIVED DATA
1	1E	00-1F	27C0	32	27DF	SUBADDRESS 30 RECEIVED DATA
1	1F	00	27E0	1	27E0	MODE CODE 00 NO DATA
1	1F	01	27E1	1	27E1	MODE CODE 01 NO DATA
1	1F	02	27E2	1	27E2	MODE CODE 02 NO DATA
1	1F	03	27E3	1	27E3	MODE CODE 03 NO DATA
1	1F	04	27E4	1	27E4	MODE CODE 04 NO DATA
1	1F	05	27E5	1	27E5	MODE CODE 05 NO DATA
1	1F	06	27E6	1	27E6	MODE CODE 06 NO DATA
1	1F	07	27E7	1	27E7	MODE CODE 07 NO DATA
1	1F	08	27E8	1	27E8	MODE CODE 08 NO DATA
1	1F	09	27E9	1	27E9	MODE CODE 09 NO DATA
1	1F	0A	27EA	1	27EA	MODE CODE 10 NO DATA
1	1F	0B	27EB	1	27EB	MODE CODE 11 NODATA
1	1F	0C	27EC	1	27EC	MODE CODE 12 NO DATA
1	1F	0D	27ED	1	27ED	MODE CODE 13 NO DATA
1	1F	0E	27EE	1	27EE	MODE CODE 14 NO DATA
1	1F	0F	27EF	1	27EF	MODE CODE 15 NO DATA
1	1F	10	27F0	1	27F0	MODE CODE 16 NO DATA
1	1F	11	27F1	1	27F1	MODE CODE 17 DATA TO SS SYNCHRONISE DATA
1	1F	12	27F2	1	27F2	MODE CODE 18 NO DATA
1	1F	13	27F3	1	27F3	MODE CODE 19 NO DATA
1	1F	14	27F4	1	27F4	MODE CODE 20 DATA TO SS SELECTED TRANSMITTER SHUTDOWN DATA
1	1F	15	27F5	1	27F5	MODE CODE 21 DATA TO SS OVERRIDE SELECTED TRANSMITTER SHUTDOWN DATA
1	1F	16	27F6	1	27F6	MODE CODE 22 RESERVED MODE DATA
1	1F	17	27F7	1	27F7	MODE CODE 23 RESERVED MODE DATA
1	1F	18	27F8	1	27F8	MODE CODE 24 RESERVED MODE DATA
1	1F	19	27F9	1	27F9	MODE CODE 25 RESERVED MODE DATA
1	1F	1A	27FA	1	27FA	MODE CODE 26 RESERVED MODE DATA
1	1F	1B	27FB	1	27FB	MODE CODE 27 RESERVED MODE DATA
1	1F	1C	27FC	1	27FC	MODE CODE 28 RESERVED MODE DATA
1	1F	1D	27FD	1	27FD	MODE CODE 29 RESERVED MODE DATA
1	1F	1E	27FE	1	27FE	MODE CODE 30 RESERVED MODE DATA
1	1F	1F	27FF	1	27FF	MODE CODE 31 RESERVED MODE DATA

NO ASSOCIATED DATAWORD NOT USED

Appendix B.3