Features

128Kx8 bit CMOS Static

Random Access Memory

- Access Times: 15, 20 and 25ns
- TTL Compatible Inputs & Outputs
- Fully Static Operation
- Center Power & Ground Pins
- Extended Temperature Testing

32 lead, JEDEC Approved Revolutionary Pinout

- Plastic SOJ, No. 7

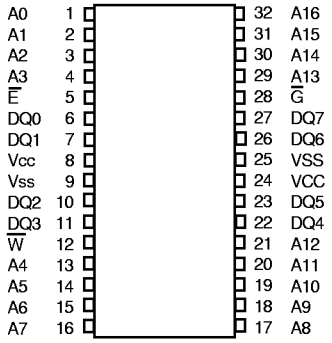
Single +3.3V (±10%) Supply Operation

128Kx8 Static RAM
CMOS, Monolithic

EDI's ruggedized plastic 128Kx8 SRAM allows the user to capitalize on the cost advantage of using a plastic component while not sacrificing all of the reliability available in a full military device.

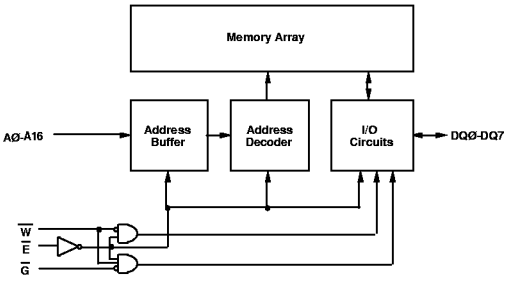
Extended temperature testing is performed with the test patterns developed for use on EDI's fully compliant 128Kx8 SRAMs. EDI fully characterizes devices to determine the proper test patterns for testing at temperature extremes. This is critical because the operating characteristics of device change when it is operated beyond the commercial temperature range. Using commercial test methods will not guarantee a device that operates reliably in the field at temperature extremes. Users of EDI's ruggedized plastic benefit from EDI's extensive experience in characterizing SRAMs for use in military systems.

Pin Configurations and Block Diagram



Pin Names

AØ-A16	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground



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Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 4.6V
Operating Temperature TA (Ambient)	
Commercial	0 ℃ to +70 ℃
Industrial	-40 ℃ to +85 ℃
Military	-55 ℃ to +125 ℃
Storage Temperature, Plastic	-65 ℃ to +125 ℃
Power Dissipation	1.5 Watt
Output Current.	20 mA
Junction Temperature, TJ	175 ℃

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	3.0	3.3	3.6	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	See Figure 1

(note: For TEHQZ,TGHQZ and TWLQZ see figure 2)

Figure 1

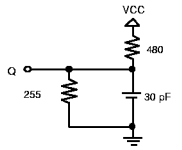
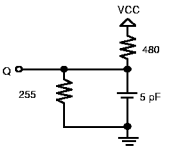


Figure 2



DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	-- --	170	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL VIN ≥ VIH	--	30	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	-- --	10	mA
Input Leakage Current	ILI	VIN = 0V to VCC	-10	10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	-10	10	µA
Output High Voltage	VOH	IOH =-4mA	2.4	--	V
Output Low Voltage	VOL	IOL = 8mA	--	0.4	V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	6	pF
Data Lines	CD/Q	8	pF

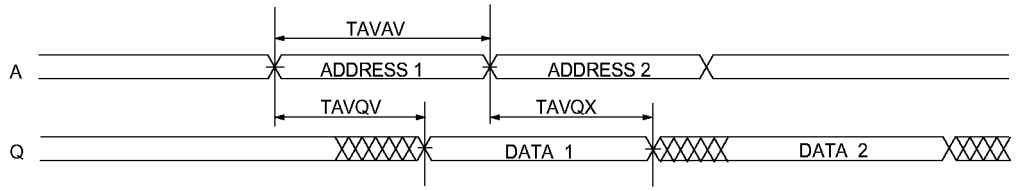
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

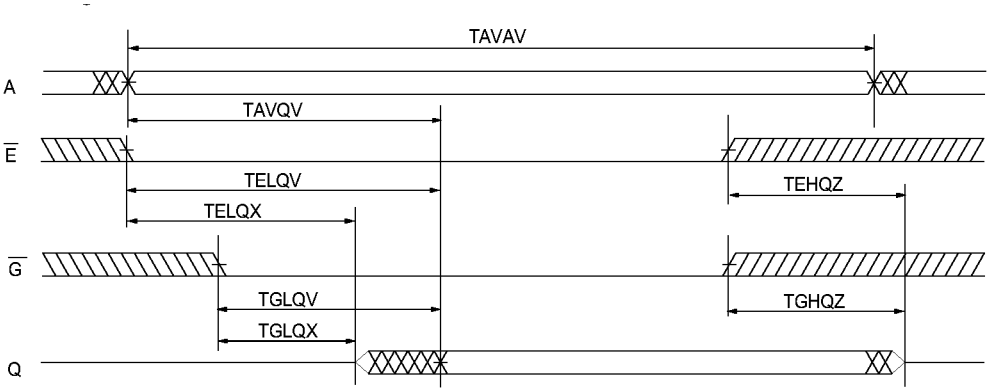
	Symbol		15ns		20ns		25ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	15		20		25		ns
Address Access Time	TAVQV	TAA		15		20		25	ns
Chip Enable Access Time	TELQV	TACS		15		20		25	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ	0	7	0	8	0	10	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		7		8		10	ns
Output Enable to Output in Low Z (1)	TGLQX	TLOZ	0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ	0	7	0	8	0	10	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High

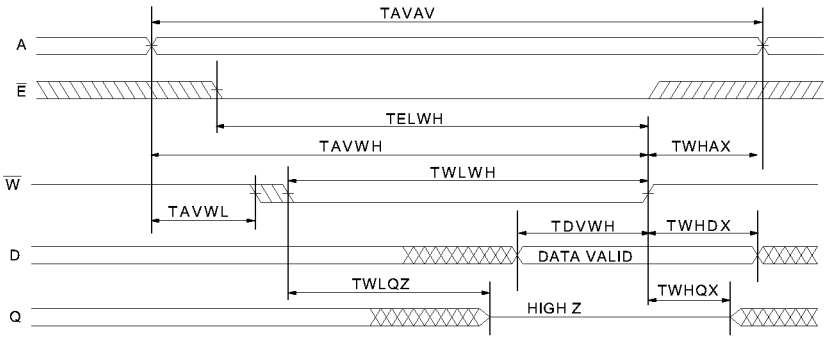


AC Characteristics Write Cycle

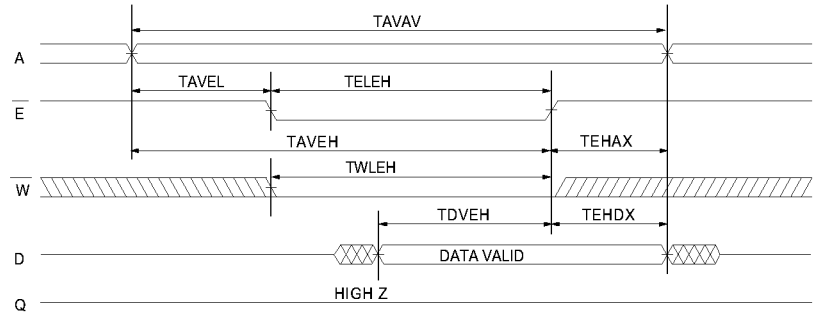
Parameter	Symbol JEDEC	Alt.	15ns Min	Max	20ns Min	Max	25ns Min	Max	Units
Write Cycle Time	TAVAV	TWC	15		20		25		ns
Chip Enable to End of Write	TELWH	TCW	10		12		17		ns
	TELEH	TCW	10		12		17		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	10		12		17		ns
	TAVEH	TAW	10		12		17		ns
Write Pulse Width	TWLWH	TWP	9		12		17		ns
	TWLEH	TWP	9		12		17		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time (1)	TWHDX	TDH	0		0		0		ns
	TEHDX	TDH	0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	7	0	8	0	10	ns
Data to Write Time	TDVWH	TDW	7		10		12		ns
	TDVEH	TDW	7		10		12		ns
Output Active from End of Write (1)	TWHQX	TWLZ	0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 - $\overline{E}$ Controlled



Ordering Information

Military (-55 ℃ to +125 ℃)

Part No.	Speed (ns)	Package No.
EDI88128V15MM	15	7
EDI88128V20MM	20	7
EDI88128V25MM	25	7

Industrial (-40 ℃ to +85 ℃)

Part No.	Speed (ns)	Package No.
EDI88128V15MI	15	7
EDI88128V20MI	20	7
EDI88128V25MI	25	7

Package Description

Package No. 7
32 Lead Plastic Small
Outline J-Lead Package
Theta J_A = 50 ℃/W
Theta J_C= 18 ℃/W