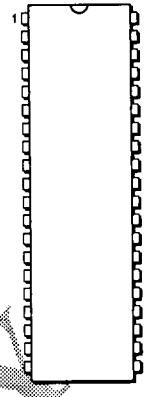
FEATURES

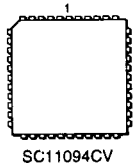
- ☐ Single +5V Supply
- ☐ Full duplex modem from 300 to 2400 bit/s
- ☐ Half duplex modes from 2400 to 14,400 bit/s
- ☐ Low power CMOS with 5mW power down mode
- ☐ On-chip constellation pattern generator
- ☐ 1800/550 Hz notch filter and 1800/550/2225 Hz tone generator
- ☐ 2 Relay Drivers
- ☐ Internal Hybrid
- ☐ Voice mode at 11,000, 9600, 8000 & 7300 s/s
- ☐ Compatible with CCITT V.17, 21, 22, 22bis, 23, 27, 27ter, 29, 26bis, 33 and Bell 103, 202, 212A Standards
- ☐ Serial DSP interface
- ☐ Synchronous and asynchronous modes
- ☐ 12-bit ADC and DAC
- ☐ Cable equalizer
- ☐ Supports caller ID & call waiting
- ☐ Captain & cellular modes

40-PIN DIP PACKAGE



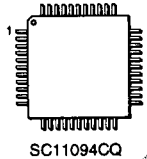
SC11094CN

44-PIN PLCC PACKAGE



SC11094CV

44-PIN QFP PACKAGE (14mm)



SC11094CQ

BLOCK DIAGRAM

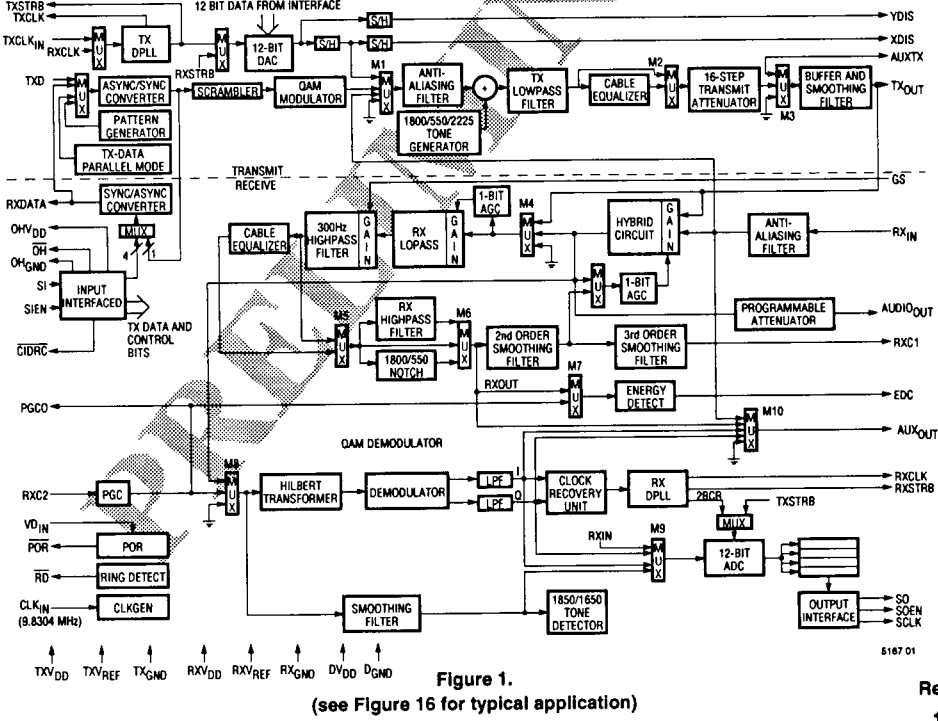


Figure 1.
(see Figure 16 for typical application)

GENERAL DESCRIPTION

The SC11094 provides all the analog functions required for a 300 through 2400 bit/s data modem and group 3 facsimile modem operating up to 14,400 bit/s. It is designed for use with the Sierra SC11066 series DSP chip with internal memory to implement a full duplex 2400 bit/s modem data pump compatible with CCITT V.22 bis recommendations and half duplex CCITT V.29, V.27ter recommendations. With the addition of one of Sierra's Modem Advanced Co-processors (SC11011, 11021, 11091 etc.), the three chip set comprises a complete intelligent EIA Class 2 fax & data modem. Depending on the Sierra DSP IC selected, a variety of modems can be built including CCITT recommendations V.21, V.23, V.26, V.17, Bell 103, 202, 212A and more. Voice messaging is supported with the 12 bit ADC and DAC. Sierra co-processors add a variety of protocols and command sets including Class 2 fax, Voice, DTMF, BFT, MNP, V.42bis etc. The chip set is ideal for pocket, laptop and notebook applications.

PIN DESCRIPTIONS

PIN NAME	TYPE	PIN NUMBER			DESCRIPTION
		PLCC	DIP	QFP	
$AUDIO_{OUT}$	AO	26	23	31	Audio monitor; Analog Output. The hybrid output is passed through a programmable attenuator and fed to this pin. It can be used to drive a speaker for line audio monitoring.
AUX_{OUT}	AO	27	24	32	Auxillary output; Analog Output. This pin is mainly used for testing purposes. It provides access to I and Q outputs, receive analog input or receive filter output.
AUXTX	B	18	16	23	Auxiliary transmit signal; Input. This pin provides an extra input for transmit signal. It can be transmitted alone or summed with the internal signal to become the final transmit signal.
CIDRC	OE	37		42	Relay Driver A.
CLK_{IN}	IA	36	33	41	Master clock; Input; TTL; CLK_{IN} = 9.830MHz.
D_{GND}	PWR	7	6	12	Digital ground; D_{GND} = 0V.
DV_{DD}	PWR	33	30	38	Digital positive power supply; DV_{DD} = +5V.
EDC	AO	29	26	34	Energy detect capacitor; A1.0uF tantelin capacitor should be connected between this pin and RXA_{GND}.
GS	IA	11	10	16	Gain Select to compensate for loss in line coupling transformer; Input. When left open or tied to V_{SS}, the compensation is 0 dB; connected to ground, +2 dB compensation is provided; and when tied to V_{CC}, the compensation is +3 dB.
N/C		10, 16, 23, 24,	9, 21	15, 21, 28, 29	These pins should be left unconnected.
$\overline{OH}$	QE	39	35	44	Off-Hook relay switch; Open Drain Output; It is used to drive directly a +5V relay coil with a worst case resistance of 360 ohms and operating voltage of 4V DC across the coil.
OH_{GND}	GND	40	36	1	Ground for Off-Hook relay switch; OH_{GND} = 0V.
OHV_{DD}	PWR	38	34	43	Positive power supply for Off-Hook relay switch; OHV_{DD} = +5V.
PGCO	AO	19	17	24	Programmable gain control output; Analog Output.
$\overline{POR}$	OD	34	31	39	Power-on reset; Output; TTL. This pin will be activated when the power is initially brought up or VD_{IN} drops below 3.5V for more than 30ms.
$\overline{RD}$	AI	1		6	Ring detect input; internal pullup. Active even in power-down.
RXV_{REF}	AI	31	28	36	Analog reference for RX section; Analog input RXV_{REF} = 2.5V.
RXC1 RXC2	AI AI	22 21	20 19	27 26	An external capacitor is required between these two pins. The capacitor, together with the internal 25K resistor, provides AC coupling between the output of the receive filter and the PGC input.

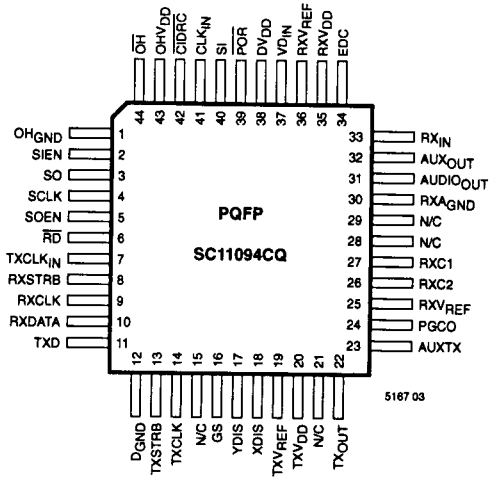
PIN DESCRIPTIONS (continued)

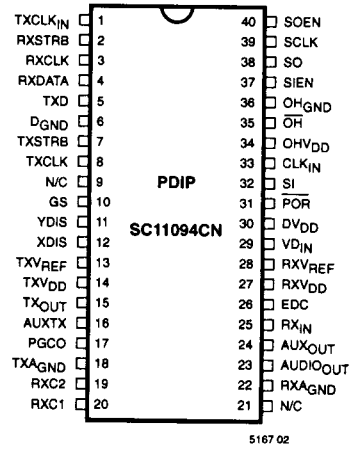
PIN NAME	TYPE	PIN NUMBER PLCC	DIP	QFP	DESCRIPTION
RXCLK	OD	4	3	9	Receive bit clock; Output; TTL. In V.29, V.27, V.33 and V.22bis synchronous mode, the falling edge of RXSTRB is synchronous to the rising edge of RXCLK. Also in V.22bis synchronous mode, data on RXDATA is valid on the rising edge of RXCLK. In V.22bis asynchronous mode, the RXCLK pin is held high. In other modes (besides V.29, V.27, V.33 and V.22bis) RXCLK is the same as TXCLK.
RXDATA	OD	5	4	10	Received data; Output TTL. The on-chip sync-to-async converter converts the demodulated and descrambled modem data from DSP into asynchronous data and feeds back to DSP at the RXDATA pin. This pin is used only in V.22bis mode. In other modes, the RXDATA pin is held high.
RX_{IN}	AI	28	25	33	Receive signal; Analog Input.
RXSTRB	OD	3	2	8	Receive strobe clock; Output; TTL. In V.29, V.27, V.33 and V.22bis mode, it is synchronous to the baud clock recovered by the Receive Phase-Locked Loop from the far end modem. Normally high, a short (6.9µs - 26µs) negative pulse is generated for every baud clock. It is used as an interrupt signal to the DSP. Internally, RXSTRB triggers the A/D conversions of I and Q channels. In one RXSTRB period, two samples are taken from each channel, one at the center of the baud, and the other at the end of the baud. In other modes, RXSTRB is the same as TXSTRB and the A/D takes only one sample of the receive signal per RXSTRB period.
RXV_{DD}	PWR	30	27	35	Analog positive power supply for RX section RXV_{DD} = +5V.
RXA_{GND}	PWR	25	22	30	Analog ground for RX section; RXA_{GND} = 0V.
SCLK	OD	43	39	4	Serial shift clock; Output; TTL. It is used both to shift data into the input register and data out of the output register.
SI	IA	35	32	40	Serial input data; Input; TTL. It is shifted serially into a 16-bit register. The three most significant bits (D15-13) designate the contents of 13 least significant bits (D12-0) into the data/control register.
SIEN	IA	41	37	2	Serial input enable; Input; TTL. It enables the writing of serial data into the 16-bit input register.
SO	OD	42	38	3	Serial output data; Output; TTL. sixteen bits of data are shifted out from the output register. The first 10 bits correspond to the ADC output bits D11-2; The next two bits can be either ADC output bits D1–D0 or status bits AGCG1 and AGCG2 come next. The last four bits are status bits ED, C1650, C1850 and TXBE. See Figure 15.
SOEN	OD	44	40	5	Serial output enable; Output; TTL. It enables the data stored at the 16-bit output register to be shifted out serially.
TXA_{GND}	IA	20	18	25	Analog ground for TX section; TXA_{GND} = 0V.
$TXCLK_{IN}$	IA	2	1	7	External clock for the Transmit Phase-Locked Loop; Input; TTL. This is the input clock for the Transmit Phase-Locked Loop which locks both TXCLK and TXSTRB.
TXD	IA	6	5	11	Transmit data; Input TTL. This pin is used only in V.22bis serial mode. In other modes, including V.22bis parallel mode, the TXD pin is ignored.
TXCLK	OD	9	8	14	Transmit bit clock; Output; TTL. It is synchronous and locked to the TXCLKIN. In V.22bis synchronous mode, data on TXD is latched on the rising edge of TXCLK. In V.22bis asynchronous mode, the TXCLK pin is held high.
TX_{OUT}	AO	17	15	22	Transmit signal; Analog Output.

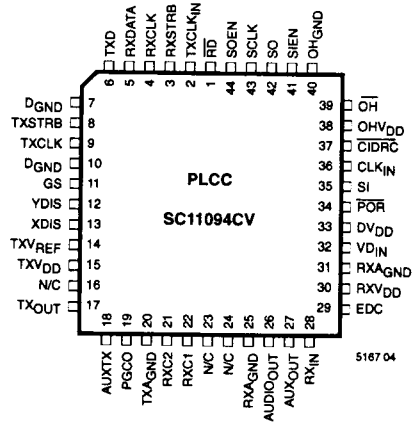
PIN DESCRIPTIONS (continued)

PIN NAME	TYPE	PIN NUMBER PLCC	PIN NUMBER DIP	PIN NUMBER QFP	DESCRIPTION
TXSTRB	OD	8	7	13	Transmit strobe clock; Output; TTL. It is used as an interrupt signal to the DSP. Internally, TXSTRB triggers the D/A conversion. The transmit data word (or 2 transmit data words if they are used to load Constellation-X and Constellation-Y registers) is transferred in one TXSTRB cycle and the D/A output is available two cycles later. In G1 and G2 mode, TXSTRB is 10.368KHz. In Tone/Voice mode, TXSTRB is either 9.6KHz or 8KHz. In other modes, it is 9.6KHz.
TXV_{DD}	PWR	15	14	20	Analog positive power supply for TX section; TXV_{DD} = +5.
TXV_{REF}	AI	14	13	19	Analog reference for TX section; TXV_{REF} = 2.5V.
VD_{IN}	PWR	32	29	37	Low voltage detect; Input. When the voltage in this pin drops below 3.5V for more than 30ms, the $\overline{POR}$ pin will be activated and the chip powered down.
XDIS	AO	13	12	18	Constellation-X display; Analog Output. 12 bits D/A output from Constellation-X register.
YDIS	AO	12	11	17	Constellation-Y display; Analog Output; 12 bits D/A output from Constellation-Y register. Both X and Y data words are written into the chip within a given strobe period and they will appear simultaneously at XDIS and YDIS two strobes later.

CONNECTION DIAGRAMS







FUNCTIONAL DESCRIPTION

Architectural Features of the Analog Processor

The analog signal processor is a 40/44 pin device that in conjunction with a digital signal processor implements high-speed facsimile and full duplex data modems.

The transmit modulation, in this implementation, is achieved in two distinctly different ways. In V.23, V.21, 103, V.29, V.27ter and single/dual tone generations, all transmit functions are achieved in the digital signal processor.

The output of the modulator is a 12-bit binary 2's complement digital word which is serially transferred to the analog signal processor on the occurrence of each transmit strobe. The 12-bit DAC on the analog processor converts the digital word to its analog value and feeds it into a sample and hold.

In all modes except G2 and G1, the transmit strobe has a rate of 9600Hz. In G2 and G1 mode, the strobe rate is 10368 Hz. The output of the sample and hold is filtered by a 6th order low-pass filter followed by a cable equalizer. The equalizer has three distinct characteristics and a by-pass mode. The 6th order low-pass filter has a flat passband. (The sinx/x distortion offsets are compensated in the digital signal processor prior to transferring the data to the analog chip. This compensation is not included in the low-pass filter since in other modes, such as V.22bis, a flat passband is desired.)

The cable equalizer is followed by a 16 step attenuator which provides 0-15dB attenuation in 1dB steps. The output of the attenuator can be summed with the signal on the AUXTX pin and after being smoothed by an analog smoothing filter, drives the TX_{OUT} pin.

In V.22bis mode, where the digital signal processor is only capable of handling the receive function, the transmit modulation is performed by the analog processor. In this mode the transmit data enters the TXD pin serially and goes to the hardware async-to-sync converter. If a synchronous mode of operation is desired, this block is disabled.

Several test and training pattern generators are included on the analog chip, which facilitates transmission of modem handshaking signals.

The async-to-sync converter is followed by the data scramblers, data encoder and I/Q channel pulse shaping filters. The outputs of pulse shaping filters are modulated by sine and cosine of the carrier and summed in a second order low-pass filter. The output of the low-pass filter is the QAM modulator signal which is directly applied to the transmit low-pass filter. From this point on, the signal goes through the same path as the output of the DAC.

Even though tone generation is done in the digital signal processor, in V.22bis mode the digital processor operates at a rate which is equal to the receiver baud timing. Therefore, it is unable to synthesize the CCITT 1800/550/2225Hz guard tones. These tones are generated by hardware means in the analog chip and summed to the QAM signal at the input of the transmit low-pass filter.

Other blocks in the transmit side include a digital phase lock loop for the transmit timing, and the "constellation-pattern" monitor outputs which can be used to display the transmit or receive signal constellations.

On the receive side, the receive signal goes through an analog anti-aliasing filter followed by a hybrid circuit. In half duplex applications the hybrid can be disabled. An audio monitor output is provided with a programmable level control which takes its input from the hybrid output signal. It can be used during call progress monitoring for audio feedback.

The output of the hybrid also goes to a one bit automatic gain control (AGC). The programmable gain is implemented at the input of the hybrid circuit. For full flexibility, the programmable gain can be forced by the processor or the AGC can be frozen to prevent it from further reacting to the peak of the incoming signal. The hybrid output goes to the receive low-pass filter, the 300 Hz high pass filter, the receive cable equalizer and the receive high-pass filter.

The receive low-pass and high-pass combination under the control of the programming bits can be altered to implement different filter types for different modes of operation.

In half duplex modes, the receive high-pass will be bypassed and the signal will go through the low-pass filter which covers only the whole frequency band of 0-3200Hz. In V.22bis, V.23, V.21 and 103 modes, where full duplex communication is achieved by frequency division techniques, the receive low-pass and high-pass combination is configured as a band pass filter.

The clock frequency is altered to move the center of the band pass filter to the frequency band of the receive signal and to place the stop band on the frequency band of the adjacent channel.

An 1800/550Hz programmable notch is included which can be placed in the receiver path to suppress the transmit 1800/550Hz guard tone. The notch filter is automatically inserted when the guard tone is activated. This will only happen during the answer mode or the originate mode with ALB = 1.

The receive filter is followed by a second order switch-capacitor low-pass smoothing filter and a third order active RC smoothing filter. The second order switched capacitor filter smooths the output of the receive filter. The RC active smoothing filter will eliminate all the clock noise present on the output

of the switched-capacitor low-pass smoothing filter.

The output of the RC active filter is brought out to a pin and is AC coupled to the input of the PGC. The PGC has a range of -9.0dB to 45.1dB with 511 steps of 0.106/step. The output of the PGC goes to an energy detect circuit, a smoothing low-pass filter and a QAM demodulator. The energy detect can be used for detecting the presence of the receive signal. It has two programmable thresholds and a 3dB hysteresis.

Under the control of the programming bits, the receive low-pass and high-pass can be configured as a 300-650Hz band-pass filter. In this mode the energy detect will be connected to the output of the PGC and the constant gain of the energy detect will be bypassed. The band-pass and energy detect combination can be used for monitoring the call progress tones with a programmable threshold. The other signal path from the output of the PGC goes to a low-pass smoothing filter.

The output of the filter goes to a zero crossing detector and 1650/1850Hz tone detector. The output of the low-pass also goes to the 12-bit analog to digital converter (ADC). In V.23, V.21, 103, signal and dual (DTMF) tone detect modes the signal is periodically sampled by the ADC and the 12-bit 2's complement binary word is supplied to the digital signal processor through the serial interface.

The sampling strobe for V.23, V.21, 103, tone detect modes is 9600Hz. In these modes the transmit and receive strobes are identical. Another signal path from the output of the PGC is to the QAM demodulator. This block includes the Hilbert transformer, two I and Q demodulators and two baseband low-pass filters.

The output of the baseband filters are the inphase (I) and quadrature (Q) components of the QAM signal, which are periodically sampled by the ADC. The sampling clock in this case is the recovered baud clock from the timing recovery circuit. The timing recovery circuit takes the I and Q channel output signals, filters them with two band pass filters centered at half the baud rate, rectifies and sums the outputs and filters the sum with a band pass centered at the baud rate.

The band pass output, after passing through a zero crossing detector, goes to a digital phase locked loop (DPLL). The output of the DPLL is the baud timing which is used by the ADC to sample the I and Q channel outputs. Two samples are taken from each channel, one at the center of the baud (mid baud sample), and the other at the end of the baud (end baud sample).

The ADC does four conversions in each baud period and stores the result in four registers which subsequently are shifted, one after the other, through the serial interface to the digital signal processor. The signal processor, having both the mid baud and end baud samples, has the option to use a T-spaced or T/2 spaced adaptive equalizer.

The QAM demodulator is used in the V.29, V.27ter, V.22bis, V.22, and Bell 212A modes. All filters and carrier signals are appropriately programmed to accommodate the selected mode.

For V.29, V.27ter, V.26bis, V.23, V.21, V.17 and 103 modes the demodulation process is completed in the digital signal processor and the demodulated data can be supplied to the parallel or serial interface. In V.22bis, V.22 and 212A modes however, during asynchronous operation, the demodulated bits should go through a sync-to-async converter for missing stop bit insertion. This block is implemented by hardware means in the analog signal processor.

During each baud period the appropriate number of digital bits are transferred back from the digital processor to the analog chip. After sync-to-async conversion, the receive data goes out of the analog chip from the RXDATA pin. This signal goes back to the digital signal processor and is multiplexed with the receive data from the digital processor. Under the control of the programming bits, depending on the selected mode, the appropriate receive output is brought to the final receive RXD pins of the digital signal processor.

The analog signal processor includes a power-on reset circuit. When the chip is initially energized a signal called $\overline{POR}$ is brought out of the analog chip and goes to the $\overline{PORI}$ pin of the digital processor. This signal causes the modem to assume a valid operational state. The $\overline{POR}$ pin is activated any time the +5V supply drops below +3.5V for more than 30 msec.

The analog signal processor timing signal is provided from the digital processor. The crystal frequency for the digital chip is 19.6608MHz. This clock, after being divided by two, provides a 9.8304MHz clock to the CLK_{IN} pin of the analog chip. To operate in all possible modes, the analog chip requires a 9.792MHz clock. This clock is generated internally by deleting one clock out of 256 clock pulses of the 9.8304MHz clock. *The clock rate is critical in facsimile synchronous operation and should be within 50ppm.*

Receive Filter

The receive filter in V.29, V.27ter, Voice, G2, G1 and tone mode consists of a low-pass filter that extends from 300-3200Hz. The low-pass filter is a 7th order elliptic filter. The 300 Hz high-pass filter is 3rd order. For full duplex applications a band-pass filter is required to reject the adjacent band by 60dB. A second filter is included on the chip, which has a seventh order high-pass characteristic. The pass band edge is 2000Hz and stopband edge is 1600Hz. By combining the 7th order low-pass and high-pass

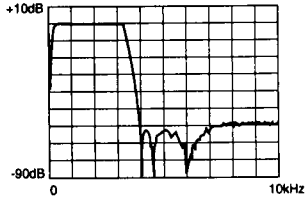


Figure 2a. Overall Frequency Response (V.29, V.27, V.33, V.17, G2 (Rx), G1, TONE/VOICE)

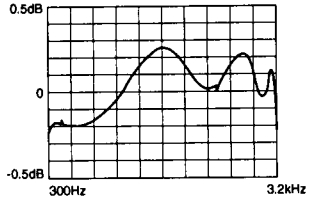


Figure 2b. Details of Passband (V.29, V.27, V.33, V.17, G2 (Rx), G1, TONE/VOICE)

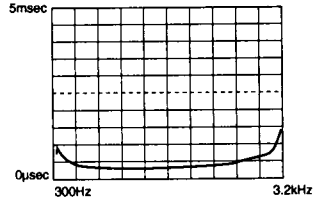


Figure 2c. Passband Group Delay (V.29, V.27, V.33, V.17, G2 (Rx), G1, TONE/VOICE)

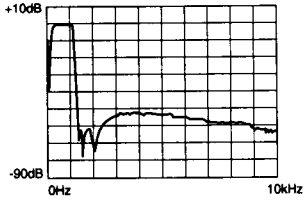


Figure 3a. Overall Frequency Response (G2 (Tx))

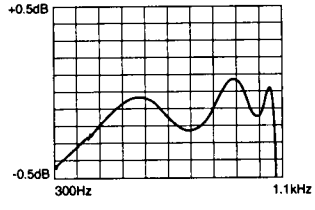


Figure 3b. Detail of Passband (G2 (Tx))

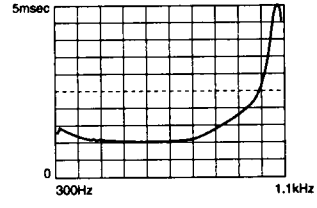


Figure 3c. Passband Group Delay (G2 (Tx))

Figure 4a. Overall Frequency Response (CPM/V.23BC/V.26A)

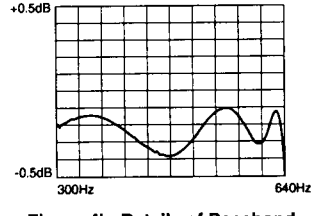


Figure 4b. Details of Passband (CPM/V.23BC)

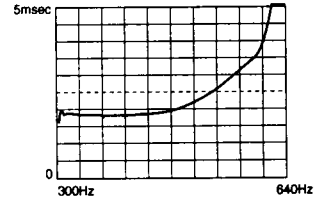


Figure 4c. Passband Group Delay (CPM/V.23BC)

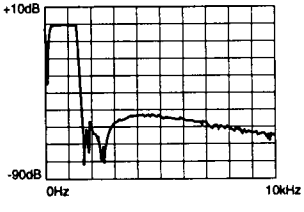


Figure 5a. Overall Frequency Response (V.21A)

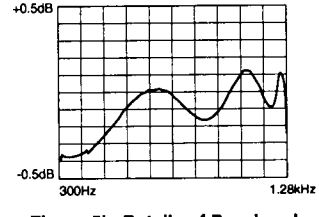


Figure 5b. Details of Passband (V.21A)

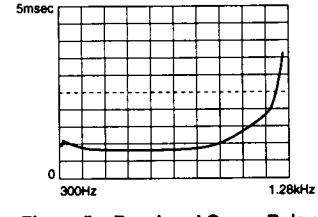


Figure 5c. Passband Group Delay (V.21A)

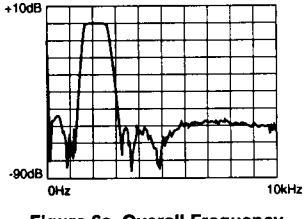


Figure 6a. Overall Frequency Response (V.21O)

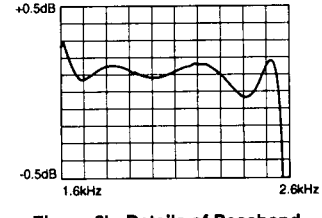


Figure 6b. Details of Passband (V.21O)

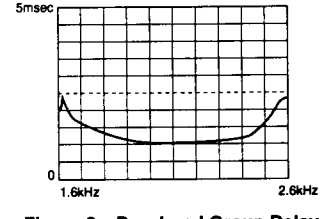


Figure 6c. Passband Group Delay (V.21O)

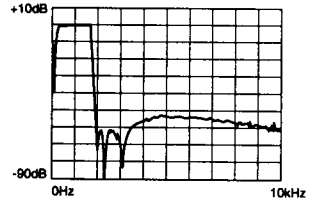


Figure 7a. Overall Frequency Response (103A)

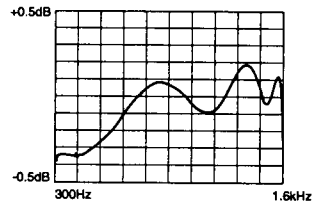


Figure 7b. Details of Passband (103A)

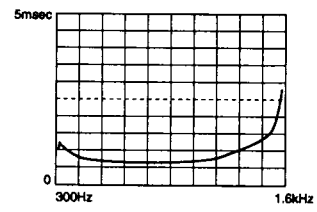


Figure 7c. Passband Group Delay (103A)

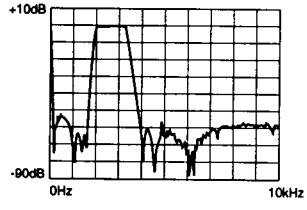


Figure 8a. Overall Frequency Response (103O)

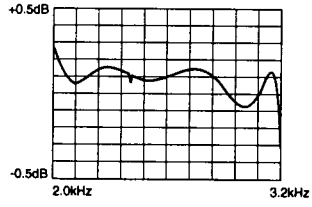


Figure 8b. Details of Passband (103O)

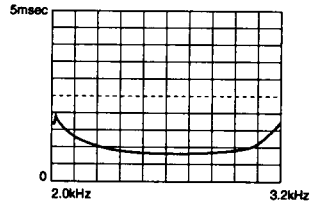


Figure 8c. Passband Group Delay (103O)

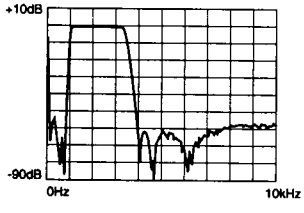


Figure 9a. Overall Frequency Response (V.23FC/V.26O)

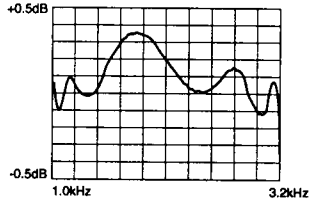


Figure 9b. Details of Passband (V.23FC)

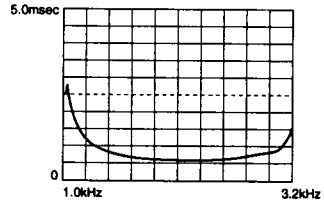


Figure 9c. Passband Group Delay (V.23FC)

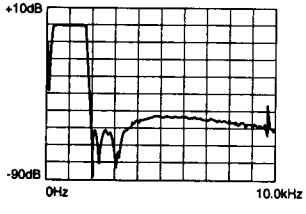


Figure 10a. Overall Frequency Response (V.22A)

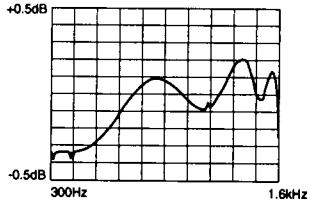


Figure 10b. Details of Passband (V.22A)

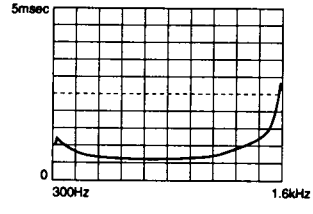


Figure 10c. Passband Group Delay (V.22A)

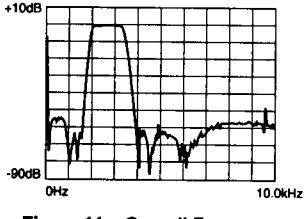


Figure 11a. Overall Frequency Response (V.22O)

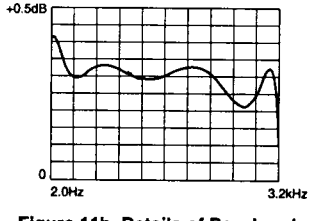


Figure 11b. Details of Passband (V.22O)

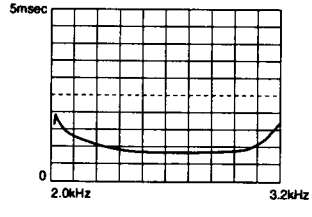


Figure 11c. Passband Group Delay (V.22O)

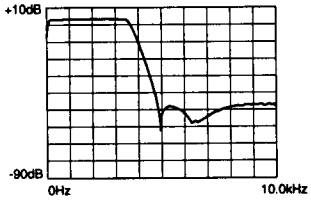


Figure 12a. Overall Frequency Response (Transmit)

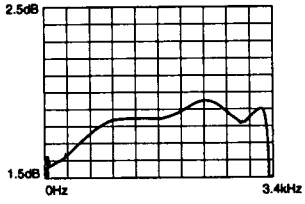


Figure 12b. Details of Passband (Transmit)

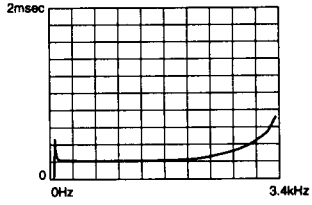


Figure 12c. Passband Group Delay (Transmit)

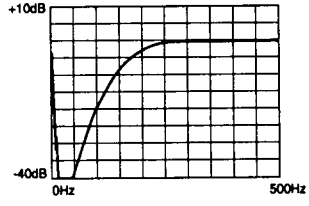


Figure 13. Highpass Response (300 Hz)

filters, several different filter configurations can be realized, which can be used as a bandsplit filter.

The overall frequency response and the group delay of the various high-band and lowband filters for different modes of operation are shown in Figures 2 through 13.

Cable Equalizers

The cable equalizer is a second order biquad which uses programmable capacitors to incorporate three distinct compromise amplitude line characteristics shown in Table 1.

These equalizers are predominantly used in the G3 mode of the facsimile modem. However, it is possible to take advantage of these characteristics to implement the required compromise amplitude equalizers in the V.22bis mode. In this mode, the low-band has a flat characteristic and the high-band directly changes by 2dB over an 800Hz band from 2000 to 2800Hz. The cable equalizer, when set in the code 2 mode, has a gain of 0.9dB at 2000Hz and 2.7dB at 2800Hz. The differential gain in 2.7-0.9 = 1.8dB, which is adequate for the high-band equalizer. The flat gain however at 2400Hz is 2.0dB which will result in some change in the transmit output level. To compensate for this change in level, when the cable equalizer is activated, the transmit amplitude is reduced by approximately 2.0dB at the transmitter output. When the modem is configured to operate in a full-duplex mode (V.22, V.22bis, 103, V.23, 212A, and V.21) and the cable equalizer is activated (CABS1=1 or CABS2=1) the control logic will force the cable select to the code 2 mode (CABS1=0 and CABS2=1).

FREQUENCY (Hz)	Gain Relative to 1700Hz(dB)			
	CODE 1	CODE 2	CODE 3	
700	-0.86	-2.36	-4.22	CABS1 = 1 Code 1, CABS2 = 0
1500	-0.22	-0.58	-1.04	CABS1 = 0 Code 2, CABS2 = 1
2000	0.35	0.91	1.61	
3000	1.41	2.95	4.33	CABS1 = 1 Code 3, CABS2 = 1

Table 1. Cable Equalizer Characteristics

Constellation DAC

The XDIS and YDIS pins are driven by the same DAC that generates the transmit S/H signal, thus the x-y display capability is available only when the transmitter is not used. The update of the x-y display can be controlled through the interface by the transmit or receive strobe. The constellation display needs to be updated only once per symbol period. In the case of the transmit strobe (9600 or 10368Hz) the XDIS and YDIS are written once every sample period. For the receive strobe, which is equal to the symbol rate, the x and y displays are written once every strobe period.

An XDIS and YDIS written into the chip within a given strobe period will appear two strobes later. If neither x nor y is written to the chip the x and y displays will hold their previous values and will not be updated. If only one value (x or y) is written into the chip, both x and y display will be updated. The display whose value was not changed will be updated according to the previous code in the corresponding register. When x and y displays are active, the transmitter will be squelched. It will be activated after the CON/TX bit is reset and the first transmit strobe that includes a transmit data. At that time x and y display will be squelched.

The constellation display capability can be used to display the transmit or receive constellation patterns and constellation patterns.

V.22bis Parallel Data Mode

In the V.22bis mode when the TXSEL2–TXSEL0 bits are set to TXSEL2 = 1 and TXSEL1 = TXSEL0 = 0, the modem enters the parallel data mode. In this mode, the transmit register (REG 6, A2 = A1 = 1, A0 = 0) is used to pass the transmit data from the DSP chip to the ana-

log chips. Since the processor is timed by the receive strobe, the analog chip should provide synchronization means between the asynchronous transmit clock and receive strobes. This synchronization is achieved by the TX buffer empty (TXBE) bit which is communicated to the DSP chip through the receive serial output interface. The analog chip transmits the TX data serially from the TX serial register. This register is clocked by the TX clock. After 8 bits have been shifted out and transmitted, the control logic loads 8-bits of new data into the TX serial register from the TX buffer register and resumes the transmission. In the meantime, it also sets the TXBE bit and sends it to the digital chip on the occurance of the next receive strobe. The digital chip should fill the transmit buffer before the 8-bits in the transmit serial register are shifted out.

Receive Serial Output Interface

During G3, V.22bis, V.22 and 212A modes, the serial interface on the analog chip transfers four sets of 16 bit data to the digital signal processor. The first 12 bits constitute the receive base band signal I and Q mid or end baud sample and the remaining bits are status information. The last 2 LSBs of the receive sample are also multiplexed with two other status bits under the control of the ERM bit in the transmit status registers. The format of the receive data is shown in Figure 14 and the output serial interface timing is shown in Figure 15.

In other modes of operation (103, V.21, V.23 and tone receive), the ADC takes only one sample from the band pass signal and transfers it to the digital processor through the serial interface. The serial output interface logic based on the control bits, programs the interface to one or four serial shifts during a receive strobe.

Transmit Serial Input Interface

The transmit and control data are transferred to the analog chip through a serial interface. When a data transfer is initiated by the digital signal processor, the SIEN signal goes high and stays high during the falling edge of the serial shift clock. This event activates the serial interface to accept data. The digital signal processor, during every data transfer, passes 16 bits of data to the analog chip. The first three bits are the address bits, the next 13 bits are the data/control bits. In the case of transmit data, the 12 bits after the three bit address are relevant, and the last bit is don't care. The logic in the serial input interface catches the first sixteen bits that shift into the analog chip and separate the address and data bits to load them into the appropriate registers. Figure 16 shows the serial input interface timing and Table 2 shows the register format.

V.26bis Mode

The V.26bis mode supports two distinct data rates: 2400 bit/s and a fallback mode of 1200 bit/s. V.26bis also supports a back channel of 75 bit/s FSK or 150 bit/s FSK. This allows support of Cellular Data Link Control (CDLC) and Racal VoData modes.

Voice Modes

Voice transmit and receive sample rates of 11,000, 9600, 8000, 7307 s/s are provided for compatibility with a variety of voice and sound sources and compression methods. 12 bit linear samples in both directions provide high quality audio signalling with simultaneous DTMF detection using Sierra's voice DSP comparison chips. Input filters are adjusted to suit the sample rate.

Ring Detect Input

The ring detect input is provided as an input pin to the analog processor. The input to this pin after passing through a first order lowpass filter which serves as a deglitching circuit, passes a comparator with hysteresis. The output of the comparator is brought to the output interface logic. In the normal mode, the 16-bit interface register has no extra bits to transfer the data corresponding to the Ring Detect input to the DSP chip. This problem is solved by modifying the data input to the interface register in the CPM mode, where the 1850 and 1650 detect bits are substituted by the Ring Detect output and the chip identification bit. The Ring Detect feature is therefore available in the CPM mode only. Two options are available for the Ring Detector. The first option corresponds to an external Ring Detector circuit which indicates the presence of the Ring input by pulling the $\overline{RD}$ pin to a low level. In the second option the Ring Detection is done in the DSP chip by counting the period of the alternating ringing input signal and comparing it to a preset value which can be modified by writing into the interface RAM. The Ring Detector circuit is shown in Figure 1.

Power Down Mode

In addition to the normal power down mode which puts the chip in complete powerdown, two new power down modes are supported which can be used for Caller ID. The two new modes are only operational during the time when the powerdown bit is activated and the chip has entered powerdown. In this mode when the chip is put in CPM powerdown mode 1, the Ring Detect circuit will be powered up and it will monitor the Ring Detect input pin. Once this pin makes a high to low transition, the serial interface will be powered up and upon the occurrence of the next RXSTRB the serial interface data will be transferred to the DSP chip. The data transfer will continue for as long as the Ring Detect input is kept low. The CPM powerdown mode 2 is basically the same as mode 1 except that the Ring Detect circuit and the serial interface will stay high regardless of the state of the Ring Detect input pin and will

continue to transfer data to the DSP chip for as long as the chip is kept in this mode. CPM powerdown mode 1 is useful in Caller ID mode where an external Ring Detect circuit is implemented and the presence of the ringing signal is indicated to the analog chip by pulling the Ring Detect pin low. Mode 2 is useful where Ring Detection should be done by validating the frequency of the ringing signal. The serial interface during CPM powerdown mode 1 and mode 2 will operate like the CPM mode. If the powerdown bit is not activated both CPM powerdown mode 1 and mode 2 will operate like the CPM mode. This minimizes power consumption during ring qualification, thus optimizing battery life.

Transmit Output High Impedance Mode

When the control bit corresponding to this mode is activated, the operational amplifier that drives the transmitter output will be put in a high impedance mode. This will effectively cause one end of the terminating resistor to float so that if the coupling transformer is AC coupled to the telephone line, it will not cause the line to be terminated. This will be useful in monitoring the line during a voice call for recording or call waiting signal detection.

Caller ID Mode

The chip has several new features that will allow the Caller ID feature to be implemented in a more effective way. Two relay drivers are provided, one for the offhook switch and the other for the Caller ID mode. An external Ring Detect circuit indicates the presence of the ringing signal by a high to low transition of the signal applied to the $\overline{RD}$ pin. During Caller ID the power down bit will be activated and the chip will be configured in the CPM powerdown mode 1. Once a ringing signal comes in that cuases the external ring detector to pull the $\overline{RD}$ pin low, the on chip ring detector will activate the serial interface and transfer the data corresponding to the presence of the ringing signal to the DSP chip. The DSP chip will wake up and will set the analog chip in the CPM powerdown mode 2, and will continue monitoring the state of the $\overline{RD}$ pin. Once the ringing goes away and the $\overline{RD}$ signal is pulled high, the DSP chip will wait for a predetermined period, after which time it will put the modem in the Caller ID mode (Bell 202) and will also activate the $\overline{CIDRC}$ signal. This will turn on the relay which will in turn connect the telephone line to the coupling transformer through a series resistor capacitor combination., This action will AC couple the telephone line to the Receive input without going off-hook. The modem will activate a timer and will look for the energy detect to be activated. Once the energy is detected the 202 demodulator will start the demodulation process. If energy is not detected and the timer expires, the modem will turn the relay off before the next high voltage ringing signal response.

RECEIVED DATA & CALL PROGRESS STATUS OUTPUT REGISTER

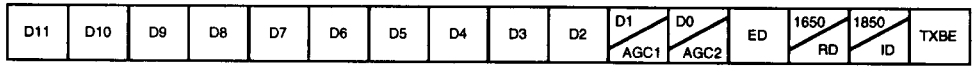


Figure 14. Format of Serial Output

Bit Number	Bit Name	Description
0	TXBE	Trasmit Buffer empty bit. This bit is set by the analog chip when the control logic loads the transmit serial register with eight bits of data from the transmit buffer register. It gets reset when the processor writes a new set of data into the TX buffer register.
1	1850/ID	Non-CPM Mode: 1850 Hz tone detection output. CPM Mode: 0 = SC11092, 1 = SC11094
2	1650/RD	Non-CPM Mode: 1650 Hz tone detection output. CPM Mode: 1 = Ring signal detected
3	ED	Energy detect output
4	D0*/AGC2	ERM = 0: AGC2 – Gain of 1 bit AGC2 AGC2 = 0: Gain is 0 dB in receiver AGC2 = 1: Gain is 9.54 dB in receiver ERM = 1: D0 – data bit
5	D1*/AGC1	ERM = 0: AGC1 – Gain of 1 bit AGC1 AGC1 = 0: Gain is 0 dB in receiver AGC1 = 1: Gain is 12.0 dB in receiver ERM = 1: D1 – data bit
6–15	D2–D11*	10 bit receive data sample.

NOTE: When ERM = 1, D0–D11 make up 12 bit receiver data samples in two's complement format.

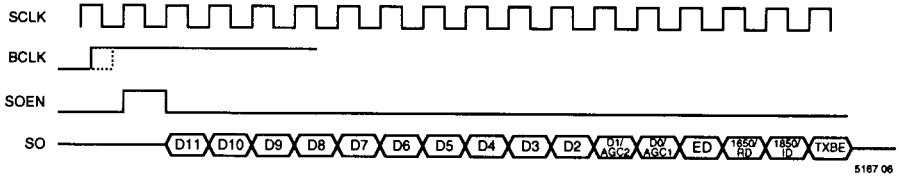
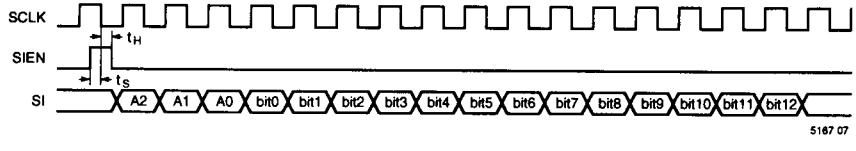


Figure 15. Serial Output Interface Timing



$A_2 - A_0$ Destination Address
$bit_0 - bit_{12}$ Thirteen control/data bits
t_s Set up time from enable high to serial clock low 50ns
t_h Hold time from serial clock low to enable low 50ns

Figure 16. Serial Input Interface Timing

Bit / Reg.	12	11	10	9	8	7	6	5	4	3	2	1	0
0	D3	D2	D1	D0	G8	G7	G6	G5	G4	G3	G2	G1	G0
1	PD	EDLVL	HYBRON	AGCFR	AGCTH	GEX2	G2I/$\overline{E}$	G1SEL	GEX1	G1I/$\overline{E}$	AUZ	CABS2	CABS1
2	TEST1	TEST2	AUDIO	RX0	ERM	ALB	TDEN	A/$\overline{O}$	M4	M3	M2	M1	M0
3	OHRC	ALC0	ALC1	1800/$\overline{550}$	TONEON	DL	TXSEL2	TXSEL1	TXSEL0	TL3	TL2	TL1	TL0
4	CIDRC	TX2	PA3	PA2	PA1	PA0	CON R/$\overline{T}$	CON/$\overline{TX}$	TDPLLJ	TDPLL INT/$\overline{EXT}$	TDPLL LOCK/$\overline{FREE}$	TX1	TX0
5	—	—	TEST0	TEST3	SYNC	DISS	RNGX	WLS1	WLS0	RDPLL SP1	RDPLL SP0	RDPLL1	RDPLL0
6	—	DX11	DX10	DX9	DX8	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0
7	—	DY11	DY10	DY9	DY8	DY7	DY6	DY5	DY4	DY3	DY2	DY1	DY0

Table 2. Input Register Allocation

CONTROL/DATA REGISTERS

Register 0 Address (A2-A0) = 000

Bit Number	Bit Name	Description
0–8	G0–G8	Programmable gain control bits. These bits control the 512 step, 0.106 dB/step programmable gain control according to the following table. The PGC has -9.03dB (1/2√2) flat gain.

G8	G7	G6	G5	G4	G3	G2	G1	G0	GAIN (dB)
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0.106
0	0	0	0	0	0	0	1	0	0.212
0	0	0	0	0	0	1	0	0	0.424
0	0	0	0	0	1	0	0	0	0.848
0	0	0	0	1	0	0	0	0	1.696
0	0	0	1	0	0	0	0	0	3.392
0	0	1	0	0	0	0	0	0	6.784
0	1	0	0	0	0	0	0	0	13.568
1	0	0	0	0	0	0	0	0	27.136

9–12	D0–D3	Four bits received data. Used only in V.22bis (2400 or 1200 bit/s) mode. These are descrambled received data bits transfered from the signal processor to the analog chip for sync-to-async conversion. D0 is the first bit appearing on the RXDATA pin after sync-to-async conversion, followed by D1, D2 and D3. In the 1200 bit/s mode, only D0 and D1 are shifted out during one baud period while D2 and D3 are ignored.

CONTROL/DATA REGISTERS (continued)

Register 1 Address (A2–A0) = 001

Bit Number	Bit Name	Description
0–1	CABS1, CABS2	To minimize the impact of local loop high frequency rolloff, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion. The following two tables illustrate the change in filter response caused by enabling each of the compromise equalizers independently.

CABS2	CABS1	LENGTH OF 0.4mm DIAMETER CABLE	
0	0	0.0	(code 0)
0	1	1.8km	(code 1)
1	0	3.6km	(code 2)
1	1	7.2km	(code 3)

	GAIN RELATIVE TO 1700Hz (dB)		
FREQUENCY (Hz)	CODE 1	CODE 2	CODE 3
700	-0.86	-2.36	-4.22
1500	-0.22	-0.58	-1.04
2000	0.35	0.91	1.61
3000	1.41	2.95	4.33

2	AUZ	Receive Auto-zero. When set, the input of the demodulator is grounded, this can be used to store the DC offset voltages of the I, Q and bandpass channels that can be cancelled by the controller. AUZ = 0 normal mode AUZ = 1* auto-zero mode The only exception is in CPM mode (CPM = 1) where AUZ controls the ADC input signal. For AUZ = 0 the input is taken from the hybrid output and for AUZ = 1 the input is taken from the PGC output.
3	G1I/$\overline{E}$	9dB front-end hybrid gain controlled internally by the 1 bit AGC1, or externally by the processor. G1I/$\overline{E}$ = 1 internal G1I/$\overline{E}$ = 0 external
4	GEX1	9dB hybrid gain controlled by the processor. Effective only when G1I/$\overline{E}$ = 0. GEX1 = 1 12dB gain GEX1 = 0 0 dB gain
5	G1SEL	Controls the selection of the input to the 1 bit AGC1 between the hybrid output or the output of receive filter. G1SEL = 1 Use output of hybrid as input to AGC1. G1SEL = 0 Use output of receive filter as input to AGC1.
6	G2I/$\overline{E}$	3dB front-end low-pass gain controlled internally by the 1 bit AGC2, or externally by the processor. G2I/$\overline{E}$ = 1 internal G2I/$\overline{E}$ = 0 external
7	GEX2	3dB receive low-pass filter gain controlled by the processor. Effective only when G2I/$\overline{E}$ = 0. GEX2 = 1 9.5dB gain GEX2 = 0 0dB gain
8	AGCTH	1 bit AGC threshold control. AGC1 AGC2 AGCTH = 0 narrow window 0.15V–0.72V 0.2V–0.6V AGCTH = 1 wide window 0.15V–1.4V 0.2V–1.0V Initially this bit is zero. After the handshaking is complete the bit can be set to one.

CONTROL/DATA REGISTERS (continued)

9	AGCFR	Freeze 1 bit AGC so that it will not react to amplitude changes. AGCFR = 1 Freeze AGCFR = 0 Active
10	HYBRON	Turn hybrid on, used in full duplex mode to cancel hybrid echo. HYBRON = 1 Turn hybrid on HYBRON = 0 Turn hybrid off
11	EDLVL	Energy detect level control. EDLVL= 1 -43dBm on, -48dBm off EDLVL= 0 -47dBm on, -52dBm off Energy detect level control in voice mode. EDLVL= 1 -47dBm on, -52dBm off EDLVL= 0 -54dBm on, -59dBm off
12	PD	Power down mode. PD = 1 Power down PD = 0 Power up

Register 2 Address (A2–A0) = 010

Bit Number	Bit Name	Description
0–4	M0–M4	Modem Mode Control

MODE	M4	M3	M2	M1	M0	SIGNAL NAME	RXCLK	RXSTRB	TXCLK	TXSTRB	CARRIER
V.29 9600	0	1	1	1	1	V29	9600	2400	9600	9600	1700
V.29 FB1 7200	0	1	1	1	0	V29F1	7200	2400	7200	9600	1700
V.29 FB2 4800	0	1	1	0	1	V29F2	4800	2400	4800	9600	1700
V.27 4800	0	1	1	0	0	V27	4800	1600	4800	9600	1800
V.27 FB 2400	0	1	0	1	1	V27F	2400	1200	2400	9600	1800
V.33 14400	0	1	0	1	0	V33	14400	2400	14400	9600	1800
V.33FB 12000	0	1	0	0	1	V33F	12000	2400	12000	9600	1800
G2(RX)/G1(TX/RX)	0	1	0	0	0	G2/G1	10368	10368	10368	10368	X
G2(TX)	0	0	1	1	1	G2TX	10368	10368	10368	10368	X
Tone Mode	0	0	1	1	0	TM	9600	9600	9600	9600	X
CPM Normal	0	0	1	0	1	CPMN	9600	9600	9600	9600	X
CPM Powerdown mode 1	1	0	0	1	0	CPMPD1	9600	9600	9600	9600	X
CPM Powerdown mode 2	1	0	0	1	1	CPMPD2	9600	9600	9600	9600	X
V.21	0	0	1	0	0	V21	9600	9600	300	9600	X
103	0	0	0	1	1	103	9600	9600	300	9600	X
V.23/202	0	0	0	1	0	C23/CID	9600	9600	1200	9600	X
V.22bis 2400	0	0	0	0	1	V22HS	2400	600	2400	9600	A/$\overline{O}$ = 1 2400 A/$\overline{O}$ = 0 1200
V.22bis 1200	0	0	0	0	0	V22LS	1200	600	1200	9600	A/$\overline{O}$ = 1 2400 A/$\overline{O}$ = 0 1200
V.26bis 2400 A/$\overline{O}$ = 0	1	0	0	0	1	V26	2400	1200	9600	9600	1800
A/$\overline{O}$ = 1							9600	9600	2400	9600	
V.26bis 1200 A/$\overline{O}$ = 0	1	0	0	0	0	V26F	1200	1200	9600	9600	1800
A/$\overline{O}$ = 1							9600	9600	1200	9600	
Voice Mode 9600	1	0	1	0	0	VM9600	9600	9600	9600	9600	X
Voice Mode 8000	1	0	1	0	1	VM8000	9600	8000	9600	8000	X
Voice Mode 7307	1	0	1	1	0	VM7307	9600	7307	9600	7307	X
Voice Mode 11027	1	0	1	1	1	VM11027	9600	11027	9600	11027	X

5	A/$\overline{O}$	When set, the modem operates in answer mode/backward channel for V.23; when clear it operates in originate mode/forward channel for V.23. This bit is active only in V.22bis, V.22, V.23, V.21 and 103 modes. In other modes the state of this bit is ignored.

CONTROL/DATA REGISTERS (continued)

6	TDEN	Tone detector enable, detects the presence of 1850Hz or 1650Hz tones while doing V.29 or V.27 demodulation. The output of the tone detector is presented to the signal processor for flag detection. TDEN = 1 enabled TDEN = 0 disabled
7	ALB	Analog loop back. When set, the transmitter output is connected to the receive path. The receive filter clocks are adjusted accordingly to place the signal in the pass-band of the filters. ALB = 1 enabled ALB = 0 disabled
8	ERM	Extended receive mode. When this bit is low, the two LSB's of the 12 bit ADC are substituted with AGC1 and AGC2 status bits. When the ERM is high, the full 12 bit ADC output is available. ERM = 0 D0 is substituted with AGC2. D1 is substituted with AGC1. ERM = 1 Full 12 bit is available.
9	RX0	This signal controls the input of the receive filter. When set, the input of the receive filter is connected to ground. When reset, it allows the selected signal by the ALB control bit to be applied to the receive filter input.
10	AUDIO	Audio output control. When set, the signal at the RX_{IN} pin, after passing through the receive antialiasing filter, is brought out to the AUX_{OUT} pin. When reset, the output signal to the AUX_{OUT} pin is controlled by the TEST1 and TEST2 bits. When the audio bit is set, TEST1 and TEST2 are ignored.
11–12	TEST2, TEST1	These two bits put the modem in a test mode according to the following table.

AUDIO	TEST1	TEST2	FUNCTION
1	x	x	Connect RX_{IN} to AUX_{OUT}
0	0	0	Squelch AUX_{OUT} (connect AUX_{OUT} to analog ground).
0	0	1	Connect I channel output to AUX_{OUT}.
0	1	0	Connect Q channel output to AUX_{OUT}.
0	1	1	Connect output of receive filter to AUX_{OUT}. It also connects RX_{IN} to input of ADC

Register 3 Address (A2-A0) = 011

Bit Number	Bit Name	Description
0–3	TL0–TL3	Transmit level adjust bits based on the following table.

TL3	TL2	TL1	TL0	LOSS (dB)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	1	0	0	4
1	0	0	0	8

CONTROL/DATA REGISTERS (continued)

4–6	TXSEL0–TXSEL2	Transmit select bits. These three bits are active during V.22bis and V.22 modes. In all other modes they are ignored. They determine the data transmitted by the transmitter according to the following table.

TXSEL2	TXSEL1	TXSEL0	TRANSMITTED DATA
0	0	0	External data sent by DTE.
0	0	1	Unscrambled S1 (Note 1).
0	1	0	Unscrambled Space.
0	1	1	Unscrambled Mark.
1	0	0	Transmit Parallel mode.
1	0	1	Scrambled Reversal (Note 2).
1	1	0	Scrambled Space.
1	1	1	Scrambled Mark.

Note 1: S1 is a pattern 0011 transmitted at 1200 bit/s rate regardless of speed (2400 or 1200 bit/s). This pattern can not be sent at 2400 bit/s. **Note 2:** Reversals are continuous streams of 01.

7	DL	Digital loop back. In this mode the descrambled receive data is sent back to the scrambler followed by the transmitter. The modem will automatically go to the synchronous mode with slave timing. Digital loop back overrides all other modes of operation.
8–9	TONEON, 1800/$\overline{550}$	These two bits are used to control the frequency of the synthesized sine wave according to the following table. They are only valid in V.22bis/V.22 modes. In other modes, the tone generator will be turned off and the programmable counters will stop to minimize noise. The summer input will be connected to ground.

TONE ON	1800/$\overline{550}$	TONE OUT
0	0	Off
0	1	2225 KHz
1	0	550 Hz
1	1	1800 Hz

10–11	ALC1–ALC0	Audio level control bits. These two bits are used to control the audio level at the $AUDIO_{OUT}$ pin according to the following table.

ALC1	ALC0	AUDIO ATTENUATOR
0	0	Audio Off
0	1	12dB
1	0	6dB
1	1	0dB

The audio signal can be amplified by 12dB by the hybrid gain control before being fed to the audio attenuator.

12	OHRC	Off-Hook Relay Control (OHRC) is a control bit for open drain output designed to drive directly a +5V relay coil with a worst case resistance of 360 ohms and operating voltage of +4.0VDC across coil. A clamp diode integrated in the chip eliminates the need for a diode across the relay coil. An external transistor can be used to drive heavier loads (e.g. electromechanical relays).

Register 4 Address (A2–A0) = 100

Bit Number	Bit Name	Description
0–1	TX0–TX1	Transmit output control. These two bits control the transmit output signal. The transmit buffer sums the output of the 16-step attenuator and the signal at the AUXTX pin according to the following table:

TX1	TX0	SIGNAL AT TX_{OUT} PIN
0	0	Squelch Transmitter
0	1	Transmit Signal from attenuator
1	0	AUXTX Signal
1	1	Transmit signal from attenuator + AUXTX signal

CONTROL/DATA REGISTERS (continued)

2–3 TDPLLLock/$\overline{\text{Free}}$, TDPLL INT/$\overline{\text{EXT}}$

Transmit phase-locked loop control bits.

TDPLL Lock/$\overline{\text{Free}}$	TDPLL INT/$\overline{\text{EXT}}$	FUNCTION
0	x	Transmit phase locked loop in free running mode.
1	1	Transmit clock locked to recovered receive clock.*
1	0	Transmit clock locked to external clock.

*The slave mode is only possible in the full duplex V.22bis or V.22 mode.

4 TDPLLJ

Transmit PLL Jam. Reset the transmit DPLL on the next rising edge of the locking clock.

TDPLLJ = 1 Jam Activated
TDPLLJ = 0 Jam Deactivated.

When, TDPLLJ bit is set, the transmit DPLL will continue to be reset on every rising edge of the locking clock. It will resume the phase locked loop action as soon as the TDPLLJ bit is reset.

5 CON/$\overline{\text{TX}}$

Constellation pattern/transmit mode control bit. This bit configures the transmit DAC to operate either in the constellation pattern monitor or normal transmit mode.

CON/$\overline{\text{TX}}$ = 1 Constellation pattern mode.
CON/$\overline{\text{TX}}$ = 0 Transmit mode.

6 CON R/$\overline{\text{T}}$

Constellation pattern monitor strobe selector. It selects the update strobe for the constellation DAC.

CON R/$\overline{\text{T}}$ = 1 Use receive strobe for constellation DAC.
CON R/$\overline{\text{T}}$ = 0 Use transmit strobe for constellation DAC.

7–10 PA0–PA4

Receive DPLL phase adjustment control. The receive timing recovery circuit works as an independent block and extracts the receive clock from the receive signal band edge component. The rising edge of the recovered clock is coincident with the center of the baud interval. The center of the baud however, is not necessarily the best sampling point of the baseband signal. In some instances, based on the line conditions, the sampling point can be advanced or retarded to improve performance. The four bits PA3-PA0 are used to do this phase adjustment. PA3 controls the direction, and PA2-PA0 control the amount of the phase change.

PA3	PA2	PA1	PA0	V.29, V.17	V.17fb	V.27	V.27fb	V.22bis
1	0	0	0	0	0	0	0	0
1	0	0	1	-6°	-9°	-4°	-6°	-5.6°
1	0	1	0	-15°	-18°	-10°	-15°	-11.2°
1	0	1	1	-21°	-27°	-14°	-21°	-16.8°
1	1	0	0	-30°	-36°	-20°	-30°	-22.4°
1	1	0	1	-36°	-45°	-24°	-36°	-28°
1	1	1	0	-45°	-54°	-30°	-45°	-33.6°
1	1	1	1	-51°	-63°	-34°	-51°	-39.2°
0	0	0	0	0	0	0	0	0
0	0	0	1	9	9°	6°	9°	5.6°
0	0	1	0	15	18°	10°	15°	11.2°
0	0	1	1	24	27°	16°	24°	16.8°
0	1	0	0	30	36°	20°	30°	22.4°
0	1	0	1	39	45°	26°	39°	28°
0	1	1	0	45	54°	30°	45°	33.6°
0	1	1	1	54	63°	36°	54°	39.2°

11 TX2

When set, the transmit output is deselected and placed in a high impedance state.

12 CIDRC

Caller ID Relay Control (CIDRC) is a control bit for open drain output designed to drive directly a +5V relay coil with a worst case resistance of 360 ohms and operating voltage of +4.0 VDC across coil.

CONTROL/DATA REGISTERS (continued)

Register 5 Address (A2-A0) = 101

Bit Number	Bit Name	Description
0–1	RDPLL0, RDPLL1	Receive DPLL control. These bits control the receive DPLL according to the following table.

RDPLL1	RDPLL0	MODE
0	0	Free Running
0	1	JAM
1	0	Activate Hangup Detector
1	1	Normal

When the Jam mode is activated, the receive DPLL will be reset on every rising edge of the incoming clock, and it will continue to do so until the Jam mode is removed. In modes where phase locking is not needed, namely, G1, G2, Tone, CPM, V.21 and 103, the DPLL is disabled.

2–3	RDPLL SP0, RDPLL SP1	Receive DPLL speed control. These two bits control the adjustment speed and hence the filter performance of the receive DPLL according to the following table.

RDPLL SP1	RDPLL SP0	SPEED
0	0	Fast mode. Insert 8 clocks per baud period.
1	0	Slow 1 mode. Insert 1 clock per baud period.
0	1	Slow 2 mode. Insert 1 clock per 2 baud period.
1	1	Slow 2 mode.

The receive DPLL band-widths are shown for different speeds in the table below

Mode / Baud Rate	SLOW 2*	SLOW1	FAST
2400Hz	±0.0245% Correction = ±204 nsec	±0.049% Correction = ±204 nsec	±0.392% Correction = ±1.63 µsec
1600Hz**	±0.01634% Correction = ±204 nsec	±0.0327% Correction = ±204 nsec	±0.262% Correction = ±1.634 µsec
1200Hz	±0.0245% Correction = ±408 nsec	±0.049% Correction = ±408 nsec	±0.392% Correction = ±3.268 µsec
600Hz	±0.0244% Correction = ±814 nsec	±0.049% Correction = ±814 nsec	±0.391% Correction = ±6.51 µsec

* In slow 2 mode, correction will be integrated over two baud periods. Therefore, the maximum effective correction (average per baud) will be half of the numbers given in the slow 1 column of the DPLL.

** Slow 2 mode should not be used for the 1600 baud rate, because the DPLL bandwidth is below the ±0.02% required by the CCITT spec.

4–5	WLS0, WLS1	Word length select bits in asynchronous mode according to the following table:

WLS1	WLS0	NUMBER OF BITS PER CHARACTER
1	0	8
1	1	9
0	0	10
0	1	11

6	RNGX	Range extender for the receiver sync/async converter. When set, the receiver sync/async can insert up to one stop bit per four (8, 9, 10 or 11-Bit) characters to compensate for a far end DTE being up to 2.3% over-speed. In this mode the inserted stop bit will have 3/4 of the length of a normal bit. When reset, one stop bit with 7/8 of the length of a normal bit can be inserted per eight characters. The transmitter async/sync converter always handles this overspeed condition regardless of the state of this bit.

CONTROL/DATA REGISTERS (continued)

7	DISS	When this bit is set, the V.22bis scrambler is disabled, when cleared it is enabled. Transmit select bits (TXSEL0-2) override this bit when in "Transmit internal mode".
8	SYNC	This bit is used in the V.22bis and 212A modes only. It controls the operation of the async-to-sync and sync-to-async converters. When set, the modem operates in synchronous mode; when reset, it operates in character asynchronous mode. When in digital loop-back mode, the modem will be forced into the synchronous mode.
9	TEST3	This bit, when set, puts the transmit side of the chip in a test mode. It disconnects the inputs of the I and Q pulse shaping filters from the data encoder and connects both inputs to TXD pin. The outputs of the pulse shaping filter will be connected to XDIS and YDIS S/H inputs. This allows the filters to be tested independently. It also forces the four bits from the I and Q encoders to a state that forces the highest gain for the filter with a positive polarity. TEST3 bit, when set, also connects the output of the async-to-sync converter to the input of the sync-to-async converter. This will facilitate the easy testing of the above two blocks.
10	TEST0	This bit activates a test mode. When set, the output of the receive antialiasing filter is connected to the transmit low-pass filter and allows it to be tested. When reset, the modem resumes its normal operation.
Register 6 and Register 7 Address (A2-A0) = 110, 111		These two 12bit registers transfer data from the signal processor to the digital-to-analog converter. In normal transmit mode, REG6 contains the transmit data and the contents of REG7 is ignored. In constellation mode, REG6 and REG7 contain the constellation x and constellation y components respectively. In V.22bis parallel mode REG6 contains the TX data bits.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6 V
DC Input Voltage (Analog Signals)	-0.6 to V_{DD} +0.6 V
DC Input Voltage (Digital Signals)	-0.6 to V_{DD} +0.6 V
Storage Temperature Range	-65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 Sec.)	300°C

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.
NOTE 2: Unless otherwise specified, all voltages are referenced to ground.
NOTE 3: Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

OPERATING CONDITIONS

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0	25	70	°C
V_{DD}	Positive Supply Voltage		4.5	5.0	5.5	V
A_{GND}, D_{GND}	Ground		-0.5	0	0.5	V
f_C	Clock Frequency			9.8304		MHz
t_R, t_F	Input Rise or Fall Time	All digital inputs except CLK_{IN}		100	500	ns
t_R, t_F	Input Rise or Fall Time	CLK_{IN}		5.0	20	ns

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{DD} = +5V ± 10%, V_{SS} = -0V)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Quiescent Current	Normal		20	30	mA
I_{DD} PD	Quiescent Current	Power Down Mode		5.0		mA
V_{IH}	High Level Input Voltage; Digital pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital pins				0.8	V
V_{OH}	High Level Output (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Output (I_{OL} = 1.6 mA)				0.6	V
VXTA	Maximum Peak Output Level at TX_{OUT} pin in other modes	V_{DD} = +5 V	2.5	3.0		V_{PP}
	Maximum QAM Signal Level in V.22bis/V.22 mode at TX_{OUT} pin	V_{DD} = +5 V	-7.0	-6.0	-5.0	dBm
VXRA	Maximum Peak Input Level at RX_{IN} pin	V_{DD} = +5 V			3.0	V_{PP}

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
All Modes except voice	EDC = 1.0 µF; measured at RX_{IN} PGC = 0 dB				
Energy detect level (ED low to high)		-45	-44	-43	dBm
Loss of energy detect level (ED high to low)	EDLVL = 1	-48	-47	-46	dBm
Hysterisis		2.0	3.0	5.0	dB
Voice Mode					
Energy detect level (ED low to high)		-49	-48	-47	dBm
Loss of energy detect level (ED high to low)		-52	-51	-50	dBm
Hysterisis		2.0	3.0	5.0	dBm

Programmable Gain Controller (PGC)

Gain step size		0.05	0.1	0.15	dB
Dynamic range		53	54	55	dB
Response time (from change in PGC register to output of A to D converter)			1.0	1.5	ms

TYPICAL APPLICATIONS

System Description

This analog processor is designed to work with the Sierra SC11088 series DSP, to implement a facsimile plus data modem. The modem will satisfy the telecommunication requirements specified in CCITT recommendations V.29, V.27ter and G3 for half duplex facsimile applications and V.22 bis, V.22, Bell 212, V.23, V21 and Bell 103 for full duplex data applications. Additionally the modem has single and dual tone generation modes. The dual tone modes can be used for DTMF dialing. It also has single and dual tone detection modes, where the dual tone detector will be restricted to the DTMF tones, and can be used as a DTMF receiver. The analog chip supports several auxiliary functions, such as programmable attenuators, audio output with level control constellation pattern monitoring etc.

The analog processor has been designed to support operation according to CCITT recommendations V.33, V.26 and V.17, also, with a suitable DSP chip.

The modem functional interconnect diagram is shown in Figure 16. System hardware circuits provide address (RS0-RS3), control ($\overline{CS}$, Read and Write) and interrupt IRQ signals for implementing a parallel interface. The system has two modes of operation, parallel and serial. In the parallel mode, the modem can transfer channel data 8 bits at a time via the microprocessor bus. The serial modem uses standard V.24 (RS-232-C compatible) signals to transfer channel data. In V.29, V.27ter, G2, G1, V.23; V.21 and 103 modes, where the transmit modulation is done in the digital signal processor, the transmit data can be provided to the modem through either the parallel or serial interface. In V.22bis, V.22 and 212A modes, the transmit data is provided to the analog chip serially through its TXD pin. The transmitter modulator, in these modes, is implemented in the analog processor and it can only take data serially. V.22bis, V.22 and 212A support asynchronous mode as well as the synchronous mode of operation. Therefore, included on the analog signal processor, is an async-to-sync converter. During reception, for the V.29, V.27ter, V.23, V.21, 103, G2 and G1 modes, the demodulation is done completely in the digital signal processor. In the asynchronous mode, however, the demodulated and descrambled modem data from the digital signal processor is fed back to the analog processor for sync-to-async conversion. The hardware sync-to-async converter makes the recovered data available on the RXDATA pin, which is connected to the $RXDATA_{IN}$ pin on the digital signal precessor. This signal is multiplexed with the receive signal from the digital processor, and under the software control provides the final output to the RXD pin.

The MAC (controller) can be driven by the clock output of the DSP chip so that only one crystal is needed.

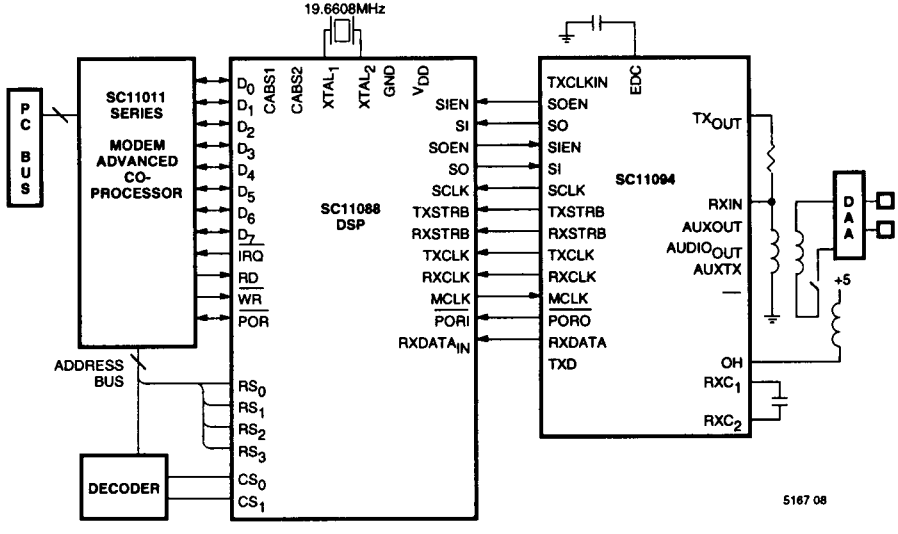


Figure 16. Simplified Block Diagram

OPERATING MODES

The following operating modes are available.

Half-Duplex Modes

Group 3 modes (for facsimile)

V.29 – 9600	Send or Receive
V.29 – 7200	Send or Receive
V.29 – 4800	Send or Receive
V.27 – 4800	Send or Receive
V.27 – 2400	Send or Receive

Full-Duplex Modes

V.26bis – 2400/75	Forward and Backward Channel
V.26bisFB – 1200/75	Forward and Backward Channel
V.22bis – 2400	Send or Receive
V.22bis – 1200	Send or Receive
V.22 – 1200	Send or Receive
212A – 1200	Send or Receive
V.21 – 300	Send or Receive
103 – 300	Send or Receive
V.23 – 1200/75	Forward and backward channel
tone transmission	Single frequency and DTMF
tone detection	Three tones simultaneously and DTMF reception

In addition to the above modes, three special full duplex modes are supported:

1. Tone detection (462Hz and 1100Hz) and G2 transmission.
2. Tone detection (1650 and 1850Hz) and G3 transmission. This feature is used to detect the presence of an HDLC FLAG (7EHEX) during G3 transmission.
3. Call progress (190–650 Hz), programmable tone detection and calling tone generation (1100 Hz, 1300 Hz)

The following bit rate and modulation schemes will be provided when used with a suitable Sierra DSP IC (SC11066, SC11077 or SC11088).

MODE	RATE (BITS/S)	MODULATION SCHEME	SYMBOL RATE (BAUD/SEC)	CARRIER (Hz)	COMMUNICATION TYPE
V.29	9600	16-pt QAM	2400	1700	Half-Duplex
V.29 FB1	7200	8-pt QAM	2400	1700	Half-Duplex
V.29 FB2	4800	4-pt QAM	2400	1700	Half-Duplex
V.27ter	4800	8-pt DPSK	1600	1800	Half-Duplex
V.27ter FB	2400	4-pt DPSK	1200	1800	Half-Duplex
V.22bis	2400	16-pt QAM	600	2400/1200	Full-Duplex
V.22bis	1200	4-pt QAM	600	2400/1200	Full-Duplex
V.21	300	FSK	300	1750/1080	Full-Duplex
V.22	1200	4-pt DPSK	600	2400/1200	Full-Duplex
Bell 212A	1200	4-pt DPSK	600	2400/1200	Full-Duplex
Bell 103	300	FSK	300	2125/1170	Full-Duplex
G2(CCITT T3)	10368	AM-VSIS	10368	2100	Half-Duplex
G1(CCITT T2)	10368	FSK	10368	1950	Half-Duplex
V.23 Forward V.23 Backward	0-1200 0-75	FSK	1200 75	1300/2100 390/450	Half-Duplex Full-Duplex
V.33/V.17	14,400	64 QAM	2400	1800	Half-Duplex
V.33FB1/V.17 FB	12000	32 QAM	2400	1800	Half-Duplex
V.26bis Forward V.26bis Backward	2400 0-75	4-pt DPSK FSK	1200 75	1800 390/450	Full-Duplex
V.26bis FB Forward V.26bis FB Backward	1200 0-75	2-pt DPSK FSK	1200 75	1800 390/450	Full-Duplex

Table 5. Summary of Modulation Methods