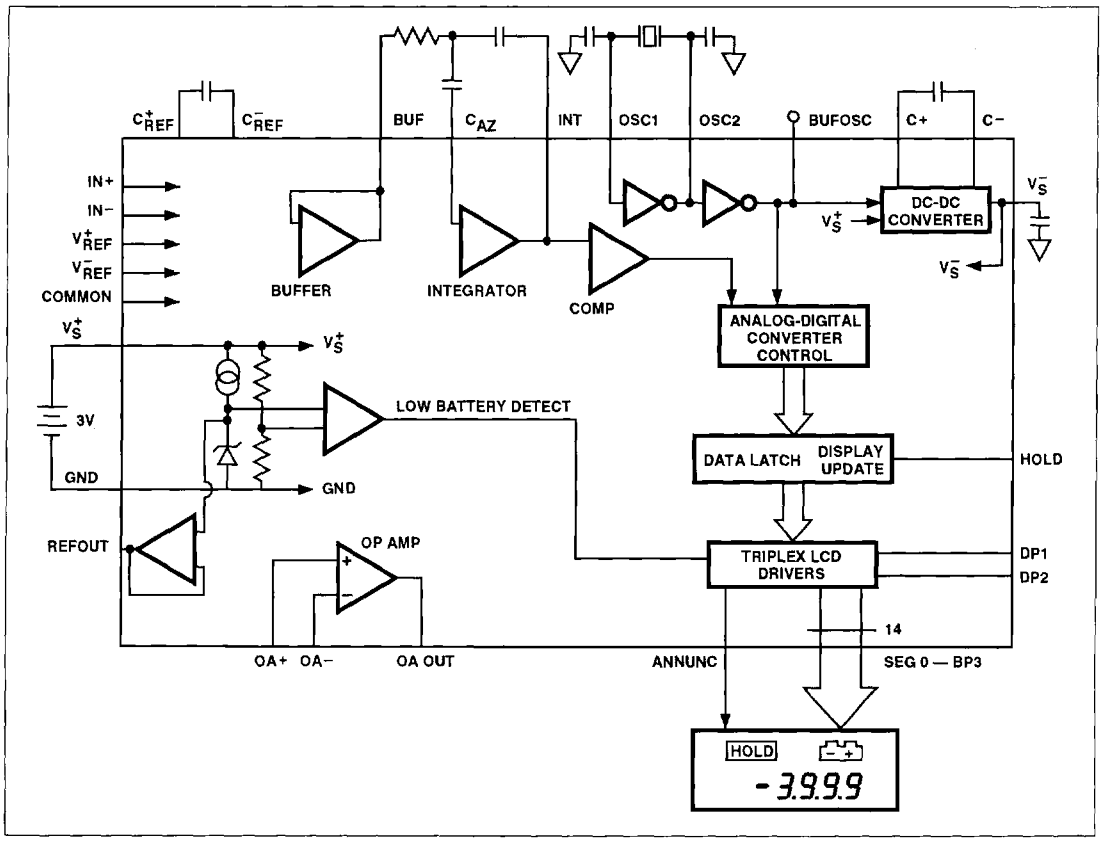
3-3/4 DIGIT LCD ANALOG TO DIGITAL CONVERTER

FEATURES

- 3-3/4 Digit (3999 maximum) Resolution
- 3V Battery Operation
  - On-Chip DC-to-DC Converter
- Low Power Operation
  - Supply Current 400 µA Typical
- Differential Signal Inputs
- Differential Reference Inputs
- LCD with Triplexed drive
  - 3-3/4 Digit Resolution
  - 3 Decimal Points
  - LCD Annunciator Driver Output
  - Low-battery and Hold Annunciators
- Op-amp for AC-to-DC Converter
- Display HOLD with LCD Annunciator
- Low-battery Detect with LCD Annunciator
- On-chip Band-gap Reference
- Crystal Oscillator
- 40-Pin DIP or 44-Pin Flat Package

FUNCTIONAL DIAGRAM



TC822
TC823

GENERAL DESCRIPTION

The TC822 is a 3-3/4 digit LCD analog-to-digital converter ADC which operates from a single 3V battery. Product designs utilizing the TC822 offer higher performance, lower parts count and smaller size than 7106-based designs, while the 3V battery permits a wide variety of packaging options.

All active components necessary to construct a 0.025% resolution measurement system are included on the TC822. Only external resistors and capacitors, an LCD and a battery are required.

The TC822 includes features which must be added externally with ADCs such as the 7106. LCD decimal point drivers, low-battery detection, and data hold function with LCD annunciator are all on chip. No external exclusive-OR gates are required. An operational amplifier, which can be used for an AC-to-DC converter or resistance measurement current source, is also included.

Differential signal inputs with 1 pA leakage simplify system design. Differential reference inputs permit ratiometric measurements, while retaining the data HOLD function. Either the internal 1.3V band-gap reference or an external reference can be used.

The TC822 LCD drive includes 3-3/4 digits, decimal points, and HOLD and low-battery annunciators. The triplexed LCD requires only 14 interconnects, which increases reliability and simplifies mechanical design.

Package options include a 40-pin DIP and 44-pin plastic leaded chip carrier (PLCC), and compact flat packages. The many on-chip features of the TC822, combined with the compact flat package and 3V battery, permit the design of very small, high quality, economical instruments.

The TC823 offers all the features of the TC822, but with a resolution of 3-1/2 digits.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_S^+ to GND) .... +4.7V
Analog Input Voltage (either input) .... V_S^+ to V_S^-
(Note 1)
Reference Input Voltage (either input) .... V_S^+ to V_S^-
Op Amp Input Voltage (either input) .... V_S^+ to V_S^-
Digital Inputs .... V_S^+ to GND
Power Dissipation, Plastic Package .... 800 mW
Operating Temperature Range
C Devices .... 0°C to +70°C
E Devices .... -40°C to +85°C
Storage Temperature Range .... -65°C to +150°C
Lead Soldering Temperature (10 sec) .... +300°C

NOTES:
1. Input voltages may exceed the supply voltages provided that input current is limited to ±100 µA. Current above this value may result in invalid display readings but will not destroy the device if limited to ±1 mA.
2. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.
3. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.
4. Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields.

ORDERING INFORMATION

Part No.	Resolution Digits	44-Pin Plastic Flat Package	44-Pin Plastic Leaded Chip (PLCC)	40-Pin Plastic DIP	Temperature Range
TC822CKW	3-3/4	X			0°C to +70°C
TC822CLW	3-3/4		X		0°C to +70°C
TC822CPL	3-3/4			X	0°C to +70°C
TC822EKW	3-3/4	X			–40°C to +85°C
TC822ELW	3-3/4		X		–40°C to +85°C
TC822EPL	3-3/4			X	–40°C to +85°C
TC823CKW	3-1/2	X			0°C to +70°C
TC823CLW	3-1/2		X		0°C to +70°C
TC823CPL	3-1/2			X	0°C to +70°C
TC823EKW	3-1/2	X			–40°C to + 85°C
TC823ELW	3-1/2		X		–40°C to +85°C
TC823EPL	3-1/2			X	–40°C to + 85°C

ELECTRICAL CHARACTERISTICS: V_S = 3.0 V, T_A = 25° C, Figure 1 Test Circuit

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Input						
	Zero Input Reading	V_{IN} = 0.0V Full-Scale = 400 mV	–0000	0000	+0000	Digital Reading
RE	Roll-Over Error	V_{IN} = ±390 mV Full-Scale = 400 mV	–1	±0.2	+1	Counts
NL	Non-Linearity (Max Deviation from Best Straight Line Fit)	Full-Scale = 400 mV	–1	±0.2	+1	Count
	Ratiometric Reading	V_{IN} = V_{REF}	1999	1999/ 2000	2000	Digital Reading
E_N	Noise (p-p value not exceeded 95% of time)	V_{IN} = 0.0V Full-Scale = 400 mV	—	15	—	µV
I_{IN}	Input Leakage Current	V_{IN}= 0.0 V T_A = 25°C 0°C ≤ T_A ≤ +70°C –40°C ≤ T_A ≤ +85°C	 — — —	 — 20 100	 10 100 250	 pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±0.2V, V_{IN} = 0.0 V Full-Scale= 400 mV	—	50	—	µV/V
V_{CMR}	Common-Mode Voltage Range	Input High, Input Low V_{IN} = 0.0V, Full-Scale = 400 mV	GND –0.5	—	GND +0.5	V
TC_{ZS}	Zero Reading Drift	V_{IN} = 0.0V 0°C ≤ T_A ≤ +70°C –40°C ≤ T_A ≤ +85°C Ext. Ref. 0 ppm/°C	 — —	 0.2 1	 — —	 µV/°C
TC_{FS}	Scale Factor Temperature Coefficient	V_{IN} = 399 mV 0°C ≤ T_A ≤ +70°C –40°C ≤ T_A ≤ +85°C Ext. Ref. 0 ppm/°C	 — —	 ±1 ±5	 ±5 ±25	 ppm/°C
	Input Voltage Range	V_{IN}^+, V_{IN}^- Normal Mode + Common-Mode Voltage	GND –0.5	—	GND +0.5	V
Reference						
V_{REF}	Reference Voltage	I_L = 25 µA (V_{REF}-GND)	1.25	1.3	1.45	V
TCV_{REF}	Reference Voltage Temperature Coefficient	0°C ≤ T_A ≤ +70°C	—	50	—	ppm/°C
Op-Amp						
V_{IOA}	Op-Amp Input Offset Voltage	V_S = 3V	—	±10	—	mV
	Op-Amp Input Voltage Range		—	±2	—	V
	Op-Amp Unity Gain Frequency		—	0.6	—	MHz
	Op-Amp Output Voltage Swing	R_L = 100 kΩ to GND	—	±2.5	—	V
	Op-Amp Slew Rate	R_L = 100 kΩ to GND, CL = 50 pF	—	1	—	V/µs

ELECTRICAL CHARACTERISTICS (Cont.): $V_S = 3.0$ V, $T_A = 25°$ C, Figure 1 Test Circuit

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Digital						
V_{IL}	Input Low Voltage	DP1, DP2, HOLD	—	—	GND +0.5	V
V_{IH}	Input High Voltage	DP1, DP2, HOLD	$V_S^+ -0.5$	—	—	V
	Control Pin Pulldown Current	$V_{IN} = V_S^+$	—	3	—	μA
	LCD Drive Voltage	$2V \leq V_S^+ \leq 4V$	3.1	3.2	3.3	V p-p
Power Supply						
I_S	Supply Current	$V_{IN} = 0.0V$ $V_S^+ = 3.0$ V	—	400	600	μA
	Supply Operating Voltage Range	V_S^+ to GND	2	—	4	V
	Low-Battery Flag Voltage	V_S^+ to GND	2.15	2.25	2.45	V

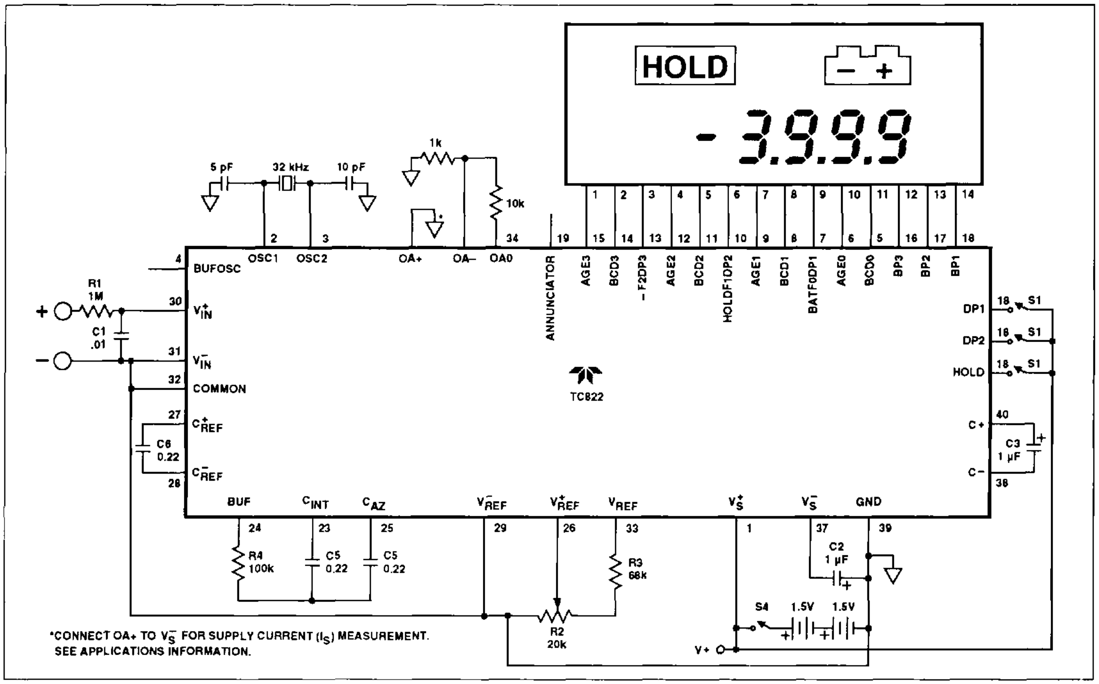
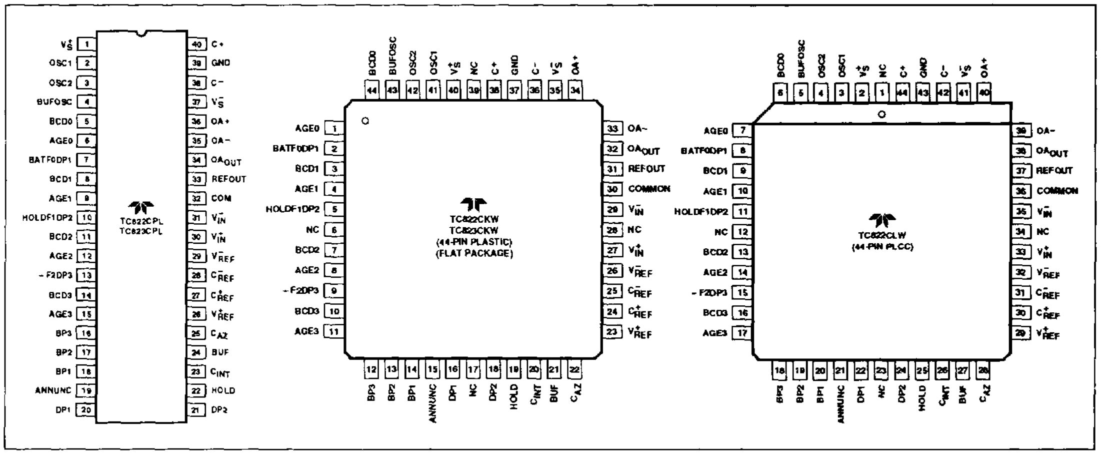


Figure 1 Test Circuit

3-3/4 DIGIT LCD ANALOG TO DIGITAL CONVERTER

TC822 TC823

PIN CONFIGURATIONS



PRELIMINARY PIN DESCRIPTION AND FUNCTION, TC822 3-3/4 DIGIT A-D CONVERTER, 3V OPERATION

Pin No. (40-Pin Package)	Symbol	Description
1	V_S^+	Positive battery supply connection. Typically 3V.
2	OSC1	Oscillator connection.
3	OSC2	Oscillator connection.
4	BUFOSC	Buffered oscillator output.
5	BCD0	LCD segment drive for 'b', 'c', and 'd' segments of least significant digit (LSD).
6	AGE0	LCD segment drive for 'a', 'g', and 'e' segments of LSD.
7	BATF0DP1	LCD segment drive for LOW-BATTERY, 'f' segment of LSD, and decimal point 1.
8	BCD1	LCD segment drive for 'b', 'c', and 'd' segments of 2nd LSD.
9	AGE1	LCD segment drive for 'a', 'g', and 'e' segments of 2nd LSD.
10	HOLDF1DP2	LCD segment drive for 'data hold', 'f' segment of 2nd LSD, and decimal point 2.
11	BCD2	LCD segment drive for 'b', 'c', and 'd' segments of 3rd LSD.
12	AGE2	LCD segment drive for 'a', 'g', and 'e' segments of 3rd LSD.
13	–F2DP3	LCD segment drive for 'polarity', 'f' segment of 3rd LSD, and decimal point 3.
14	BCD3	LCD segment drive for 'b', 'c', and 'd' segments of most significant digit (MSD).
15	AGE3	LCD segment drive for 'a', 'g', and 'e' segments of MSD.
16	BP3	LCD backplane #3.
17	BP2	LCD backplane #2.
18	BP1	LCD backplane #1.
19	ANNUNC	Square wave output at the backplane frequency, synchronized to BP1. ANNUNC can be used to control display annunciators. Connecting an LCD segment to ANNUNC turns it on; connecting it to its backplane turns it off.
20	DP1	Decimal Point select input.
21	DP2	Decimal Point select input.
22	HOLD	Hold input. Connecting this pin to V_S^+ will 'freeze' the LCD.

PRELIMINARY PIN DESCRIPTION AND FUNCTION, TC822 3-3/4 DIGIT A-D CONVERTER, 3V OPERATION (Cont.)

Pin No. (40-Pin Package)	Symbol	Description
23	C_{INT}	Integrator output. Connect to integration capacitor.
24	BUF	Buffer output. Connect to integration resistor.
25	C_{AZ}	Autozero capacitor connection.
26	V_{REF}^+	High differential reference input connection.
27	C_{REF}^+	Positive connection for reference capacitor.
28	C_{REF}^-	Negative connection for reference capacitor.
29	V_{REF}^-	Low differential reference input connection.
30	V_{IN}^+	High analog input signal connection.
31	V_{IN}^-	Low analog input signal connection.
32	COM	Analog circuit ground reference point.
33	REFOUT	Output of 1.3V voltage reference.
34	OA_{OUT}	Output of uncommitted operational amplifier.
35	OA-	Inverting input of uncommitted operational amplifier.
36	OA+	Noninverting input of uncommitted operational amplifier.
37	V_S^-	Output of DC-to-DC converter. Connect a 1 µF capacitor from this pin to power ground.
38	C–	Capacitor connection for DC-to-DC converter.
39	GND	Power ground.
40	C+	Capacitor connection for DC-to-DC converter.

FEATURES

The TC822 and TC823 are high-resolution analog-to-digital converters which include all of the active components required to build a typical digital multimeter or other measurement instrument. The on-chip op-amp can be configured as a sensor amplifier, AC-to-DC converter, or resistance measurement current source. The LCD includes decimal points, low-battery detection, and data hold annunciators. A DC-to-DC converter permits operation from a single 3V battery. With on-chip voltage reference and LCD drive circuitry, the TC822 simplifies the design of multi-mode measurement instruments.

The TC822 has a resolution of 3-3/4 digits (3999, maximum) while the TC823 has a resolution of 3-1/2 digits (1999, maximum). The features of both converters are the same, so that both 3-3/4 digit and 3-1/2 digit designs can be produced with only one basic design. The differences between the TC822 and the TC823 primarily affect system timing, and are noted in the ADC System Timing section of the data sheet.

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

The TC822 ADC operates on the principle of dual-slope integration. An understanding of the dual-slope conversion technique will aid the user in following the detailed TC822 theory of operation following this section. A conventional dual-slope converter measurement cycle has two distinct phases:

1) Input Signal Integration
2) Reference Voltage Integration (Deintegration)

Referring to Figure 2, the unknown input signal to be converted is integrated from zero for a fixed time period (t_{INT}), measured by counting clock pulses. A constant reference voltage of the opposite polarity is then integrated until the integrator output voltage returns to zero. The reference integration (deintegration) time (t_{DEINT}) is then directly proportional to the unknown input voltage (V_{IN}).

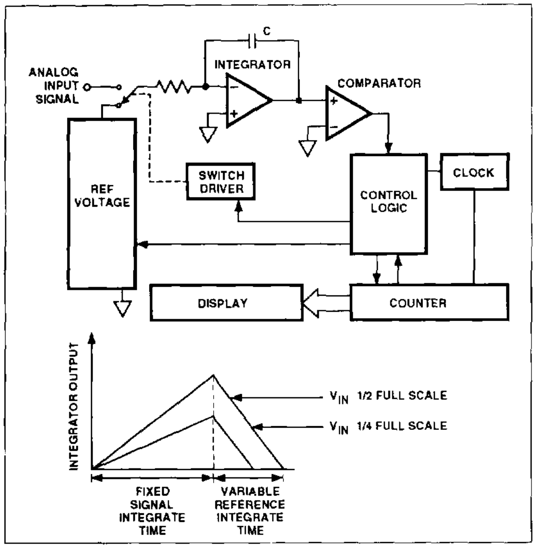


Figure 2 Basic Dual-Slope Converter

In a simple dual-slope converter, a complete conversion requires the integrator output to 'ramp-up' from zero and 'ramp-down' back to zero. A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{R_{INT} C_{INT}} \int_0^{t_{INT}} V_{IN}(t)dt = \frac{V_{REF} t_{DEINT}}{R_{INT} C_{INT}}$$

where: V_{REF} = Reference Voltage
t_{INT} = Integration Time
t_{DEINT} = Deintegration Time

For a constant T_{INT}:

$$V_{IN} = V_{REF} \bullet \frac{t_{DEINT}}{t_{INT}}$$

Accuracy in a dual-slope converter is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. An inherent benefit of the dual-slope technique is noise immunity. Noise spikes are integrated, or averaged, to zero during the integration periods, making integrating ADCs immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals, with frequency components at multiples of the averaging (integrating) period, will be attenuated (see Figure 3). Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period.

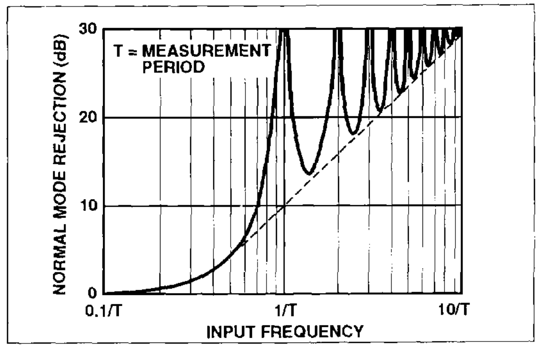


Figure 3 Normal-Mode Rejection of Dual-Slope Converter

TC822 ADC THEORY OF OPERATION

Analog Section

In addition to the basic integrate and deintegrate dual-slope phases discussed above, the TC822 design incorporates a 'Zero Integrator Output' phase and an 'Auto Zero' phase. These additional phases ensure that the integrator starts at zero volts (even after a severe over-range conversion) and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

1) Zero Integrator Output Phase
2) Auto Zero Phase
3) Signal Integrate Phase
4) Reference Deintegrate Phase

Zero Integrator Output Phase

This phase guarantees that the integrator output is at zero volts after an overrange input occurs. Thus, the next reading after an overranged reading will be correct. The ZI phase duration varies from 0 to 600 counts.

Auto Zero Phase

During the Auto Zero phase, the differential input signal is disconnected from the measurement circuit by opening internal analog switches and the internal nodes are shorted to Analog Common (0 volt ref) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator to permit comparator offset voltage error compensation. A voltage established on C_{AZ} then compensates for internal device offset voltages during the measurement cycle. The Auto Zero phase residual is typically 10 to 15 μV. The Auto Zero duration is 1600 counts, plus the ZI counts if an overrange did not occur, plus unused deintegration counts. Thus, the AZ phase can occupy from 1600 to 6000 counts (600 to 3000 counts for TC823).

Signal Integration Phase

Upon completion of the Auto Zero phase, the Auto Zero loop is opened and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is then integrated for a fixed time period, which in the TC822 is 2000 counts (4000 clock periods) and in the TC823 is 1000 counts (4000 clock periods). The externally set clock frequency is divided by two (TC822) or four (TC823) before clocking the internal counters. The integration time period is:

$$t_{INT} = \frac{4000}{f_{OSC}}$$

Note that, for the same clock frequency, the TC822 and TC823 will have the same signal integration time. Therefore, the noise rejection performance of the two converters will be the same.

Polarity is determined at the end of signal integration phase. The sign bit is a 'true polarity' indication in that signals less than 1 LSB are correctly determined. This allows precision null detection which is limited only by device noise and Auto Zero residual offsets.

Reference Integrate (Deintegrate) Phase

The reference capacitor, which was charged during the Auto Zero phase, is connected to the input of the integrating amplifier. The internal sign logic insures that the polarity of the reference voltage is always connected in the phase which is opposite to that of the input voltage. This causes the integrator to ramp back to zero at a constant rate which is determined by the reference potential.

The amount of time required (t_{DEINT}) for the integrating amplifier to reach zero is directly proportional to the amplitude of the voltage that was put on the integrating capacitor (V_{INT}) during the integration phase:

$$t_{DINT} = \frac{R_{INT} \bullet C_{INT} \bullet V_{INT}}{V_{REF}}$$

The digital reading displayed by the TC822 is:

$$\text{Digital Count} = 2000 \bullet \frac{V_{IN}^+ - V_{IN}^-}{V_{REF}}$$

For the TC823, the digital reading displayed is:

$$\text{Digital Count} = 1000 \bullet \frac{V_{IN}^+ - V_{IN}^-}{V_{REF}}$$

ADC System Timing

The oscillator frequency is divided by 2 (4 for TC823) prior to clocking the internal decade counters. The four phase measurement cycle takes a total of 8000 (4000) counts or 16000 (16000) clock pulses. The 8000 (4000) count phase is independent of input signal magnitude or polarity.

Each phase of the measurement cycle has the following length:

Conversion Phase	TC822	TC823	
1) Auto Zero	1600 to 5999	600 to 2999	Counts
2) Signal Integrate*	2000	1000	Counts
3) Reference Integrate	1 to 4000	1 to 2000	Counts
4) Integrator Output Zero	0 to 400	0 to 400	Counts

* This time period is fixed. The integration period for the TC822 is:

$$t_{INT\,(TC822)} = \frac{4000}{f_{OSC}} = 2000 \text{ Counts}$$

For the TC823, the integration period is:

$$t_{INT\,(TC823)} = \frac{4000}{f_{OSC}} = 1000 \text{ Counts}$$

where f_{OSC} is the clock oscillator frequency.

ANALOG PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs (V_{IN}^+, V_{IN}^-)

The TC822 is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The maximum input voltage range, which includes normal-mode + common-mode signals, is ±0.5V.

Common-mode voltages are removed from the system when V_{IN}^- is connected to Analog Common. The TC822's on-chip DC-to-DC converter eliminates most common-mode difficulties and permits measurements where measurement and power grounds cannot be isolated. (see Figure 4)

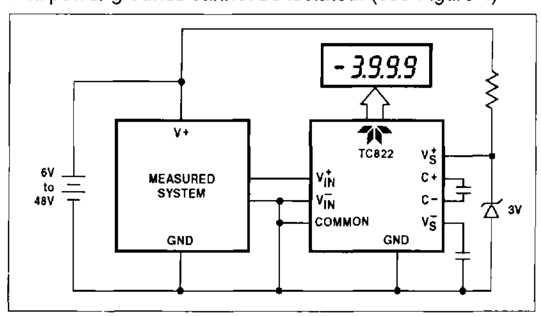


Figure 4 DC-to-DC Converter Permits Ground Referenced Measurements

Common-mode voltages with respect to power GND do, however, affect the integrator output level. The user must be particularly careful that the integrator does not saturate when at minimum battery voltage. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 5). For such applications the integrator output swing can be reduced below the recommended 1.5V full-scale swing. The integrator output will swing within 0.3V of V_S^+ or V_S^- without increased linearity error.

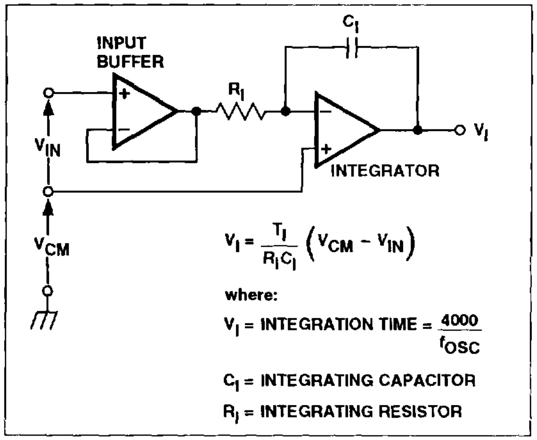


Figure 5 **Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)**

Reference Inputs (V_{REF}^+, V_{REF}^-)

The TC822 reference, like the analog signal input, has true differential inputs. In addition, the reference voltage can be generated anywhere within the power supply voltage of the converter. The differential reference inputs permit ratiometric measurements and simplify interfacing with sensors such as load cells and temperature sensors.

Reference Output (REFOUT)

This pin is the buffered output of the internal CMOS band-gap reference. The output voltage is typically 1.3V above power GND, with a load current of 25 µA. The temperature coefficient of REFOUT is typically 50 ppm/°C.

Analog Common

The TC822 connects the internal V_{IN}^+ and V_{IN}^- inputs to Analog Common during the Auto Zero cycle. During the reference integrate phase V_{IN}^- is connected to Analog Common. If V_{IN}^- is not externally connected to Analog Common, a common-mode voltage exists. This is rejected by the converter's 86 dB common-mode rejection ratio. In battery powered applications, Analog Common and V_{IN}^- are usually connected, removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, Analog Common should be connected to V_{IN}^-.

The Analog Common pin serves to set the analog section reference or common point. The TC822 is specifically designed to operate from a battery or in any measurement system where input signals are referenced to the TC822 power source, so Analog Common is normally connected to power GND.

DIGITAL PIN FUNCTIONAL DESCRIPTION

DP1, DP2

These inputs control the LCD decimal points. The decimal point truth table is shown in Table 1. These inputs have internal 3 µA pulldowns to DGND.

Table 1 TC822 Decimal Point Truth Table

Decimal Point DP2	Inputs DP1	LCD
0	0	3999
0	1	399.9
1	0	39.99
1	1	3.999

Hold

HOLD can be used to hold or 'freeze' the display. Connecting this pin to V_S^+ inhibits the display update process. Conversions will continue, but the display will not change.

APPLICATIONS INFORMATION

Power Supplies

The TC822 is designed to operate from a 3V battery, but will operate over a range of 2.0 to 4.0V. An on-chip DC-to-DC converter converts the +3V supply to –3V, which permits bipolar input voltages to be converted. Measurements are referenced to battery ground, so that the TC822/823 are ideal for applications such as measuring battery voltage, battery charging current, etc.

Op-Amp Power Supply Current

The op-amp of the TC822 has a low-distortion class A output, which is biased at 100 µA. To reduce supply current when the op-amp is not being used, connect the non-inverting input to V_S^-, as shown in Figures 6 and 11. When the op-amp is used, supply current will increase by about 200 µA.

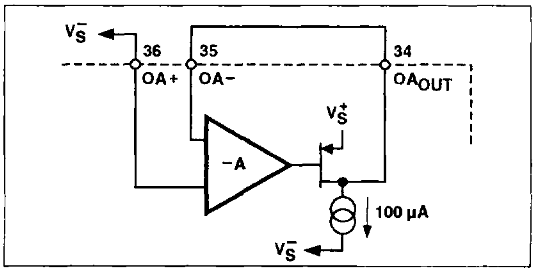


Figure 6 Simplified Op-Amp Output Schematic

Clock Oscillator

The crystal oscillator circuit is shown in Figure 7. An inexpensive 32.768 kHz watch crystal gives about 27 dB noise rejection at 60 Hz, while a 40 kHz crystal (used in ultrasonic alarms) will almost totally reject 50 and 60 Hz noise.

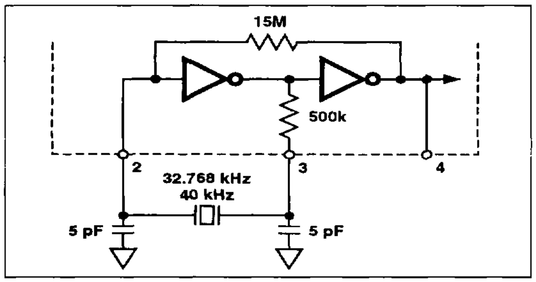


Figure 7 Crystal Oscillator Circuit

System Clock

All system timing is derived from the clock oscillator. The clock oscillator is divided by two (four for TC823) prior to clocking the A/D counters. The clock is also divided by 4 to drive the DC-to-DC converter, and by 768 to generate the LCD backplane frequency. A simplified diagram of the system clock is shown in Figure 8.

COMPONENT VALUE SELECTION

Auto Zero Capacitor - C_{AZ}

The size of the Auto Zero capacitor (C_{AZ}) has some effect on system noise. A 0.22 µF capacitor is recommended. A capacitor with low dielectric absorption (polyester) is required.

Reference Voltage Capacitor - C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate

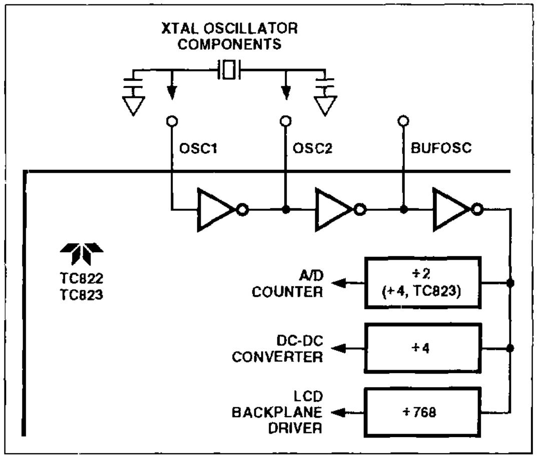


Figure 8 System Clock Generation

cycle is stored on C_{REF}. A 0.22 µF capacitor is typical. A good quality, low leakage capacitor, such as polyester, should be used.

Integrating Capacitor - C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case a ±1.5 V integrator output swing is optimum when the analog input is near full-scale. For 2.5 readings/second (f_{OSC} = 40 kHz) and V_{FS} = 400 mV, a 0.27 µF value is suggested. For a 32.768 kHz crystal, use 0.22 µF. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±1.5V integrator swing. An exact expression for C_{INT} is:

$$C_{INT} = \frac{4000\ V_{FS}}{V_{INT} \bullet R_{INT} \bullet f_{OSC}}$$

where: f_{OSC} = Clock frequency
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor - R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The integrator and buffer can supply 5 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 400 mV full-scale, R_{INT} should be about 100 kΩ.

Reference Voltage Selection

A full scale reading (4000 counts for TC822 and 2000 counts for TC823) requires that the input signal be twice the reference voltage. For example, a 400 mV full scale TC822 requires a reference voltage of 200 mV.

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, that a pressure transducer output is 500 mV for 4000 lb/in^2. Rather than dividing the input voltage by 1.25, the reference voltage should be set to 250 mV. This permits the transducer input to be used directly. For best results, full scale voltage should be limited to 500 mV.

The TC822 can also operate with an external reference. Figure 9 shows internal and external reference applications.

Ratiometric Resistance Measurements

The TC822 true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current is passed through the pair (Figure 10). The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the input voltage will equal the reference voltage and the display will read 2000 (1000 for TC823). The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \cdot 2000$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$

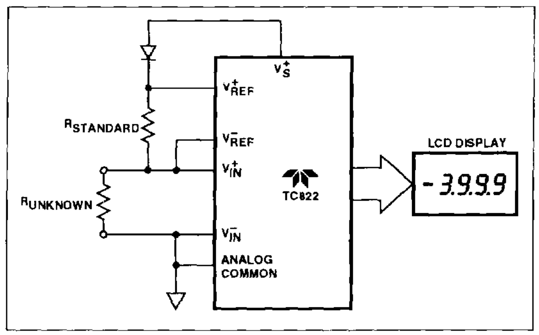


Figure 10 Low Parts Count Ratiometric Resistance Measurement

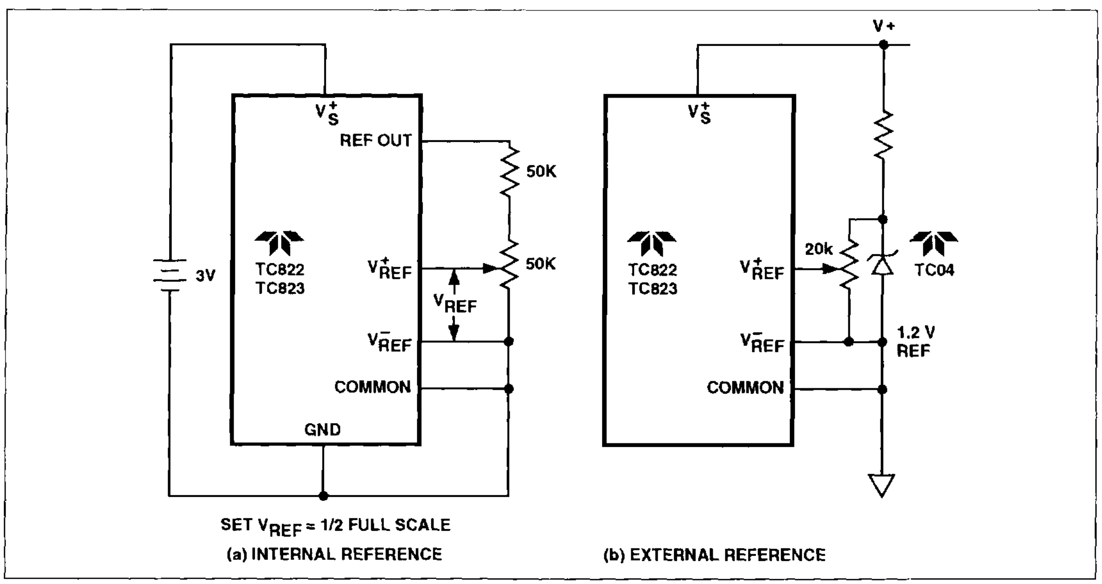


Figure 9 Internal and External Reference Applications

AC-to-DC Converter

The on-chip op amp of the TC822/823 can be combined with external components to convert an AC voltage into a DC voltage. Figure 11 shows a typical circuit.

LCD

The TC822 drives a triplex (multiplexed 3:1) liquid crystal display with three backplanes. The LCD includes decimal points, polarity sign, and annunciators for data hold and low-battery. Table 2 shows the assignment of the display segments to the backplanes and segment drive lines. The backplane drive frequency is obtained by dividing the oscillator frequency by 768.

Table 2 LCD Pin Assignment, TC822

Pin	COM1	COM2	COM3
1	COM1	—	—
2	—	COM2	—
3	—	—	COM3
4	B0	C0	D0
5	A0	G0	E0
6	BATTERY	F0	P1
7	B1	C1	D1
8	A1	G1	E1
9	HOLD	F1	P2
10	B2	C2	D2
11	A2	G2	E2
12	Y	F2	P3
13	B3	C3	D3
14	A3	G3	E3
15	—	—	—
16	—	—	—
17	—	—	—
18	—	—	—

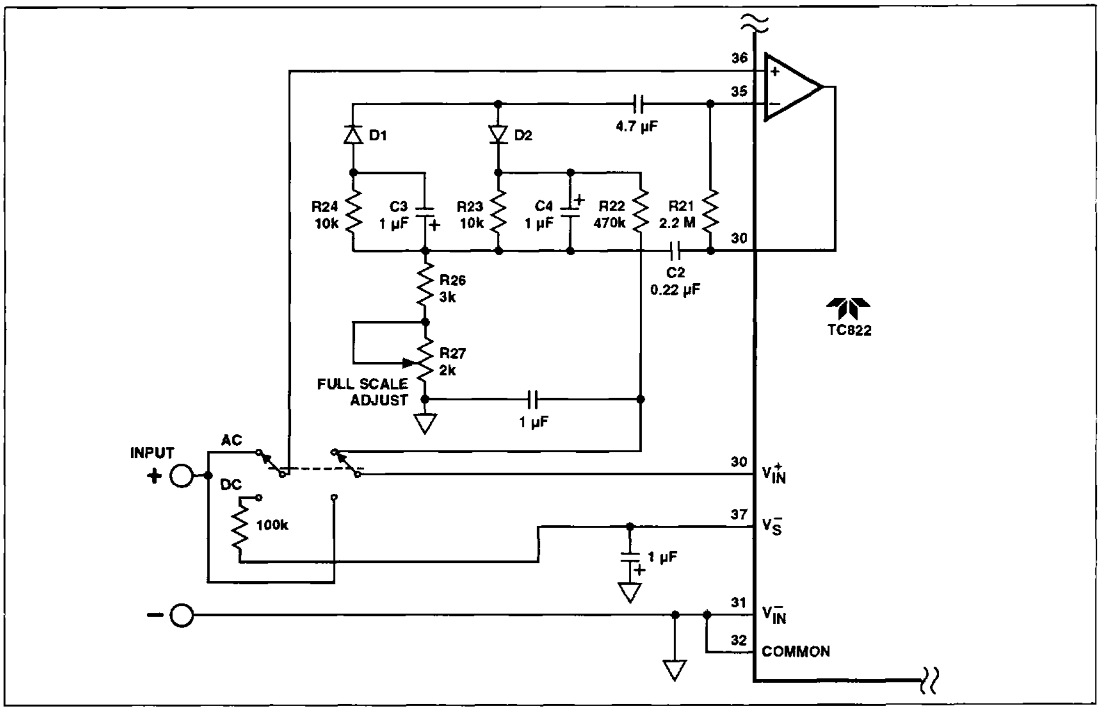


Figure 11 Low Cost AC-to-DC Converter

Backplanes waveforms are shown in Figure 12. These appear on outputs BP1, BP2, and BP3. They remain the same regardless of the segments being driven.

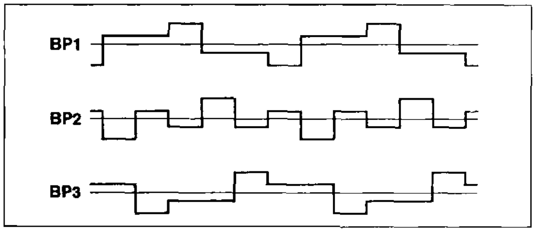


Figure 12 Backplane Waveforms

Other display output lines have waveforms that vary depending on the displays values. Figure 13 shows a set of waveforms for the AGE outputs of one digit for several combinations of 'on' segments.

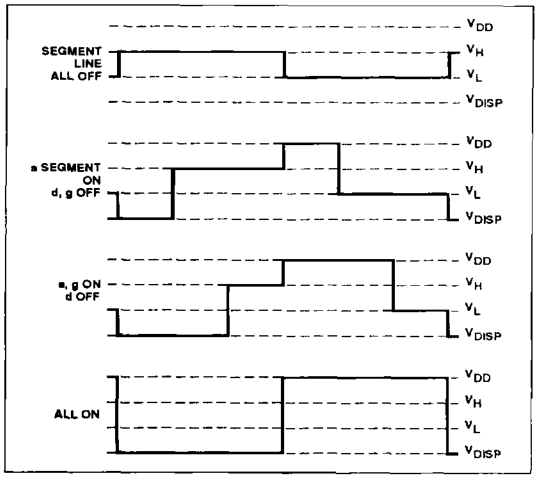


Figure 13 Typical Display Output Waveforms

LCD Source

Although most users will design their own custom LCD, a standard display for the TC822 is available. Figure 14 shows a display, part No. VIM428-DP, available from Varitronix.

Varitronix (USA)	Varitronix
VL Electronics	9/F Liven House
3171 Los Feliz Blvd	61-63 King Yip Street
Suite 303	Kwun Tjong
Los Angeles, CA 90039	Hong Kong
Tel: (312) 661-8883	Tel: 3-410286
FAX: (213) 663-3711	FAX: 3-439555
Part No.:jg VIM428-DP	

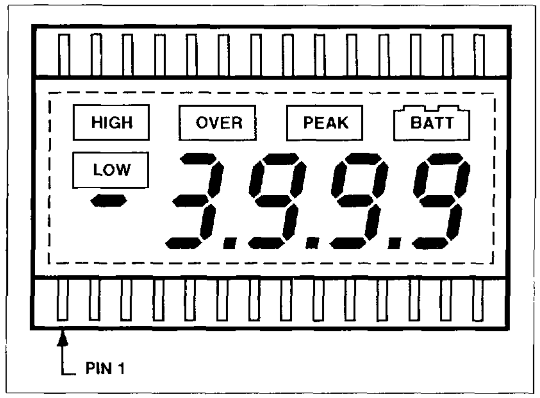


Figure 14 Typical TC822/823 LCD

Annunciator Output

The annunciator output is a square wave running at the backplane frequency (for example, 52 Hz when f_{OSC} = 40 kHZ). The peak-to-peak amplitude is the same as the backplane and segment driver outputs. Connecting an annunciator of the LCD to the annunciator output turns it on; connecting it to its backplane turns it off.

LCD Drive Voltage

The peak-to-peak LCD drive voltage is typically 3.2 Vpp. This voltage will remain stable until the battery voltage falls below the point where the low-battery flag turns on (about 2.1V).