MOTOROLA

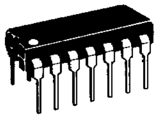
MC12000

DIGITAL MIXER/TRANSLATOR
(D Flip-Flop w/Translator)

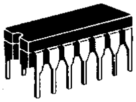
The MC12000 is intended for use as a digital mixer in phase-locked loop frequency synthesizers and other applications where a MECL "D" flip-flop with translators is required. Toggle frequency is typically 250 MHz. TTL to MECL and MECL to TTL translators are provided to facilitate interfacing with MECL or TTL circuits.

The MC12000 is designed to operate from a single power supply of either +5.0 Vdc or −5.2 Vdc.

DIGITAL MIXER/TRANSLATOR

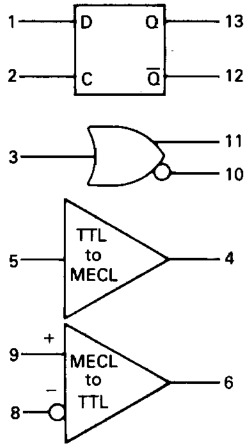


P SUFFIX
PLASTIC PACKAGE
CASE 646



L SUFFIX
CERAMIC PACKAGE
CASE 632

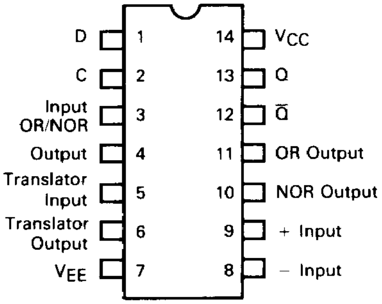
LOGIC DIAGRAM



D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

V_{CC} = Pin 14
V_{EE} = Pin 7

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 V

@ Test Temperature	Volts											mA		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHA}	V_R	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}
0°C	+4.25	+3.130	+3.855	+3.49	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-0.4
25°C	+4.28	+3.150	+3.895	+3.525	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-0.4
75°C	+4.37	+3.170	+3.955	+3.550	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-0.4

Characteristic	Symbol	Pin Under Test	MC12000 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	7				85	117			mAdc		–	–	–		–	–	–	–	–	14	–	–		7
Input Current	I_{INH1}	1	–	–	–		200	–		µAdc	1	2	–	–	–	–	–	–	–	–	14	–	–	–	7
		2	–	–	–		200	–		↓	2	1	–	–	–	–	–	–	–	–	↓	–	–	–	↓
		3	–	–	–		200	–			3	–	–	–	–	–	–	–	–	–		–	–	–	
	I_{INH2}	5	–	40	–	–	40	–	40		–	–	–	–	–	–	5	–	–	–		–	–	–	
	I_{INH3}	8		–	1.4	–	3.6	–	–	mAdc	9	8	–	–	–	–	–	–	–	–		–	–	–	
		9	–	–	—	–	—	–			9	8	–	–	–	–	–	–	–	–		–	–	–	
	I_{INL1} (Leakage Current)	1	–	–	–	–	2.0	–	–	µAdc	–	–	–	–		–	–	–	–		14	–		–	1,7
		2	–	–	–		2.0	–	–	↓	–	–	–	–	–	–	–	–	–	–	↓	–	–	–	2,7
		3	–			–	2.0	–	–			–	–	–	–	–	–	–	–	–			–	–	3,7
	I_{INL2}	5		+1.6		–	+1.6		+1.6	mAdc	–	–	–		5	–	–	–	–	–			–	–	7
	I_{INL3}	8			2.0	–	5.0		–	↓	8	9	–		–	–	–	–		–			–	–	↓
	I_{INL4}	9			0.8	–	2.0	–	–		8	9	–	–	–	–	–	–	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH1}	4	4.000	4.25	4.040	–	4.28	4.100	4.37	Vdc	–	–	–	–	–	5	–	–	–	–	14	4	–	–	7
		10	↓	↓	↓	–	↓	↓	↓	↓	–	3	–	–	–	–	–	–	–	–	↓	10	–	–	↓
		11				–					3	–	–	–	–	–	–	–	–	–		11	–	–	
		12†										1	–	–	–	–	–	–	–	–		12	–	–	
		13†									1	–	–	–	–	–	–	–	–	–		13	–	–	
	V_{OH2}	6	2.400		2.400	–		2.400	–	Vdc	9	8	–	–	–	–	–	–	–	–	14	–	–	6	7
Logic "0" Output Voltage	V_{OL1}	4	3.0	3.370	3.05		3.380	3.07	3.46	Vdc	–	–	–	–	5	–	–	–	–	–	14	4	–	–	7
		10	↓	↓	↓	–	↓	↓	↓	↓	3	–	–	–	–	–	–	–	–	–	↓	10	–	–	↓
		11				–					–	3	–	–	–	–	–	–	–	–		11	–	–	
		12†									1	–	–	–	–	–	–	–	–	–		12	–	–	
		13†									–	1	–	–	–	–	–	–	–	–		13	–	–	
	V_{OL2}	6		0.500	–	–	0.500	–	0.500	Vdc	8	9	–	–	–	–	–	–	–	–	14	–	6	–	7
Logic "1" Threshold Voltage	V_{OHA}	4	3.980		4.020	–		4.080	–	Vdc	–	–	–	–	–	–	–	–	5	–	14	4	–	–	7
		10	↓		↓	–	–	↓	–	↓	–	–	–	3	–	–	–	–	–	–	↓	10	–	–	↓
		11				–	–		–		–	–	3	–	–	–	–	–	–	–		11	–	–	
		12†				–			–		–	–	–	1	–	–	–	–	–	–		12	–	–	
		13†									–	–	1	–	–	–	–	–	–	–		13	–	–	
Logic "0" Threshold Voltage	V_{OLA}	4		3.390		–	3.400	–	3.430	Vdc	–	–	–	–	–	–	–	–	–	5	14	4	–	–	7
		10	–	↓		–	↓	–	↓	↓	–	–	3	–	–	–	–	–	–	–	↓	10	–	–	↓
		11	–			–		–			–	–	–	3	–	–	–	–	–	–		11	–	–	
		12†				–					–	–	1	–	–	–	–	–	–	–		12	–	–	
		13†						–			–	–	–	1	–	–	–	–	–	–		13	–	–	
Short Circuit Current	I_{SC}	6	-65	-20	-65		-20	-65	-20	mAdc	9	8	–	–	–	–	–	–	–	–	14	–	–	–	6,7

†Output Level to be measured after a clock pulse has been applied to the C input (pin 2) $\sqcap$ V_{IHmax} / V_{ILmin}

ELECTRICAL CHARACTERISTICS

Supply Voltage = -5.2 V

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}
	TEST VOLTAGE/CURRENT VALUES													
	Volts											mA		
0°C	-0.75	-1.870	-1.145	-1.51	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-0.4
25°C	-0.72	-1.850	-1.105	-1.475	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-0.4
75°C	-0.63	-1.830	-1.045	-1.450	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-0.4

Characteristic	Symbol	Pin Under Test	MC12000 0°C Min	0°C Max	25°C Min	25°C Typ	25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	–	–	–	90	117	–	–	mAdc
Input Current	I_{INH1}	1	–	–	–	–	200	–	–	µAdc
		2	–	–	–	–	200	–	–	↓
		3	–	–	–	–	200	–	–	↓
	I_{INH2}	5	–	40	–	–	40	–	40	↓
	I_{INH3}	8	–		1.4	–	3.6	–	–	mAdc
		9	–	–	–	–	–	–	–	
	I_{INL1} (Leakage Current)	1	–	–	–	–	2.0	–	–	µAdc
		2	–	–	–	–	2.0	–	–	↓
		3	–	–	–	–	2.0	–	–	↓
	I_{INL2}	5	–	1.6	–	–	1.6	–	1.6	mAdc
	I_{INL3}	8	–		2.0	–	5.0	–	–	↓
	I_{INL4}	9	–	–	0.8	–	2.0	–	–	↓
Logic "1" Output Voltage	V_{OH1}	4	-1.000	-0.75	-0.960	–	-0.72	-0.900	-0.63	Vdc
		10	↓	↓	↓	–	↓	↓	↓	↓
		11	↓	↓	↓	–	↓	↓	↓	↓
		12†	↓	↓	↓	–	↓	↓	↓	↓
		13†	↓	↓	↓	–	↓	↓	↓	↓
	V_{OH2}	6	-2.800	–	-2.800	–		-2.800	–	Vdc
Logic "0" Output Voltage	V_{OL1}	4	-1.99	-1.635	-1.95	–	-1.620	-1.93	-1.54	Vdc
		10	↓	↓	↓	–	↓	↓	↓	↓
		11	↓	↓	↓	–	↓	↓	↓	↓
		12†	↓	↓	↓	–	↓	↓	↓	↓
		13†	↓	↓	↓	–	↓	↓	↓	↓
	V_{OL2}	6	–	-4.700		–	-4.700	–	-4.700	Vdc
Logic "1" Threshold Voltage	V_{OHA}	4	-1.020	–	-0.980	–	–	-0.920	–	Vdc
		10	↓	–	↓	–	–	↓	–	↓
		11	↓	–	↓	–	–	↓	–	↓
		12†	↓	–	↓	–	–	↓	–	↓
		13†	↓	–	↓	–	–	↓	–	↓
Logic "0" Threshold Voltage	V_{OLA}	4		-1.615	–		-1.600	–	-1.575	Vdc
		10		↓	–		↓	–	↓	↓
		11		↓	–		↓	–	↓	↓
		12†		↓	–		↓	–	↓	↓
		13†	–	↓	–		↓	–	↓	↓
Short Circuit Current	I_{SC}	6	-65	-20	-65	–	-20	-65	-20	mAdc

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

Symbol	Pin Under Test	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OL}	(V_{CC}) Gnd
I_E	7	–	–	–	–	–	–	–	–	–	–	7	–	–	–	14
I_{INH1}	1	1	2	–	–	–	–	–	–	–	–	7	–	–	–	14
	2	2	1	–	–	–	–	–	–	–	–	↓	–	–	–	↓
	3	3	–	–	–	–	–	–	–	–	–	↓	–	–	–	↓
I_{INH2}	5	–	–	–	–	–	–	5	–	–	–	↓	–	–	–	↓
I_{INH3}	8	9	8	–	–	–	–	–	–	–	–	↓	–	–	–	↓
	9	9	8	–	–	–	–	–	–	–	–	↓	–	–	–	↓
I_{INL1} (Leakage Current)	1	–	–	–	–	–	–	–	–	–	–	1,7	–	–	–	14
	2	–	–	–	–	–	–	–	–	–	–	2,7	–	–	–	↓
	3	–	–	–	–	–	–	–	–	–	–	3,7	–	–	–	↓
I_{INL2}	5	–	–	–	–	5	–	–	–	–	–	7	–	–	–	↓
I_{INL3}	8	8	9	–	–	–	–	–	–	–	–	↓	–	–	–	↓
I_{INL4}	9	8	9	–	–	–	–	–	–	–	–	↓	–	–	–	↓
V_{OH1}	4	–	–	–	–	–	5	–	–	–	–	7	4	–	–	14
	10	–	3	–	–	–	–	–	–	–	–	↓	10	–	–	↓
	11	3	–	–	–	–	–	–	–	–	–	↓	11	–	–	↓
	12†	–	1	–	–	–	–	–	–	–	–	↓	12	–	–	↓
	13†	1	–	–	–	–	–	–	–	–	–	↓	13	–	–	↓
V_{OH2}	6	9	8	–	–	–	–	–	–	–	–	7	–	–	6	14
V_{OL1}	4	–	–	–	–	5	–	–	–	–	–	7	4	–	–	14
	10	3	–	–	–	–	–	–	–	–	–	↓	10	–	–	↓
	11	–	3	–	–	–	–	–	–	–	–	↓	11	–	–	↓
	12†	1	–	–	–	–	–	–	–	–	–	↓	12	–	–	↓
	13†	–	1	–	–	–	–	–	–	–	–	↓	13	–	–	↓
V_{OL2}	6	8	9	–	–	–	–	–	–	–	–	7	–	6	–	14
V_{OHA}	4	–	–	–	–	–	–	–	–	5	–	7	4	–	–	14
	10	–	–	–	3	–	–	–	–	–	–	↓	10	–	–	↓
	11	–	–	3	–	–	–	–	–	–	–	↓	11	–	–	↓
	12†	–	–	–	1	–	–	–	–	–	–	↓	12	–	–	↓
	13†	–	–	1	–	–	–	–	–	–	–	↓	13	–	–	↓
V_{OLA}	4	–	–	–	–	–	–	–	–	–	5	7	4	–	–	14
	10	–	–	3	–	–	–	–	–	–	–	↓	10	–	–	↓
	11	–	–	–	3	–	–	–	–	–	–	↓	11	–	–	↓
	12†	–	–	1	–	–	–	–	–	–	–	↓	12	–	–	↓
	13†	–	–	–	1	–	–	–	–	–	–	↓	13	–	–	↓
I_{SC}	6	9	8	–	–	–	–	–	–	–	–	6,7	–	–	–	14

†Output Level to be measured after a clock pulse has been applied to the C input (pin 2) V_{IHmax} ⎍ V_{ILmin}

AC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC12000								TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW:					
			0°C		+25°C			+75°C								
			Min	Max	Min	Typ	Max	Min	Max	Unit	Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	Pulse Out	V_{EE} -3.2 V or -3.0 V	V_{CC} +2.0 V
Propagation Delay (See Figure 4)	t_{2+13+}	2,13	–	–	–	2.4	3.5	–	–	ns	2	1	–	13	7	14
	t_{2+13-}	2,13	–	–	–	2.4	3.5	–	–	ns	2	1	–	13	7	14
	t_{2+12+}	2,12	–	–	–	2.4	3.5	–	–	ns	2	1	–	12	7	14
	t_{2+12-}	2,12	–	–	–	2.4	3.5	–	–	ns	2	1	–	12	7	14
	t_{3+11+}	3,11	–	–	–	1.5	2.5	–	–	ns	3	–	–	11	7	14
	t_{3-11-}	3,11	–	–	–	1.5	2.5	–	–	ns	3	–	–	11	7	14
	t_{3+10-}	3,10	–	–	–	1.5	2.5	–	–	ns	3	–	–	10	7	14
	t_{3-10+}	3,10	–	–	–	1.5	2.5	–	–	ns	3	–	–	10	7	14
	t_{5+4+}	5,4	–	–	–	3	4.5	–	–	ns	–	–	5	4	7	14
	t_{5-4-}	5,4	–	–	–	1.5	2.5	–	–	ns	–	–	5	4	7	14
	t_{9+6+}	9,6	–	–	–	8.0	12.0	–	–	ns	A	–	–	6	7	14
	t_{9-6-}	9,6	–	–	–	5.0	10.0	–	–	ns	A	–	–	6	7	14
Output Rise Time (See Figure 4)	t_{13+}	13	–	–	–	2.8	3.5	–	–	ns	2	1	–	13	7	14
	t_{12+}	12	–	–	–	2.8	↓	–	–	ns	2	1	–	12	7	14
	t_{11+}	11	–	–	–	2.0	↓	–	–	ns	3	–	–	11	7	14
	t_{10+}	10	–	–	–	2.0	↓	–	–	ns	3	–	–	10	7	14
	t_{4+}	4	–	–	–	2.4	↓	–	–	ns	–	–	5	4	7	14
Output Fall Time (See Figure 4)	t_{13-}	13	–	–	–	2.8	3.5	–	–	ns	2	1	–	13	7	14
	t_{12-}	12	–	–	–	2.8	↓	–	–	ns	2	1	–	12	7	14
	t_{11-}	11	–	–	–	2.0	↓	–	–	ns	3	–	–	11	7	14
	t_{10-}	10	–	–	–	2.0	↓	–	–	ns	3	–	–	10	7	14
	t_{4-}	4	–	–	–	2.4	↓	–	–	ns	–	–	5	4	7	14
Setup Time (See Figure 5)	$t_{setup"1"}$	13	–	–	–	0.2	–	–	–	ns	2	1	–	–	7	14
	$t_{setup"0"}$	13	–	–	–	0.7	–	–	–	ns	2	1	–	–	7	14
Hold Time (See Figure 5)	$t_{hold"1"}$	13	–	–	–	0.0	–	–	–	ns	2	1	–	–	7	14
	$t_{hold"0"}$	13	–	–	–	1.0	–	–	–	ns	2	1	–	–	7	14
Toggle Frequency (See Figure 6)	f_{tog}	13	200	–	200	250	–	200	–	MHz	–	–	–	–	7	14

FIGURE 2 — TYPICAL DIGITAL MIXER

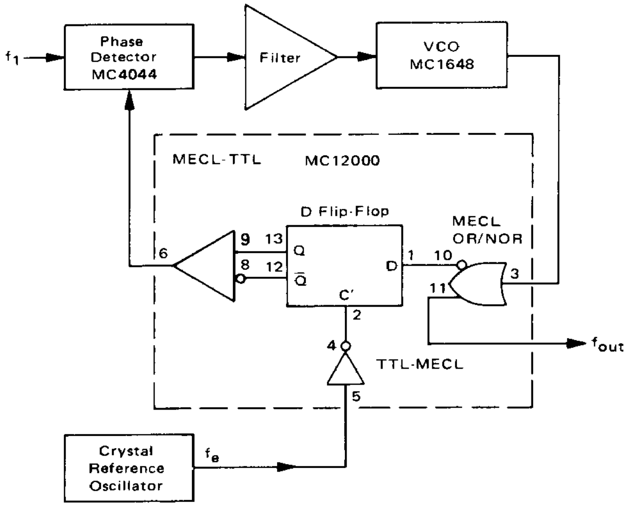
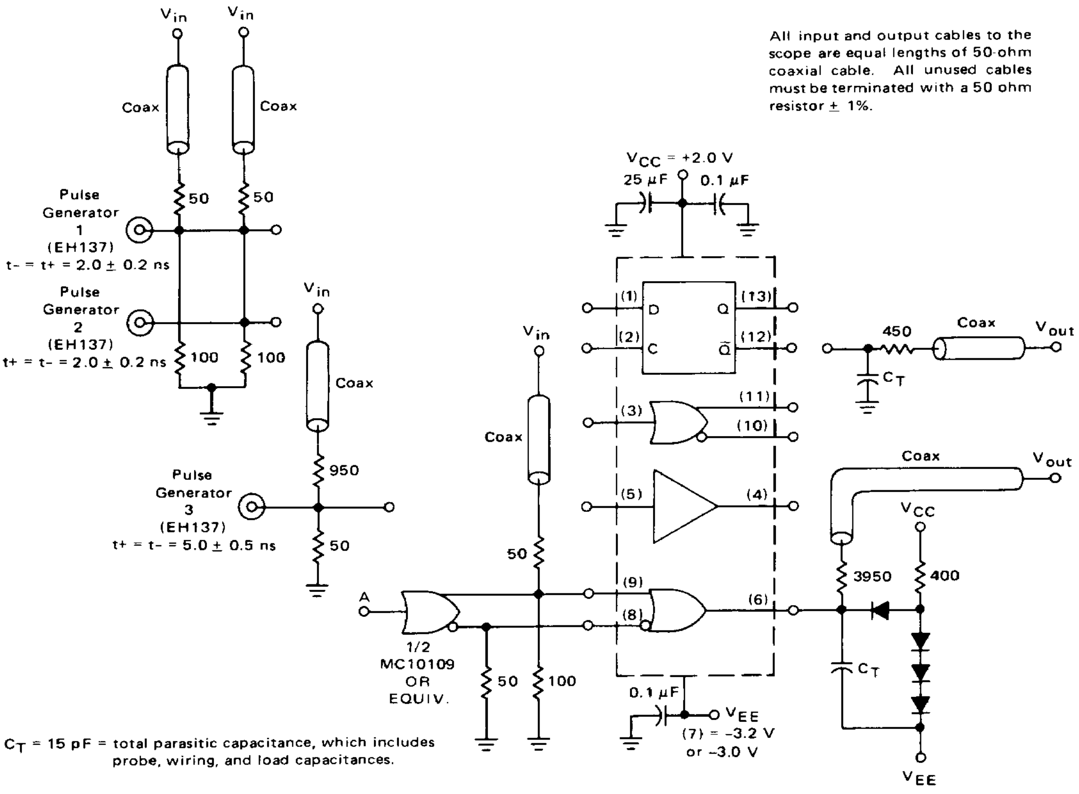


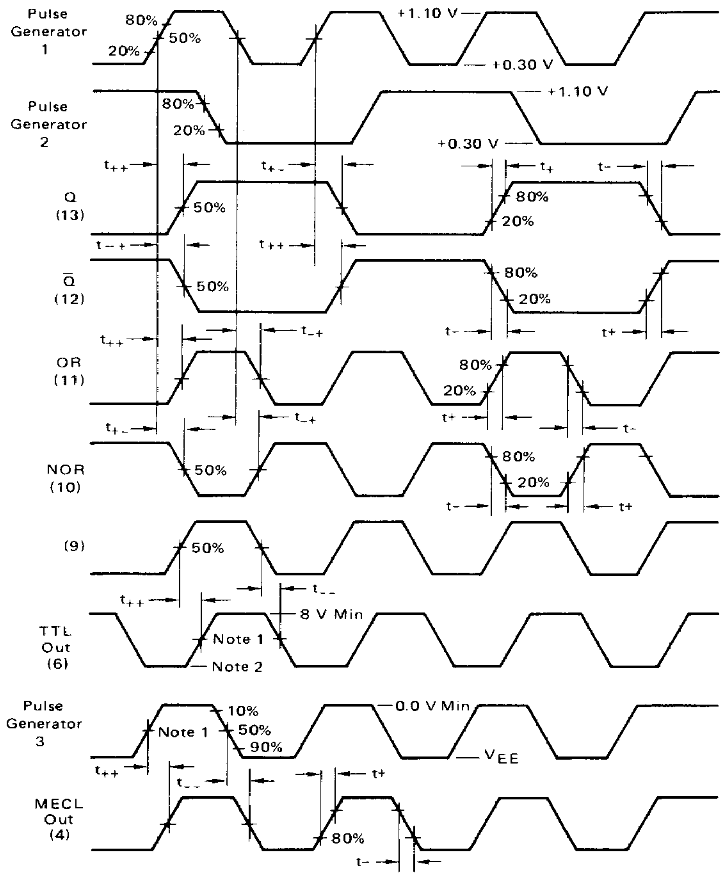
FIGURE 3 — SWITCHING TIME TEST CIRCUIT



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. All unused cables must be terminated with a 50 ohm resistor ± 1%.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 4 — AC TEST VOLTAGE WAVEFORMS



NOTES:

1. V_{EE} + 1.5 V
2. V_{EE} + 0.5 V max

FIGURE 5 — SETUP AND HOLD TIME WAVEFORMS (See Figure 3)

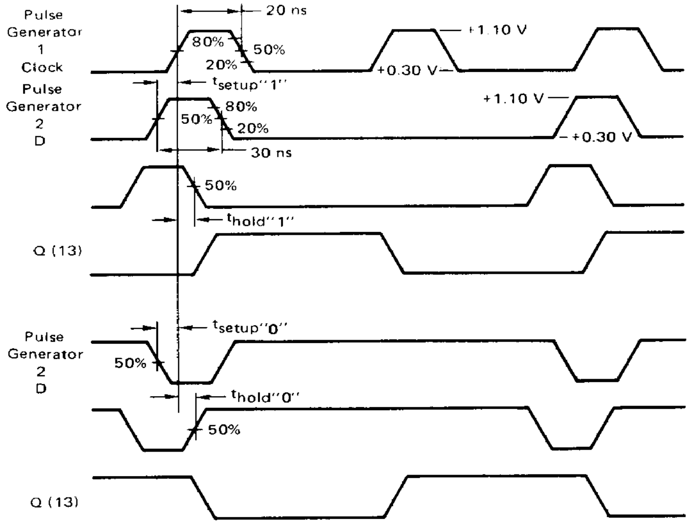
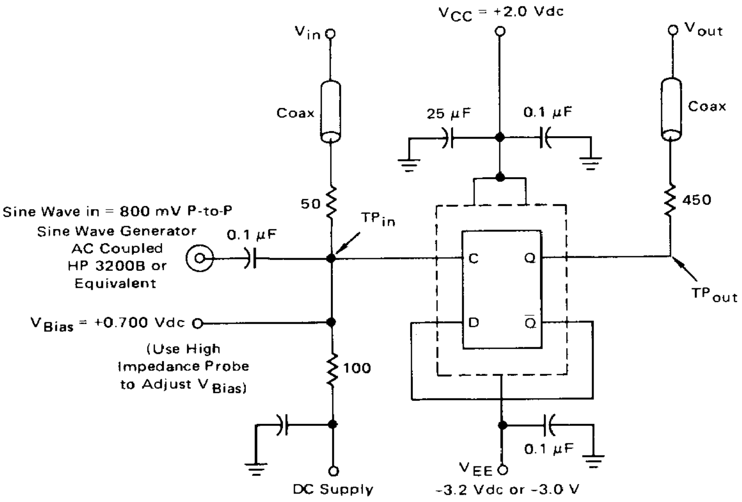


FIGURE 6 — TOGGLE FREQUENCY TEST CIRCUIT



The maximum Toggle Frequency of MC12000 has been exceeded when either:

1. The output Peak-to-Peak voltage swing falls below 600 mV

   or

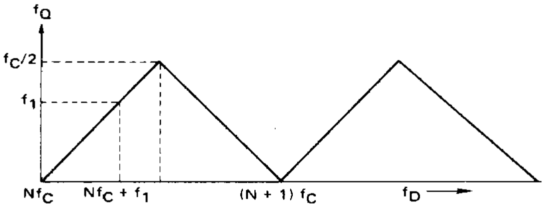
2. The devices cease to Toggle (divide by 2).

MC12000 DIGITAL MIXER

This device is a digital mixer designed to operate with logic levels at its input and output ports. In operation it is an MECL type "D" flip-flop with level translators to and from TTL to accomodate most interfacing demands. Output frequency (f_Q) as a function of "D" and clock inputs is shown in Figure 7. It can be seen that either direct or harmonic mixing may be employed, that is, f_Q may be either the difference between f_D and f_C or the difference between f_D and the Nth harmonic of f_C.

One particular advantage of mixing in phase locked loops (PLL) is that lower frequencies may be generated for use in portions of the circuit where digital processing is done (with divide-by-P network and/or phase detector). Lower frequency operation often reduces overall system cost since a less expensive logic form may be utilized. However use of the mixing technique is not a panacea for all VHF applications and the design of such synthesizer systems must be approached with care.

FIGURE 7



Use of the MC12000 in a non-harmonic PLL is straightforward (Figure 8). Output frequency is the sum of both input quantities ($f_1 + f_C$) as long as f_1 is less than $f_C/2$ (See Figure 7), since f_Q can go no higher than that. Unless VCO output range is restricted somewhat there is a chance also that the loop may operate at the second harmonic of f_C. This problem is minimal in the loop of Figure 8, however, since the output frequency would have to vary more than 2:1.

Mixing is used because the digital phase detector has an upper frequency limit of about 10 MHz and many loops require direct locks at 20 MHz or more. Direct downmixing does not change any loop characteristics except the sampling rate which restricts loop natural frequency to about $f_C/10$ in practical circuits. Although output frequency may be changed by varying either f_1 or f_C, the clock input is usually crystal controlled since it is of the same magnitude as f_D and more difficult to stabilize.

FIGURE 8

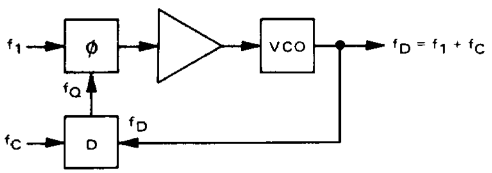
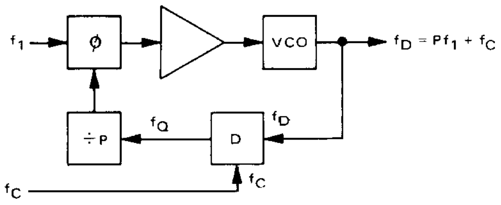


FIGURE 9



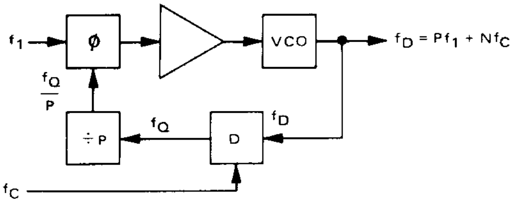
Combining a standard synthesis configuration with the mixer yields a circuit capable of high frequency operation at low cost (Figure 9), if the output frequency range is relatively small $(P_{max} - P_{min})\ f_1 < f_C/2$. In fact the choice of harmonic or non-harmonic mixing is largely based on the availability of a suitable crystal or other reference source for f_C versus the needed frequency coverage. Considering all the restrictions on f_C, its value (and the maximum harmonic number N) are dictated by the following expressions:

$$N < \frac{f_{D(min)} - f_1}{2\ \Delta f_D} \quad (1)$$

$$Nf_C = f_{D(min)} - f_1 \quad (2)$$

where Δf_D = change in output frequency.

FIGURE 10



Using Equations (1) and (2) above the minimum value of f_C may be found for the circuit of Figure 10 and still get adequate frequency coverage. In this minimum configuration all necessary output frequencies may be generated by programming the "P" count string. But the divide number might bear no obvious relation to the output frequency such as often happens with non-mixing synthesizers.

DESIGN EXAMPLES

Example #1

Output Frequency: 48-54 MHz
Frequency Increments: 10 kHz

Using Equations (1) and (2), a minimum frequency (f_C) version can be designed:

$$f_1 = \text{increment} = 10\text{ kHz}$$

$$N < \frac{48\text{ MHz} - 10\text{ kHz}}{2\ (54\text{-}48)\text{ MHz}}$$

$$N < 4$$

Let $N = 3$

$$Nf_C = 47.99\text{ MHz}$$

$$f_C = \frac{Nf_C}{N} = \frac{47.99}{3} = 15.99666\text{ MHz}$$

$$f_C = 15.996666\text{ MHz}$$

$$P_{min} = 1$$

$$P_{max} = \frac{\Delta f_D}{10\text{ kHz}} + P_{min} \qquad (3)$$

$$P_{max} = \frac{6\text{ MHz}}{10\text{ kHz}} + P_{min}$$

$$P_{max} = 601$$

$$\begin{aligned} f_{Q(max)} &= P_{max}\, f_1 \\ &= 6.01\text{ MHz} \end{aligned} \qquad (4)$$

Equation (4) above puts the divider string (divide-by-P) into a medium frequency situation where devices such as the MC4016/4316 may be utilized. Note that the divider number now indicates the channel selected rather than output frequency. That is, at $f_D = 48.000$ MHz, $P = 1$; at $f_D = 54.000$ MHz, $P = 601$.

If "proper" divide-by-P readings are desired for direct frequency readout a slight circuit modification is necessary. To enable a division at 48.000 MHz the first divide-by-P must be 100 rather than 1, and P_{max} would then be 700 to cover all 6 MHz. Recalculating $f_{Q(max)}$ from Equation 4 we still find that the 7 MHz maximum value allows use of the same components. The next question concerns the allowable range of f_Q in relation to f_C ($f_Q < f_C/2$). Since f_C is nearly 16 MHz, the range of f_Q can be contained. A cosmetic change to the most significant digit switch completes the design. Instead of reading 1 through 7 it must be modified to display 48 through 54.

Example #2

Output Frequency: 144-148 MHz
Frequency Increments: 10 kHz

$$f_1 = \text{increment} = 10\text{ kHz}$$

$$N < \frac{144.00 - 0.01}{2\ (4)}$$

$$N < 18$$

Let $N = 17$

$$\begin{aligned} Nf_C &= 144.00 - 0.01\text{ MHz} \\ &= 143.99 \end{aligned}$$

$$f_C = \frac{Nf_C}{N} = 8.470\text{ MHz}$$

$$P_{min} = 1$$

$$\begin{aligned} P_{max} &= \frac{4\text{ MHz}}{10\text{ kHz}} + 1 \\ &= 401 \end{aligned}$$

$$f_{Q(max)} = P_{max}\, f_1 = 4.01\text{ MHz}$$

Maximum frequency seen by the divide-by-P chain is still well within the MC4016 rating.

When converting this synthesizer to one that needs frequency directly, a "1" is again added to the most significant digit (MSD). This results in a P_{min} of 100 to P_{max} of 500. In this example, however, $f_{Q(max)}$ is 5 MHz which easily exceeds $f_C/2$. To alleviate this difficulty, the "N" factor must be decreased in order to raise f_C to at least 10 MHz.

$$N < \frac{f_{D(min)} - f_1}{f_C}$$

Let $f_C = 10$ MHz

$$N < \sim 14.4$$

Let $N = 14$

$$Nf_C = 143.99\ \text{(from above)}$$

$$f_C = \frac{Nf_C}{N} = \frac{143.99}{14}$$

$$f_C = 10.28540\text{ MHz} \qquad (5)$$

VCO RANGE RESTRICTIONS

As in all harmonically locked PLL's, it is possible for the loop to lock on the wrong harmonic if there is too wide a range in the VCO. This situation is shown in Figure 11 where the possible false lock areas are indicated near the (N − 1) and (N + 1) harmonic points. The problem of VCO restraint however is more than just making sure that output frequency f_D isn't able to go to B or A′ (the closest false lock points). Actual operating limits are C and C′, symmetrically placed frequencies corresponding to $f_{D(min)}$ about Nf_C and $f_{D(max)}$ about $(Nf+1/2)\ f_C$. If the VCO drops below C while the feedback counter is at P_{min} the phase detector will try to push f_D even lower, toward the stable condition at A (Figure 12). Likewise, at C′ (when $P = P_{max}$) the tendency is for the loop to accelerate toward lockup at B′ (Figure 13). When C or C′ are exceeded the loop will "hang up" and not attain the proper lock.

FIGURE 11

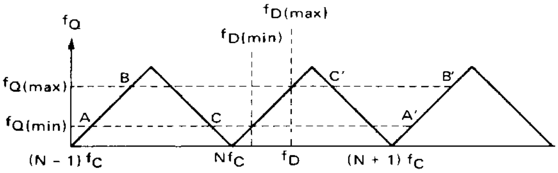


FIGURE 12

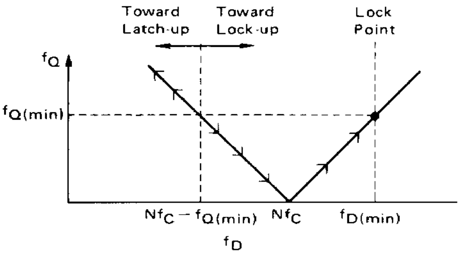
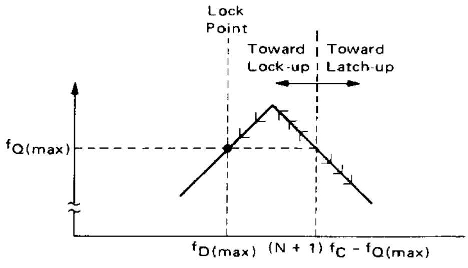
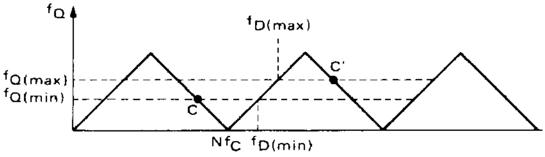


FIGURE 13



The VCO frequency constraints may be quite severe if the minimum f_C formulation is followed and the Nth harmonic is quite high. Where VCO constraint may pose a problem, decrease N below the maximum indicated by Equation (1) until sufficient room is generated by placing the operating range of f_Q on only a small part of the f_D slope (Figure 14). Note that f_C goes up as we approach the more idealized case (Equation 5).

FIGURE 14



The most likely reasons for a "latched up" state in a harmonic loop are turn-on transients and loop overshoot when changing frequency abruptly from one end of the range to the other.

SUMMARY OF SYNTHESIS PROCEDURE

1. Compute harmonic number N

$$N < \frac{f_{D(min)} - f_1}{2\ \Delta f_D}$$

where Δf_D = change in output frequency
f_1 = channel spacing

2. Compute minimum mixing frequency f_C

$$f_C = \frac{f_{D(min)} - f_1}{N}$$

3. Calculate feedback divider's maximum value

$$P_{max} = \frac{\Delta f_D}{f_1} + P_{min}$$

where $P_{min} = 1$ for minimum f_C.

4. Find maximum divide-by-P frequency

$$f_{Q(max)} = \Delta f_D + f_1$$

5. Calculate allowable VCO swing

$$Nf_C - f_1 < f_{VCO} < (N+1)\ f_C - f_{Q(max)}$$

6. If the above constraints are too tight choose the next lower number for N and repeat steps 2 and 5 until satisfied.

SKIP-LOCK TUNING

Harmonic mixing provides an alternate means to frequency synthesis without the feedback divide-by-P network. In this instance the design objective is to provide a large frequency coverage with a set (and relatively wide) channel spacing. The configuration is identical to a single frequency PLL (Figure 15) except it operates in the harmonic mode and tuning is accomplished at the VCO. Output frequency is fixed as being f_1 above all harmonics of f_C. As the VCO is tuned through its range, the loop will acquire and lose signals spaced f_C apart. Since there must be some frequency for the phase detector to operate with, the output frequency cannot be a direct harmonic of f_C. This facet of the circuit often causes users to refer to f_1 as the "offset" frequency.

The value of f_1 is often dictated by output frequency and channel spacing requirements. However the relationship of f_1 to f_C has a large effect on the tunability both up and down the frequency range. If, for example, the loop were locked at point A (Figure 16) and B were the next desired point, then the VCO must be "dragged" from A to A' before lock can be achieved. This frequency adjustment may be quite critical since the frequency difference between A' and B is only $2f_1$. If the VCO is tuned past B the opportunity for lock has been passed.

On the other hand, in going from B to A, the upper end of the VCO control range must only cross A' before the loop acquires frequency A. In either case it's apparent that the loop will not "jump" from one lock point to another and some indication of loop lock should be added. This is normally done by monitoring the VCO dc control line with a pair of comparators and noting when the line reaches its limits.

FIGURE 15

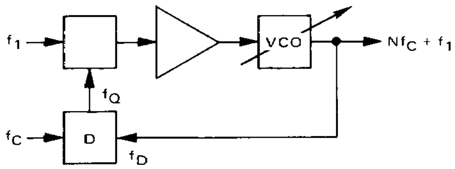


FIGURE 16