



ISO-CMOS MD65SC22

Versatile Interface Adapter

Preliminary Information

Features

- Input/Output Latches.
- Serial data port.
- Two 8-bit bidirectional I/O ports.
- Two 16-bit programmable timers.
- Expanded handshake control.
- Direct replacement for existing NMOS part
- Single 5 volt power supply.
- Low power ISO-CMOS technology.
- Fully TTL compatible.

Applications

- General microprocessor I/O port.
- RS232 interface.
- Keyboard controller.
- Peripheral controller.

Description

The MD65SC22 is a Versatile Interface Adapter containing two 8-bit bidirectional latched ports, two 16-bit programmable timers and a serial to parallel/parallel to serial shift register. The device is fabricated in Mitel's ISO-CMOS technology.

9161-002-046 NA.

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Pin Connections

VSS	1	40	CA1
PA0	2	39	CA2
PA1	3	38	RS0
PA2	4	37	RS1
PA3	5	36	RS2
PA4	6	35	RS3
PA5	7	34	RESET
PA6	8	33	D0
PA7	9	32	D1
PB0	10	31	D2
PB1	11	30	D3
PB2	12	29	D4
PB3	13	28	D5
PB4	14	27	D6
PB5	15	26	D7
PB6	16	25	φ2
PB7	17	24	CS1
CB1	18	23	CS2
CB2	19	22	R/W
VDD	20	21	IRQ

Ordering Information

- MD65SC22AC - 40 Pin Ceramic Package
- MD65SC22AE - 40 Pin Plastic Package

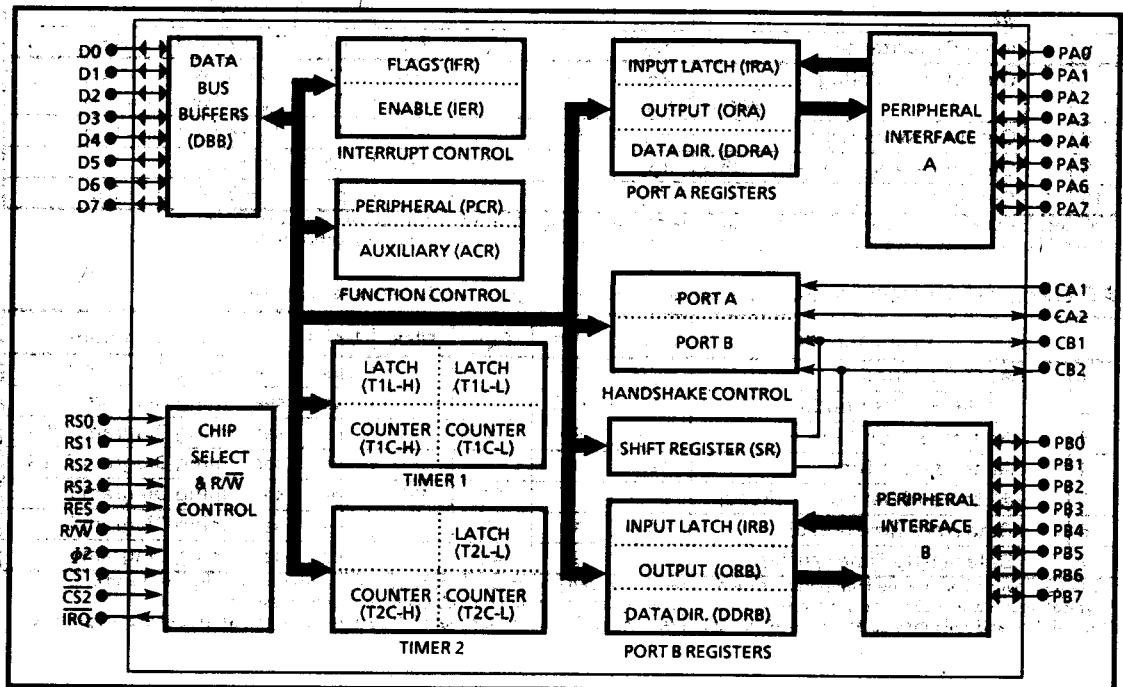


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	$V_{DD}-V_{SS}$	-0.3	7.0	V
2	Voltage on any I/O pin	V_I	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	Current on any I/O pin	I_I		± 10	mA
4	Operating Temperature	T_A	-40	+85	°C
5	Storage Temperature	T_S	-65	+150	°C
6	Power Dissipation	Plastic P_D Ceramic P_D		0.6 1.0	W W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Input Voltage	V_{IH} V_{IL}	2.4 V_{SS}		V_{DD} 0.4	V V	For a noise margin of 400 mV
3	Operating Temperature	T_A	-40	+25	+85	°C	
4	Operating Frequency	f	0		2.0	MHz	

* Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DD1}		90		μA	Inputs High, $\phi 2$ stopped
2	Operating Supply Current	I_{DD}		0.56		mA	$\phi 2 = 2$ MHz, Inputs High
3	Input High Voltage	V_{IH}	2.0		V_{DD}	V	
4	Input Low Voltage	V_{IL}	V_{SS}		0.8	V	
5	Input Leakage Current R/W, RES, RS0-3, CS1, CS2, CA1, $\phi 2$	I_{IZ}			± 2.5	μA	$V_I = V_{SS}$ or $V_I = V_{DD}$
6	Input Capacitance	C_{IN}			7.0	pF	$T_A = 25^\circ C$, f = 1 MHz
7	Output High Voltage	V_{OH}	2.4		V_{DD}	V	$V_{DD} = 4.75V$, $I_{LOAD} = -100\mu A$
	Port B	V_{OH}	1.5		V_{DD}	V	$V_{DD} = 4.75V$, $I_{LOAD} = -1.0mA$
8	Output Low Voltage	V_{OL}	V_{SS}		0.4	V	$V_{DD} = 4.75V$, $I_{LOAD} = 1.6mA$
9	Output Leakage Current	TRQ I_{OZ}		0.01	10	μA	Off State
10	Output Capacitance	C_O			10	pF	$T_A = 25^\circ C$, f = 1 MHz

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages

* Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	$\phi 2$ Cycle Period	t_{CYC}	0.5			μs	see Timing Diagram 1
2	$\phi 2$ HIGH Pulse Width	t_C	0.22			μs	see Timing Diagram 1
3	Address Set-up Time	t_{AS}	90	0		ns	see Timing Diagram 2 & 3
4	Address Hold Time	t_{AH}	0			ns	see Timing Diagram 2 & 3
5	$\phi 2$ to Valid Data Delay (Read)	t_{DDR}		54	190	ns	see Timing Diagram 2
6	Data Hold Time (Read)	t_{DHR}	10	20		ns	see Timing Diagram 2
7	Data Set-up Time (Write)	t_{DSW}	90	42		ns	see Timing Diagram 3

† Timing is over recommended temperature range & recommended power supply voltages. Test loads shown in figures 5 and 6.

* Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Note: Ⓞ Rise and Fall times (t_r & t_f) are < 10 ns; Ⓢ The term negate denotes removal of the active signal and assert denotes its presence.

AC Electrical Characteristics* (Continued) - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ [†]	Max	Units	Test Conditions
8	Data Hold Time (Write)	t_{DHW}	10	0		ns	see Timing Diagram 3
9	Read/Write Set-up Time	t_{RWS}	90	10		ns	see Timing Diagram 2 & 3
10	Read/Write Hold Time	t_{RWH}	0			ns	see Timing Diagram 2 & 3
11	Peripheral Data Set up Time	t_{PCR}	150	0		ns	see Timing Diagram 2
12	Peripheral Data Delay Time	t_{CPW}			500	ns	see Timing Diagram 3
13	$\phi 2$ negate to CA2 falling edge (read, handshake-pulse mode)	t_{CA2}		0.20	1.0	μs	see Timing Diagram 4 & 5
14	$\phi 2$ negate to CA2 rising edge (pulse mode)	t_{RS1}		0.10	1.0	μs	see Timing Diagram 4
15	CA1 assert to CA2 rising edge (handshake mode)	t_{RS2}		0.25	2.0	μs	see Timing Diagram 5
16	$\phi 2$ assert to CA2, CB2 falling edge (write handshake)	t_{WHS}	0.05	0.07	1.0	μs	see Timing Diagram 6 & 7
17	Peripheral Data to CB2 falling edge	t_{DS}	0.20	0.30	1.5	μs	see Timing Diagram 6 & 7
18	$\phi 2$ assert to CA2, CB2 rising edge (pulse mode)	t_{RS3}		0.70	1.0	μs	see Timing Diagram 6
19	CA1, CB1 assert to CA2, CB2 rising edge (handshake mode)	t_{RS4}		0.30	2.0	μs	see Timing Diagram 7
20	CA2, CB2 falling edge to CA1, CB1 assert (handshake mode)	t_{21}	400	330		ns	see Timing Diagram 7
21	Peripheral Data Set up Time to CA1, CB1 assert (input latching)	t_{IL}	300	0		ns	see Timing Diagram 8
22	CA1, CB1 negate time before next latch	t_{AL}	$t_C + 50$	160		ns	see Timing Diagram 8
23	Peripheral Data Hold after CA1, CB1 assert (input latching)	t_{PDH}	150	50		ns	see Timing Diagram 8
24	$\phi 2$ negate to Shift Data Valid	t_{SR1}		40	300	ns	see Timing Diagram 9
25	Shift Data Valid to $\phi 2$ assert	t_{SR2}	300	20		ns	see Timing Diagram 10
26	External Shift to $\phi 2$ negate	t_{SR3}	100	220	t_{CYC}	ns	see Timing Diagram 10
27	Pulse Width, CB1 input pulse	t_{ICW}	$2 \times t_{CYC}$			ns	see Timing Diagram 11
28	Pulse Spacing, CB1 input pulse	t_{ICS}	$2 \times t_{CYC}$			ns	see Timing Diagram 11
29	Pulse Width, PB6 input pulse	t_{IPW}	$2 \times t_{CYC}$			ns	see Timing Diagram 12
30	Pulse Spacing, PB6 input pulse	t_{IPS}	$2 \times t_{CYC}$			ns	see Timing Diagram 12
31	CA1, CB1, CA2, CB2 negate time before next assert	t_{PWI}	$t_C + 50$	170		ns	see Timing Diagram 13
32	$\phi 2$ assert to CB1 rising edge (SR shifted by internal clock)	t_{DPR}		0		ns	see Timing Diagram 14
33	$\phi 2$ assert to CB1 falling edge (SR shifted by internal clock)	t_{DPL}		0		ns	see Timing Diagram 14

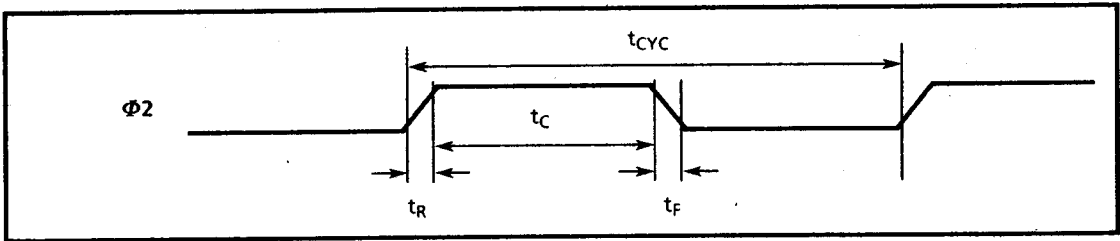
[†] Timing is over recommended temperature range & recommended power supply voltages. Test loads shown in figures 5 and 6.

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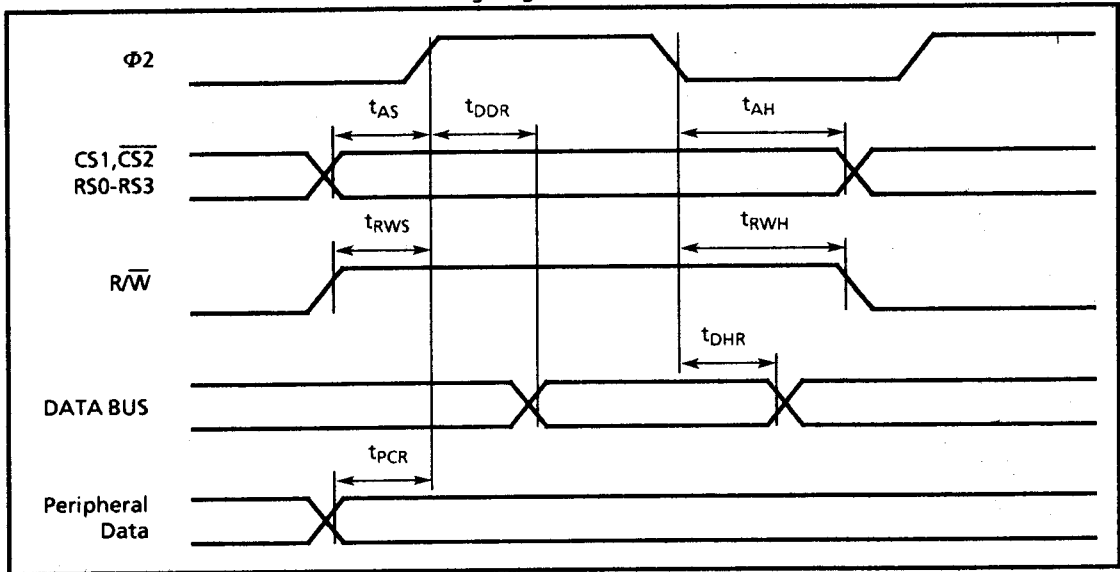
Note: Ⓞ Rise and Fall times (t_r & t_f) are < 10 ns; Ⓢ The term *negate* denotes removal of the active signal and *assert* denotes its presence.

Timing Diagrams

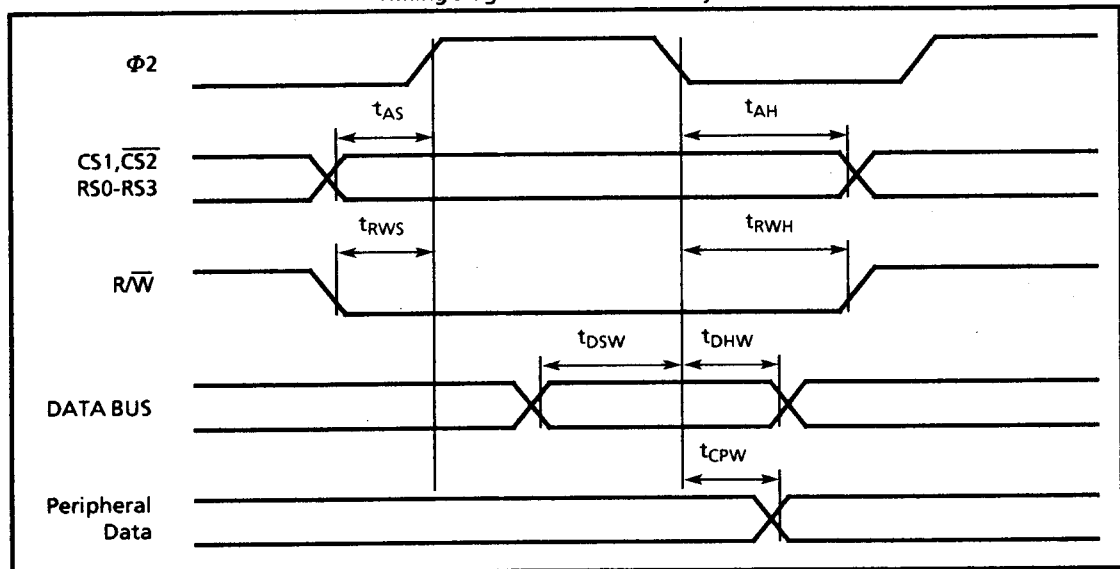
The points from which these timing values are measured are V_{IH} & V_{IL} for inputs and V_{OH} and V_{OL} for outputs



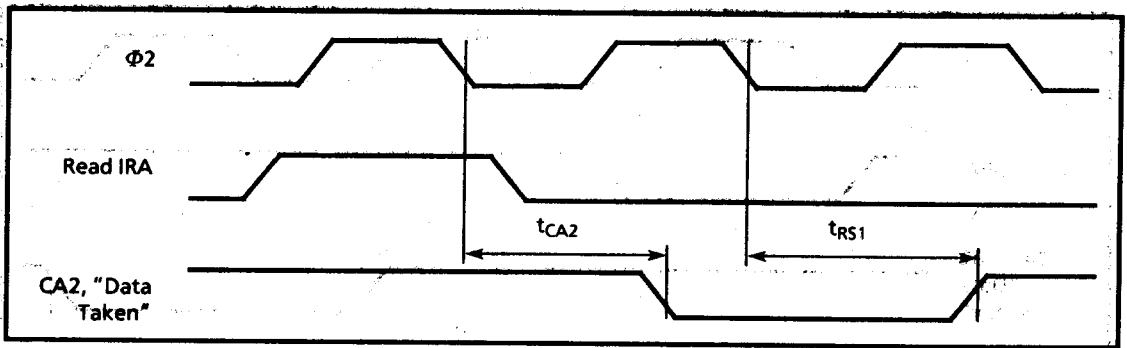
Timing diagram 1. $\Phi 2$ Pulse



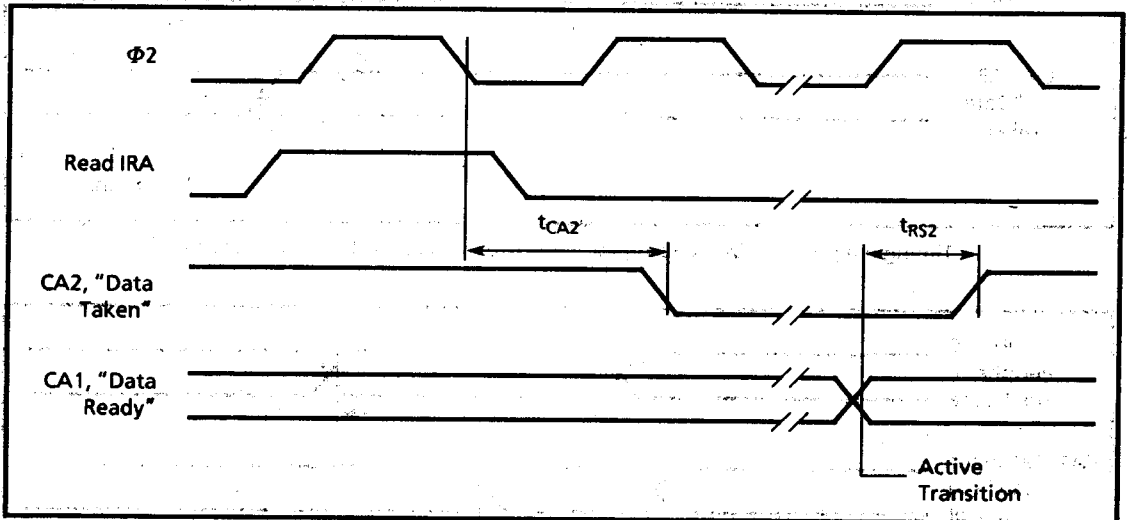
Timing diagram 2. MPU Read Cycle



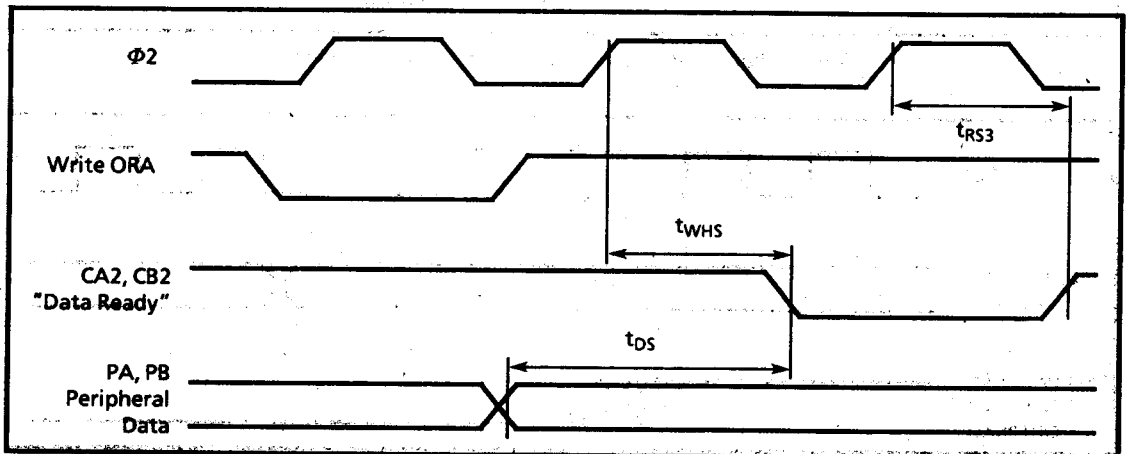
Timing diagram 3. MPU Write Cycle



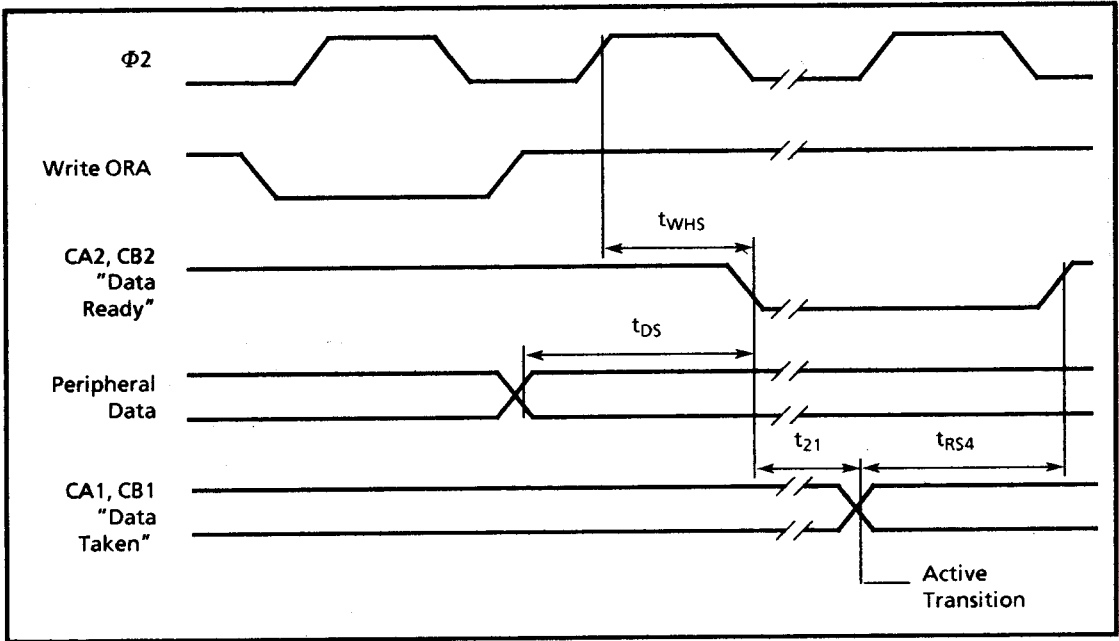
Timing diagram 4. CA2 Timing for Read Handshake, Pulse Mode



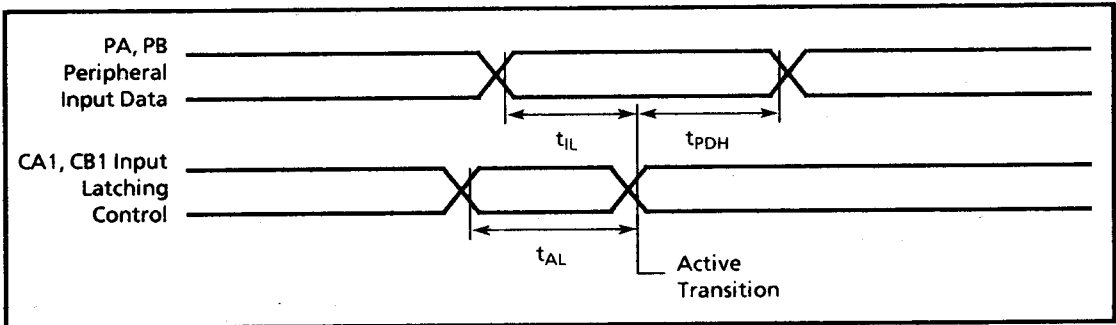
Timing diagram 5. CA2 Timing for Read Handshake, Handshake Mode



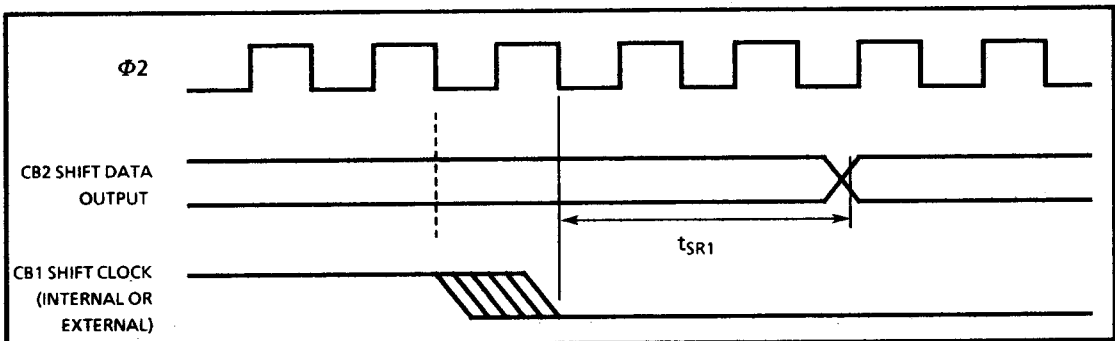
Timing diagram 6. CA2, CB2 Timing for Write Handshake, Pulse Mode



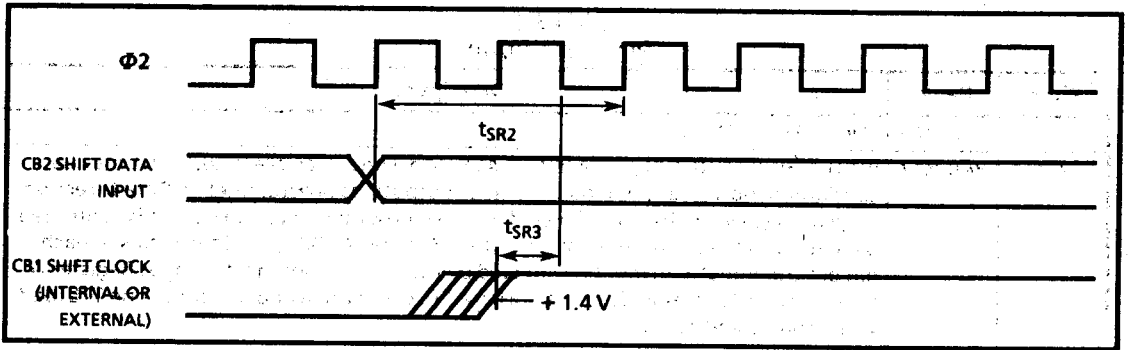
Timing diagram 7. CA2, CB2 Timing for Write Handshake, Handshake Mode



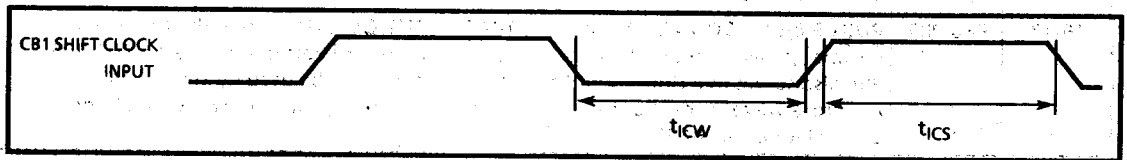
Timing diagram 8. Peripheral Data Input Latch Timing



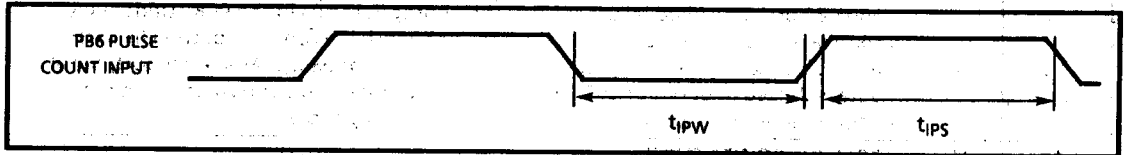
Timing diagram 9. Timing for Shift Out with Internal or External Shift Clocking



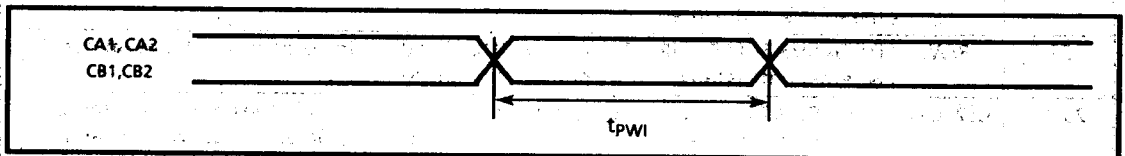
Timing diagram 10. Timing for Shift In with Internal or External Shift Clocking



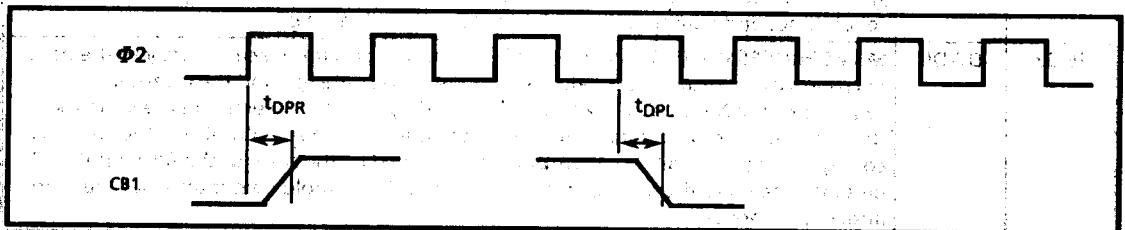
Timing diagram 11. External Shift Clock Timing



Timing diagram 12. Pulse Count Input Timing



Timing diagram 13. Setup Time to Triggering Edge



Timing diagram 14. Shift in/out with Internal Clock - Delay from $\Phi 2$

TABLE 1.
Pin Description

Pin #	Name	Description
1	V _{SS} /GND	LOGIC GROUND
2-9	PA0-PA7	PORT A BIDIRECTIONAL DATA INTERFACE. An 8 line interface whose lines may be configured individually as either inputs or outputs; as programmed in Data Direction Register A (DDRA). The logic level of each pin programmed as an output is controlled by writing to the appropriate bit in Output Register A (ORA), and the status of each pin programmed as an input is reflected by the corresponding bit in Input Register A (IRA). The logic thresholds of the port are TTL compatible and appear as one TTL load when configured as inputs.
10-15	PB0-PB5	PORT B BIDIRECTIONAL INTERFACE. These pins operate in the same manner as PA0-PA7, under the control of DDRB, ORB and IRB. Their logic thresholds are TTL compatible except that they can source 10 mA of current at 1.5 volts, in order to drive Darlington transistor pairs. As inputs they appear as one TTL load.
16-17	PB6-PB7	PORT B BIDIRECTIONAL INTERFACE; TIMER INPUT/OUTPUT. When the timers are disabled, these pins are the two most significant bits of Port B, identical to PB0-PB5. PB6 also serves as a clock input for Timer 2, and PB7 can be used by Timer 1 to generate waveforms. Control of the timer functions is provided by the Auxiliary Control Register (ACR).
18-19	CB1,CB2	PORT B CONTROL LINES AND SERIAL PORT. The port B control lines have various functions, determined by the state of the shift register control bits in the ACR, and the port B control bits in the Peripheral Control Register (PCR). If the shift register is disabled (the use of the shift register preempts the use of these pins by port B), CB1 and CB2 are controlled by the state of the appropriate bits in the PCR. Under PCR control, these pins are used for data transfer handshake control, specifically in the write direction (from the perspective of the microprocessor). As a serial port, serial data is shifted in or out of CB2, and CB1 acts as a clock input or output. Both pins operate as either inputs or outputs, and are TTL compatible.
20	V _{DD}	POSITIVE POWER SUPPLY.
21	IRQ	INTERRUPT REQUEST. This open drain output notifies the controlling microprocessor that the MD65SC22 needs to be serviced. It may only go low when the interrupt enable bits in the Interrupt Enable Register (IER) are programmed to acknowledge the source of the interrupt.
22	R/W	DATA BUS BUFFER DIRECTION CONTROL. The direction control input determines whether data is latched into, or read from the MD65SC22.
23,24	$\overline{CS}2$, CS1	CHIP SELECTS 1 AND 2. These inputs, when asserted, enable the data bus buffer so data may be transferred into or out of the device. Chip Select 1 is active high, and Chip Select 2 is active low. These inputs are qualified by the system clock ($\phi 2$) so that a transfer may only occur when the system clock is high.
25	$\phi 2$	SYSTEM CLOCK (OR ENABLE CLOCK). This input from the microprocessor allows synchronization with the MD65SC22 on data bus transfers. All microprocessor bus set up times and hold times are referenced to the edges of $\phi 2$.
26-33	D7-D0	MICROPROCESSOR DATA PORT. This bidirectional port interfaces directly to the host microprocessor, providing a data path between the data bus and the internal registers of the MD65SC22. When not enabled by the Chip Selects and the $\phi 2$ clock, this port appears as a high impedance to the data bus. Whether the port is configured as an input or an output is determined by the state of the R/W input. All pins interfacing to the microprocessor bus are TTL threshold compatible but are high impedance inputs.

TABLE 1.
Pin Description (continued)

Pin #	Name	Description
34	RES	RESET. The reset pin allows an external reset of the device. An active level (logic low) on this input will clear all internal registers, except the shift registers and the timer latches. All functions are disabled, including interrupts originating from the device. The parallel ports initialize as inputs after a reset.
35-38	RS3-RS0	REGISTER SELECTS 0-3. There are 16 registers inside the MD65SC22, accessible from the controlling microprocessor. When the data port is enabled, the selection of a register for participation in the data transfer is determined by the state of these inputs. RS0 is the least significant bit of the 4 bit register address.
39, 40	CA2, CA1	PORT A CONTROL LINES. These pins have a function very similar to the port B control lines, however, CA1 and CA2 can be used for handshaking control in data transfers in both the write and the read directions (from the microprocessor's perspective). These pins are TTL threshold compatible but are high impedance inputs.

TABLE 2.
Register Decode And Designation

RS3	RS2	RS1	RS0	Register Selected	
				Write Operation	Read operation
0	0	0	0	Output Register B (ORB)	Input Register B (IRB)
0	0	0	1	Output Register A (ORA)	Input Register A (IRA)
0	0	1	0	Data Direction Register B (DDRB)	Data Direction Register B (DDRB)
0	0	1	1	Data Direction Register A (DDRA)	Data Direction Register A (DDRA)
0	1	0	0	T1 Low Order Latches (T1C-L)	T1 Low Order Counter (T1C-L)
0	1	0	1	T1 High order Counter (T1C-H)	T1 High Order Counter (T1C-H)
0	1	1	0	T1 Low Order Latches (T1L-L)	T1 Low Order Latches (T1L-L)
0	1	1	1	T1 High Order Latches (T1L-H)	T1 High Order Latches (T1L-H)
1	0	0	0	T2 Low Order Latches (T2C-L)	T2 Low Order Counter (T2C-L)
1	0	0	1	T2 High Order Counter (T2C-H)	T2 High Order Counter (T2C-H)
1	0	1	0	Shift Register (SR)	Shift Register (SR)
1	0	1	1	Auxiliary Control Register (ACR)	Auxiliary Control Register (ACR)
1	1	0	0	Peripheral Control Register (PCR)	Peripheral Control Register (PCR)
1	1	0	1	Interrupt Flag Register (IFR)	Interrupt Flag Register (IFR)
1	1	1	0	Interrupt Enable Register (IER)	Interrupt Enable Register (IER)
1	1	1	1	ORA (without handshaking)	IRA (without handshaking)

TABLE 3.
Port A pin to register map

External Pin	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Data Register bit	ORA _b 7 IRA _b 7	ORA _b 6 IRA _b 6	ORA _b 5 IRA _b 5	ORA _b 4 IRA _b 4	ORA _b 3 IRA _b 3	ORA _b 2 IRA _b 2	ORA _b 1 IRA _b 1	ORA _b 0 IRA _b 0
Data Direction Reg. bit	DDRA _b 7	DDRA _b 6	DDRA _b 5	DDRA _b 4	DDRA _b 3	DDRA _b 2	DDRA _b 1	DDRA _b 0

TABLE 4.
Port B pin to register map

External Pin	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Data Register bit	ORB _b 7 IRB _b 7	ORB _b 6 IRB _b 6	ORB _b 5 IRB _b 5	ORB _b 4 IRB _b 4	ORB _b 3 IRB _b 3	ORB _b 2 IRB _b 2	ORB _b 1 IRB _b 1	ORB _b 0 IRB _b 0
Data Direction Reg. bit	DDRB _b 7	DDRB _b 6	DDRB _b 5	DDRB _b 4	DDRB _b 3	DDRB _b 2	DDRB _b 1	DDRB _b 0

TABLE 5.
Data Register A operation

Data Flow	DDRA _b x = 0 (input)		DDRA _b x = 1 (output)	
	ACR _b 0 = 0	ACR _b 0 = 1	ACR _b 0 = 0	ACR _b 0 = 1
Read IRA	μP reads logic level of port pin transparently	μP reads logic level of port pin transparently until an active signal is applied on CA1, which latches the state of the port pin until the port is read.	μP reads logic level of port pin transparently	μP reads logic level of port pin transparently until an active signal is applied on CA1, which latches the state of the port pin until the port is read.
Write ORA	logic level of pins not affected until direction of pin is changed*	logic level of pins not affected until direction of pin is changed	logic level of output pins follows logic level written into ORA	logic level of output pins follows logic level written into ORA

*may be continually rewritten, retaining last data written

TABLE 6.
Data Register B operation

Data Flow	DDRB _b x = 0 (input)		DDRB _b x = 1 (output)	
	ACR _b 1 = 0	ACR _b 1 = 1	ACR _b 1 = 0	ACR _b 1 = 1
Read IRB	μP reads logic level of port pin transparently	μP reads logic level of port pin transparently until an active signal is applied on CB1, which latches the state of the port pin until the port is read.	μP reads logic level written to the ORB, not what may be on the port pin.	μP reads logic level written to the ORB, not what may be on the port pin.
Write ORB	logic level of pins not affected until direction of pin is changed*	logic level of pins not affected until direction of pin is changed	logic level of output pins follows logic level written into ORB	logic level of output pins follows logic level written into ORB

*may be continually rewritten, retaining last data written

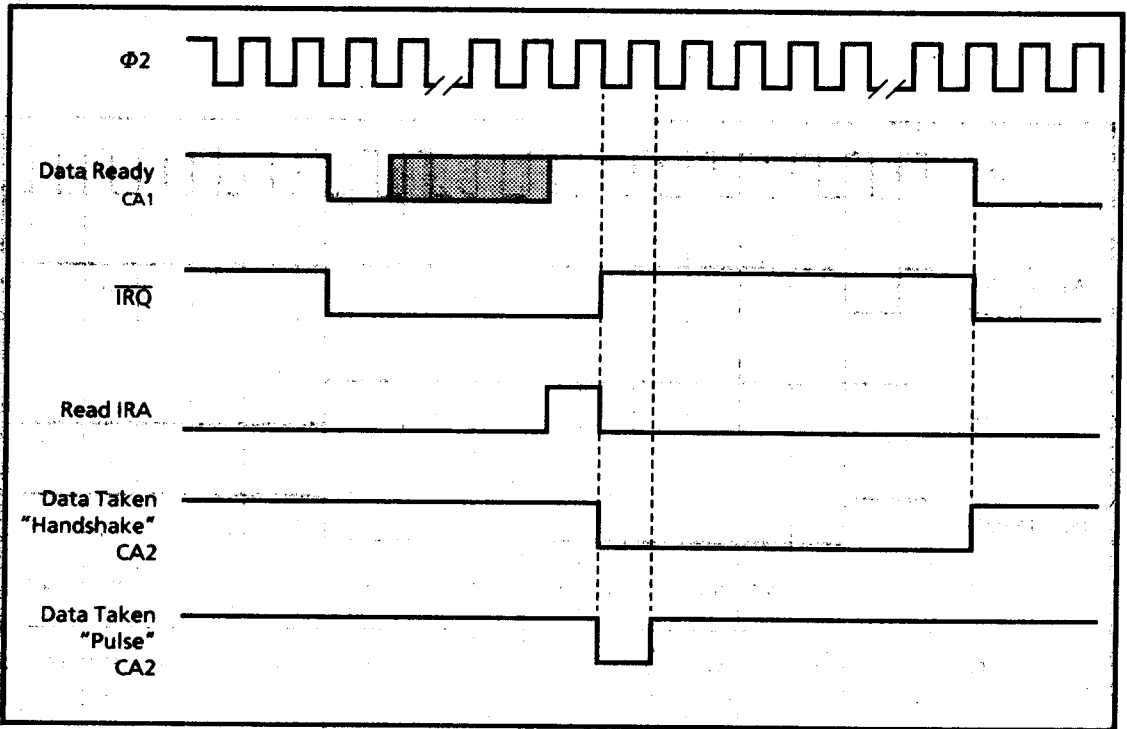


Figure 1. Read Handshake Timing (Port A only)

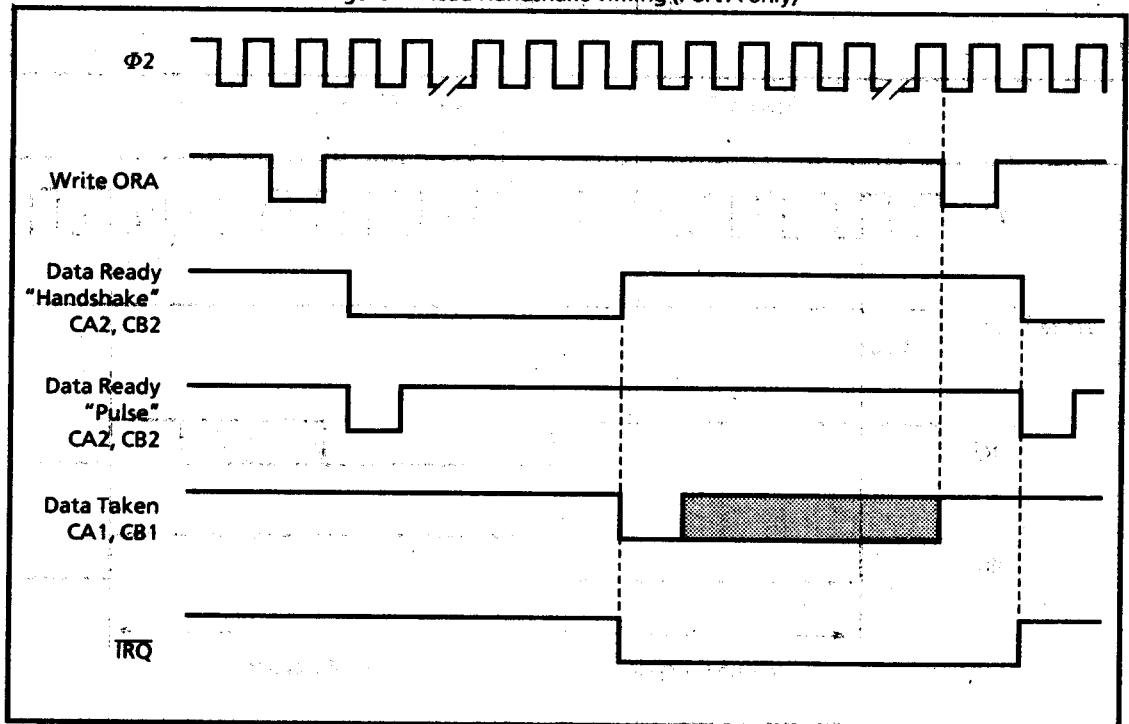


Figure 2. Write Handshake Timing

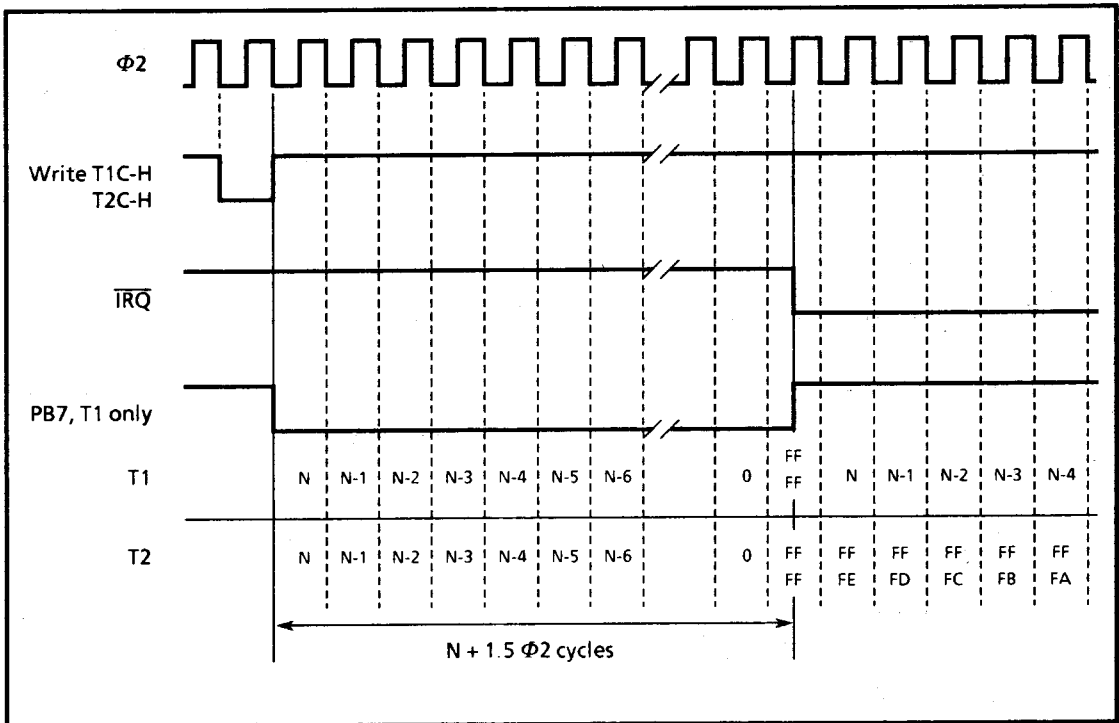


Figure 3. Timer 1 and Timer 2 Single Pass Mode

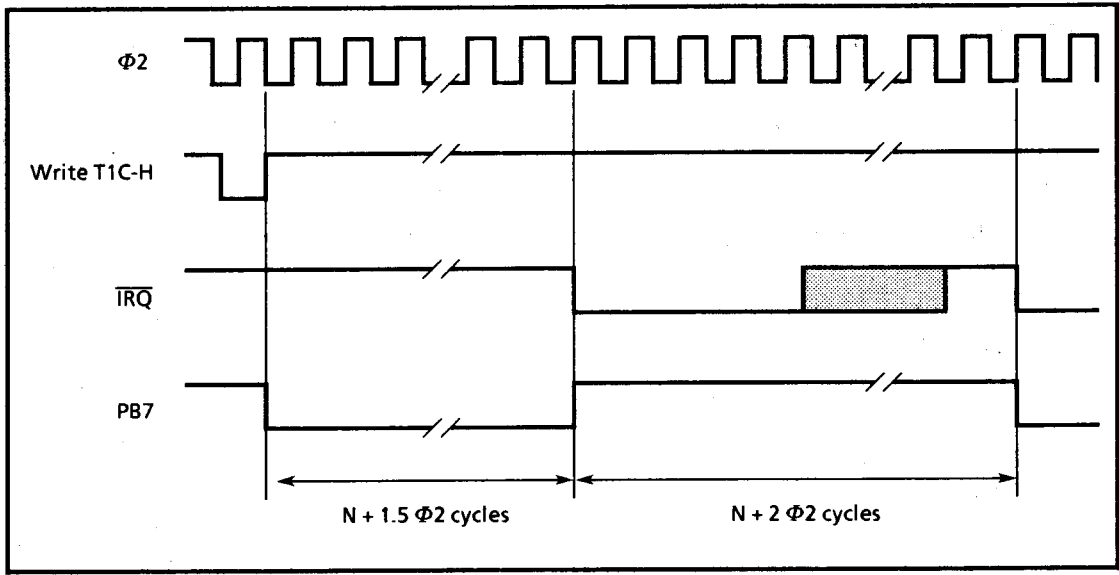


Figure 4. Timer 1 Free Run Mode

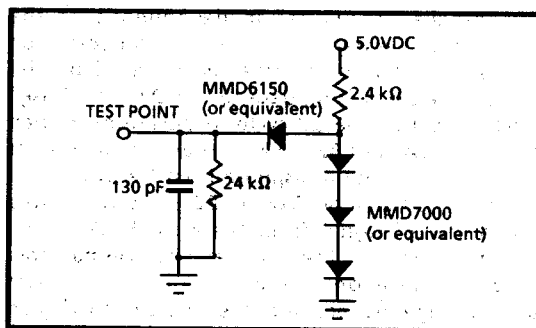


Figure 5. Test load for all pins except IRQ

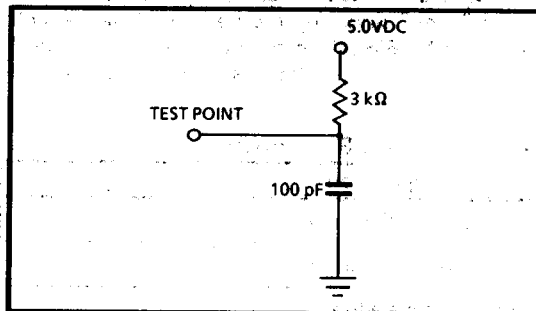


Figure 6. Test load for IRQ

FUNCTIONAL DESCRIPTION

The MD65SC22 is a system utility device, combining multiple functions into one component. The MD65SC22 provides 2 bidirectional, parallel ports (8 bit); a bidirectional serial port; and 2 timers (16 bits each). Each function is qualified by a number of powerful and flexible user modes. Access and control of the MD65SC22 utility is provided through a microprocessor interface and 16 programmable registers. Complementing this interface, a maskable interrupt capability may be used to notify the microprocessor of real time events. Two registers are provided to qualify the possible sources of an interrupt, and to determine which source originated an interrupt.

Parallel Port Operation (Port A and Port B)

There are 7 registers that control and report the state of parallel ports A and B. The determination of a port pin as an input or an output is performed by the contents of the Data Direction Registers (DDRA and DDRB). Writing a bit in a DDR to a logical '1' defines the corresponding pin of the port as an output. Conversely, writing a logical '0' to the bit causes the port pin to be an input. DDRA₀ (bit 0

in DDRA) controls the direction of pin PA0, DDRA₁ controls the direction of pin PA1, etc., up to DDRA₇ controlling PA7. Port B pins follow the same conventions for mapping to DDRB bits. The contents of the DDRs may be read back by the microprocessor.

The Data Registers (ORA-B and IRA-B) control and monitor the logic level of their respective pins. The bits of these registers are mapped to the pins of the ports in the same manner as the DDRs. If a parallel port pin is defined as an output, the logic level of the pin follows the logic level written into the corresponding bit in the port's OR. When the pin is defined as an input, writing to the OR has no effect, the state of the pin may only be monitored. Changing the pin from an input to an output will cause the logic level of the output to follow the last logic level written to the OR bit.

Read access to individual bits in the OR and the IR is determined by the appropriate bit in the DDR. As well, there are differences between Port A and Port B. Port B pins configured as outputs will only return the last logic level written to them. Port B pins configured as inputs, and Port A pins configured as both inputs and outputs have 2 modes in which they may monitor data: transparent mode and latch mode. In transparent mode, reading an IR bit or ORA bit always returns the actual logic level present on the parallel port pin. In latch mode, an active transition on CA1 or CB1 (CA1 for port A and CB1 for port B) will latch the current logic level of the pin into its respective IR bit or ORA bit, until it is read by the microprocessor. After the bit has been read, and until the next active transition of CA1 or CB1, each bit follows the logic level of its pin as in transparent mode.

Latch mode may be enabled or disabled by 2 bits in the Auxiliary Control Register (ACR): ACR₀ (Port A) and ACR₁ (Port B). Writing a logical '0' to these bits disables the latching of the parallel ports, and logical '1' enables latching. Figure 7 shows the input/output circuitry of each of the parallel port pins.

Handshaking

The Control pins (CA1, CA2, CB1 and CB2) have the task of providing handshaking for data transfers (via the MD65SC22) between the controlling microprocessor and another device. The various operating modes of the Control lines are determined by the contents of the Peripheral Control Register (PCR). PCR₀ and PCR₄ define the

active edge of the CA1 and CB1 inputs respectively. PCR_b1-3 determine the operation of the CA2 pin, and PCR_b5-7 determine the operation of the CB2 pin.

Port A may be used for handshaking data transfers in both the microprocessor to peripheral device direction (write) and in the peripheral device to microprocessor direction (read). Port B only provides handshaking in the microprocessor to peripheral device direction. It should be made clear that handshaking only occurs in 2 out of a possible 8 modes for the CA2 and the CB2 pins. These are clearly shown in Table 7 as the "Handshake mode" and the "Pulse mode". The setting of the pertinent bits in the PCR for these modes as well as the other modes of the CA2 and CB2 lines are shown.

The protocol for a controlled data transfer in "Handshake" or "Pulse" mode depends on the direction of the transfer. A "write" (supported on Port A and Port B) transfer is initiated by the microprocessor writing data to the OR. In "Pulse" mode, a pulse (one ϕ 2 cycle in duration) is then output on CA2 or CB2. In Handshake mode, CA2 or CB2 goes low until a response from the peripheral device. This signal on CA2 or CB2 is equivalent to a "Data Ready" signal from the MD65SC22 to the peripheral device. The peripheral device may now read the data on the port's pins, and must acknowledge the receipt of the data by applying an active edge on the CA1 or CB1 line. If the "Handshake" mode is enabled, application of the "Data Taken" signal by the peripheral device will cause the MD65SC22 to remove the "Data Ready" signal. "Data Taken" also sets the interrupt flag for

TABLE 7.
Peripheral Control Register (CA1, CA2, CB1, CB2 control)

b7	b6	b5	b4	b3	b2	b1	b0	Operation
x	x	x	x	x	x	x	0	CA1 Interrupt control, negative active edge
x	x	x	x	x	x	x	1	CA1 Interrupt control, positive active edge
x	x	x	x	0	0	0	x	CA2 control, input, negative active edge
x	x	x	x	0	0	1	x	CA2 control, input, negative active edge, not cleared by read of O/IRA*
x	x	x	x	0	1	0	x	CA2 control, input, positive active edge
x	x	x	x	0	1	1	x	CA2 control, input, positive active edge, not cleared by read of O/IRA*
x	x	x	x	1	0	0	x	CA2 control, output, "Handshake" mode
x	x	x	x	1	0	1	x	CA2 control, output, "Pulse" mode
x	x	x	x	1	1	0	x	CA2 control, output low
x	x	x	x	1	1	1	x	CA2 control, output high
x	x	x	0	x	x	x	x	CB1 Interrupt control, negative active edge
x	x	x	1	x	x	x	x	CB1 Interrupt control, positive active edge
0	0	0	x	x	x	x	x	CB2 control, input, negative active edge
0	0	1	x	x	x	x	x	CB2 control, input, negative active edge, not cleared by read of O/IRB*
0	1	0	x	x	x	x	x	CB2 control, input, positive active edge
0	1	1	x	x	x	x	x	CB2 control, input, positive active edge, not cleared by read of O/IRB*
1	0	0	x	x	x	x	x	CB2 control, output, "Handshake" mode
1	0	1	x	x	x	x	x	CB2 control, output, "Pulse" mode
1	1	0	x	x	x	x	x	CB2 control, output low
1	1	1	x	x	x	x	x	CB2 control, output high

*See section on IFR function

CA1 or CB1, which will cause an interrupt of the microprocessor if that particular interrupt is enabled. The interrupt may be removed by the microprocessor writing to the port.

A "read" data transfer (supported on only Port A) follows a very similar pattern to the "write" protocol. A "read" data transfer is initiated by the peripheral device by presenting an active edge to the CA1 input ("Data Ready") when the data from the peripheral is present on Port A pins. This will set the interrupt flag for CA1, and if this interrupt is enabled, the microprocessor will be interrupted. The microprocessor may read the data at Port A, thereby removing the interrupt and presenting a "Data Taken" signal or pulse (one ϕ_2 cycle in duration) on CA2. "Data Taken" is cleared by the next active edge of "Data Ready" from the peripheral device.

In Port A operation, the type of handshaken data transfer performed ("read" or "write") depends on what event occurs first after the last data transfer; a write into ORA by the microprocessor, or a "Data Ready" signal from the peripheral device. For data transfers that do not require handshaking, there are 6 modes of CA2, CB2 control that do not follow the previously described protocol. As illustrated in Table 7, the logic level of CA2 or CB2 may be placed high or low, independent of any action from the peripheral device. CA2 and CB2 may also be configured as inputs that trigger an interrupt to the microprocessor. Selection is available between which edge of an input (positive or negative) causes interrupt triggering, and the manner in which the interrupt is cleared is also selectable (Table 7). Interrupts from the CA2 and CB2 inputs may be cleared by reading their respective IRs; or writing

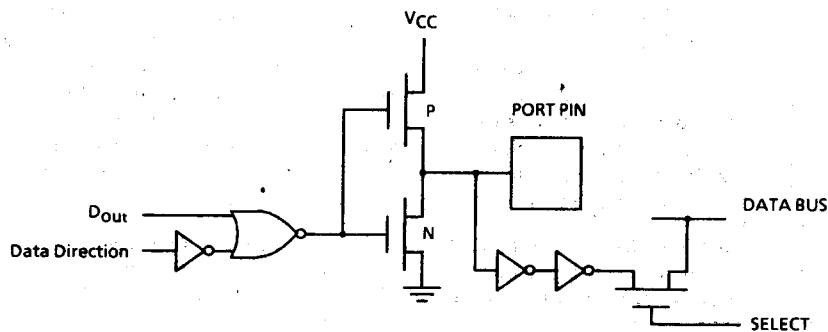


Figure 7a. Port A Equivalent Circuit.

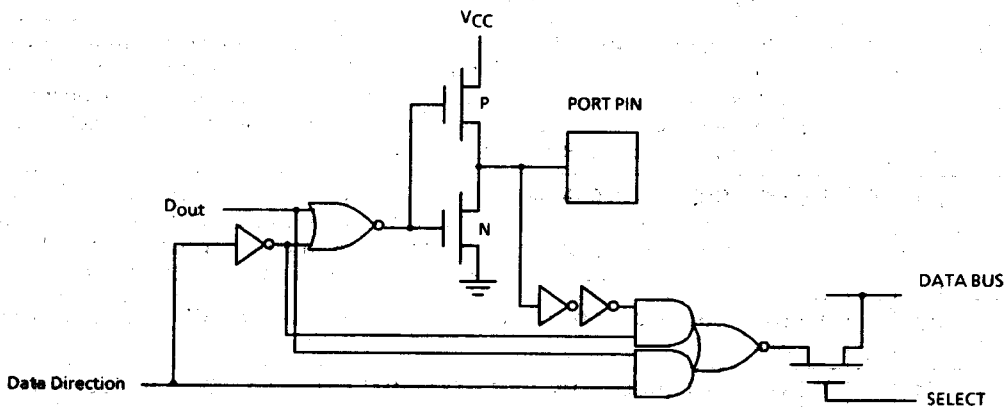


Figure 7b. Port B Equivalent Circuit.

Figure 7. Port A and Port B Equivalent Circuits.

into the Interrupt Flag Register (IFR) may be made mandatory in order to clear the interrupt. This latter method of clearing interrupts is described in the section on the IFR.

A final register is provided for use as a parallel port. This register is equivalent to ORA and IRA, however data transfers performed through this register may not utilize the handshaking protocol (see table 2).

Timer 1 Operation

Timer 1 (T1) is an interval timer, which decrements from a programmable 16-bit count to zero. When the count reaches zero and subsequently rolls over to FFFF_H, an interrupt flag in the IFR is set, interrupting the μ P if enabled in the Interrupt Enable Register (IER). T1 decrements every full cycle of the ϕ 2 clock. The timer is divided into a low count and a high count, each of which are separately accessible.

TABLE 8.
Shift register operation

Mode	ACR state			Operation
	b4	b3	b2	
0	0	0	0	SR DISABLED - SR interrupt flag disabled, and CB1 and CB2 controlled by contents of PCR.
1	0	0	1	SHIFT IN UNDER T2 CONTROL - CB1 is an output and CB2 is an input. CB1 is normally high. A read or a write to the SR initializes shift operation. CB1 changes state on every T2 timeout (N + 2 cycles of ϕ 2 and coincident with the rising edge of ϕ 2; note that only the lower byte of the timer is used in the timeout) after the read or write of the SR. Data at CB2 should be stable until the falling edge of ϕ 2 (which shifts in data) following a rising edge of CB1. After 8 pulses on CB1, the interrupt flag will be set and CB1 will remain high. If enabled in the IER, the interrupt pin will go low on the falling edge of ϕ 2 following the last rising edge of CB1. This interrupt is cleared by the next initialization of the shift operation (see fig. 8).
2	0	1	0	SHIFT IN UNDER CONTROL OF ϕ2 - Similar to mode 1. CB1 is an output and CB2 is an input. CB1 is toggled on the rising edge of ϕ 2 after shift initialization, providing a frequency half that of ϕ 2. All other operation is the same as mode 1 (see fig. 9).
3	0	1	1	SHIFT IN UNDER CONTROL OF EXTERNAL CB1 CLOCK - CB1 and CB2 are both inputs. Data is shifted in on each falling edge of the first ϕ 2 cycle after the rising edge of the signal on CB1. Since CB1 may not be synchronized with ϕ 2, data must be held at CB2 for at least one full ϕ 2 cycle after the CB1 rising edge. Initialization and interrupt operation is the same as modes 1 and 2 (see fig. 10).
4	1	0	0	SHIFT OUT FREE RUN AT T2 RATE - Same as mode 5 except no interrupt, no initialization. When data is written to the SR, it is shifted out as in mode 5, but is shifted back into the most significant bit. CB1 continues toggling and no interrupt flag is set after 8 T2 timeouts. The same data will continue to be shifted out until new data is written to the SR (see fig. 11).
5	1	0	1	SHIFT OUT UNDER CONTROL OF T2 - CB1 and CB2 are both outputs. Similar to mode 1, but CB2 is now an output. Last data is maintained on CB2 until next falling edge of ϕ 2 after falling edge of CB1. Initialization and interrupt operation is the same as mode 1, but last data remains on CB2 until next initialization (see fig. 12).
6	1	1	0	SHIFT OUT UNDER CONTROL OF ϕ2 - Same as mode 5, but CB1 behaves as in mode 2 (see fig. 13).
7	1	1	1	SHIFT OUT UNDER CONTROL OF EXTERNAL CB1 CLOCK - CB1 is an input and CB2 is an output. Similar clocking operation as mode 3, data is shifted out on the first falling edge of ϕ 2 after the falling edge of CB1. Data remains on CB1 until next shift. Initialization and interrupt are the same as the mode 6.

To alleviate the synchronization problem of transferring 16 bits of data to the counter simultaneously, the low order count of T1 is always latched when written by the μ P (a write to T1C-L or T1L-L). When the count for the high order byte is written (a write to T1C-H), the low order byte is transferred from its latch to the timer. This write to the high order count initiates a count-down on the next cycle of ϕ 2 immediately following.

A latch for the high order count of the timer is also provided (T1L-H), because T1 reinitiates its count automatically in one mode of operation. This causes a requirement for the data to be available repeatedly. Writing to this latch does not transfer the data to the count until the current count

decrements to zero. Writing to T1C-L and T1L-L are equivalent operations, however reading T1C-L will return the current state of the low order count, just as reading T1C-H returns the current state of the high order count. Reading T1L-L and T1L-H will merely return the values written to those latches by the μ P. Writing to T1C-H and reading from T1C-L both clear the interrupt flag (clearing the interrupt to the μ P if it is enabled). Any access of the T1L registers will not affect the operation of the interrupt mechanism. A passive read or write of the timer latches, that doesn't affect the current count of the timer, will prove useful in the "continuous" mode of operation.

T1 allows 2 modes of operation, the "single pass mode" and the "continuous mode", selected by the

TABLE 9.
Interrupt Flag Register

IFR bit	Source	Set by	Cleared by
0	CA2	CA2 active edge	Read or Write of O/IRA* or set IFR bit
1	CA1	CA1 active edge	Read or Write of O/IRA or set IFR bit
2	SHIFT REG	Completion of 8 Shift Register shifts	Read or Write of SR or set IFR bit
3	CB2	CB2 active edge	Read or Write of O/IRB* or set IFR bit
4	CB1	CB1 active edge	Read or Write of O/IRB or set IFR bit
5	TIMER 2	Time out of T2	Read T2 low or Write T2 high, or set IFR bit
6	TIMER 1	Time out of T1	Read T1 low or Write T1 high, or set IFR bit
7	IRQ	Any enabled interrupt	Clearing all enabled interrupts

*See Table 7. If it is indicated there that the flag will not be cleared by a Read or Write of O/IRA or O/IRB, then the flag must be cleared by writing a logic '1' to the bit position in the IFR occupied by the flag. There are several modes of Port A and Port B operation that require this method of flag clearing.

TABLE 10.
Interrupt Enable Register

IER bit	ENABLE DISABLE	Disabled by	Enabled by
0	CA2	Write 0xxxxx1 ₂ to IER, returns 1xxxxx1 ₂	Write 1xxxxx1 ₂ to IER, returns 1xxxxx0 ₂
1	CA1	Write 0xxxx1x ₂ to IER, returns 1xxxx1x ₂	Write 1xxxx1x ₂ to IER, returns 1xxxx0x ₂
2	SHIFT REG	Write 0xxxx1xx ₂ to IER, returns 1xxxx1xx ₂	Write 1xxxx1xx ₂ to IER, returns 1xxxx0xx ₂
3	CB2	Write 0xxx1xxx ₂ to IER, returns 1xxx1xxx ₂	Write 1xxx1xxx ₂ to IER, returns 1xxx0xxx ₂
4	CB1	Write 0xx1xxxx ₂ to IER, returns 1xx1xxxx ₂	Write 1xx1xxxx ₂ to IER, returns 1xx0xxxx ₂
5	TIMER 2	Write 0x1xxxxx ₂ to IER, returns 1x1xxxxx ₂	Write 1x1xxxxx ₂ to IER, returns 1x0xxxxx ₂
6	TIMER 1	Write 01xxxxxx ₂ to IER, returns 11xxxxxx ₂	Write 11xxxxxx ₂ to IER, returns 10xxxxxx ₂

Note: x is intended to represent don't care in all binary representations, returned data is data read subsequent to enable or disable of an interrupt.

state of ACR_{b6} . In both modes, if DDR_{b7} and ACR_{b7} are 1, pin PB7 may be controlled by the timer. Otherwise, control reverts to the parallel port. In "single pass mode", the timer will decrement from the programmed count to zero, set the interrupt flag, and disable further interrupts. The interrupt may be cleared by reading T1C-L or by reading T1C-H, but further interrupts are only made possible by initiating another countdown (a write to T1C-H). Writing to T1C-H also effectively loads register T1L-H with the same data. If $ACR_{b7} = 1$, and $DDR_{b7} = 1$, then PB7 will be low for the duration of the single pass countdown ($N + 1.5$ cycles of $\phi 2$, where N is the contents of the low count and the high count), then go high until the next count is initiated. Time from count initiation to interrupt flag set is the same as the period of the PB7 negative pulse.

In "continuous mode" ($ACR_{b6} = 1$), rather than disable interrupts after the zero count is reached,

the count is transferred into the counter from the high and low order latches, and the timer starts the count over. PB7 alternates between a high and a low on each timeout. The interrupt on timeout may be cleared without affecting the countdown, by reading T1C-L. Providing the ability to alter the contents of the latches without affecting the current count allows the period of the next timeout to be varied. This provides the facility for generating complex waveforms on PB7. The waveform on PB7 in continuous mode begins with a low going half cycle of $N + 1.5 \phi 2$ cycles duration, where N is the value of the count. Subsequent half cycles will be $N + 2 \phi 2$ cycles in duration. Timeout can be "postponed" by writing to T1C-H before timeout occurs. This effectively starts the count immediately at its new value. The ability to do this is valuable for use in "Watchdog" or "Sanity" timer functions (if the interrupt occurs, a recovery process begins).

TABLE 11.
Auxiliary Control Register

b7	b6	b5	b4	b3	b2	b1	b0	Operation
x	x	x	x	x	x	x	0	Port A latch disable
x	x	x	x	x	x	x	1	Port A latch enable
x	x	x	x	x	x	0	x	Port B latch disable
x	x	x	x	x	x	1	x	Port B latch enable
x	x	x	0	0	0	x	x	Shift register disabled
x	x	x	0	0	1	x	x	Shift register shift in under control of T2
x	x	x	0	1	0	x	x	Shift register shift in under control of $\phi 2$
x	x	x	0	1	1	x	x	Shift register shift in under control of external clock
x	x	x	1	0	0	x	x	Shift register shift out free running at T2 rate
x	x	x	1	0	1	x	x	Shift register shift out under control of T2
x	x	x	1	1	0	x	x	Shift register shift out under control of $\phi 2$
x	x	x	1	1	1	x	x	Shift register shift out under control of external clock
x	x	0	x	x	x	x	x	T2 Timer timed interrupt
x	x	1	x	x	x	x	x	T2 Timer count down with pulses on PB6
0	0	x	x	x	x	x	x	T1 Timer timed interrupt each time T1 is loaded (PB7 disabled)
0	1	x	x	x	x	x	x	T1 Timer continuous interrupts (PB7 disabled)
1	0	x	x	x	x	x	x	T1 Timer timed interrupt each time T1 is loaded, PB7 one shot output
1	1	x	x	x	x	x	x	T1 Timer continuous interrupts, square wave output on PB7

Timer 2 Operation

Timer 2 operates in 2 modes: a single pass mode similar to that of T1 ($ACR_{b5} = 0$), and a pulse count mode ($ACR_{b5} = 1$). Because there is no "continuous" mode operation, a high order byte latch is not needed to store the value of the high order count for sequential timeouts. Again, the interrupt flag may be cleared by reading the T2C-L and writing to T2C-H reinitializes the timeout as well as clearing the interrupt flag. Reading either T2C-L or T2C-H transfers the contents of the timer onto the data bus. Interrupt occurs $N + 1.5 \phi_2$ cycles after timeout initialization just as in T1 operation, but, although interrupts are disabled until reenabled by writing to T2C-H, the count rolls over to $FFFF_H$ and continues to decrement. The user may use this feature to determine how long it took to service the interrupt. Response time is measured by subtracting the count of the timer from $FFFF_H$.

In Pulse counting mode, the count of the timer is decremented by negative pulses on PB6. PB6 must be configured as an input by DDR_{b6} , and $ACR_{b5} = 1$. The interrupt flag is set by the pulse that rolls the count in T2 over to $FFFF_H$. As in other modes, the interrupt may be cleared by reading T2C-L or T2C-H, but to enable subsequent interrupts T2C-H must be written to.

Shift Register Operation

Parallel /Serial I/O operations are made possible by the provision of an 8-bit serial Shift Register (SR). The serial port uses the 2 port B control pins (CB1 and CB2) when operating. CB1 is used for synchronizing the shifting operation. In some modes it is used as an output, providing shift timing for external circuitry; in other modes it is used by the external circuitry to control the shift operation of the MD65SC22. CB2 is the data stream, and can be configured as either an input or an output.

When being used as an output, data in the SR is shifted from the least significant bit, towards the most significant bit, through the intervening bits. From the most significant bit, the data is shifted out of CB2. This direction of shifting produces a serial data stream starting with the most significant bit of the SR contents and ending with the least

significant bit of the SR contents. When CB2 is being used as an input, the same shift direction is followed, so the first bit in the serial stream will become the most significant bit in the SR after 8 shifts. The order of bit transmission and reception should be taken into consideration when trying to use the MD65SC22 to communicate with a device that uses a standard serial communication protocol (MD65SC51 ACIA), as these devices shift the least significant bit out first.

The operating mode of the SR is determined by the state of several bits in the ACR: ACR_{b4} , ACR_{b3} and ACR_{b2} . For a description of the operating modes of the SR, see Table 8.

Interrupt Registers (IFR and IER)

Control and monitoring of the many different interrupts that may originate from the MD65SC22 is implemented by the Interrupt Flag Register and the Interrupt Enable Register. Specific events have been described that set (logic '1') a bit in the interrupt flag register. Such an event does not necessarily interrupt the microprocessor. To assert the interrupt pin, the bit in the IER that coincides with the set flag must be set (by a write of a logic 1 from the μP). IFR_{b7} reflects the state of the interrupt pin. If the interrupt pin is asserted, IFR_{b7} will be set (logic '1'), otherwise it will be clear.

The IFR may be read to determine the origin of an interrupt, or it may be written to. Writing to the IFR provides an alternate method of clearing an interrupt flag (modes 1 & 3 - CA2 and CB2). This may be done by writing a logic '1' to the bit intended to be cleared. IFR_{b7} may not be cleared in this manner, it may only be cleared if all other flags in the register are cleared, or disabled in the IER.

IER is also a read/write register. As explained, writing to the register enables or disables interrupts to the μP . If IER_{b7} is a 0, when writing a byte of information to IER, any other bit in the byte that is a logic '1' clears its corresponding interrupt enable bit. When a 1 is written to IER_{b7} , any other bit in the byte that is a logic '1' sets its corresponding interrupt enable (set = enable; clear = disable). Reading the register returns the enabled/disabled information (enabled = logic '1'; disabled = logic '0') written to the register, except for IER_{b7} . This bit always returns a logic '1'.

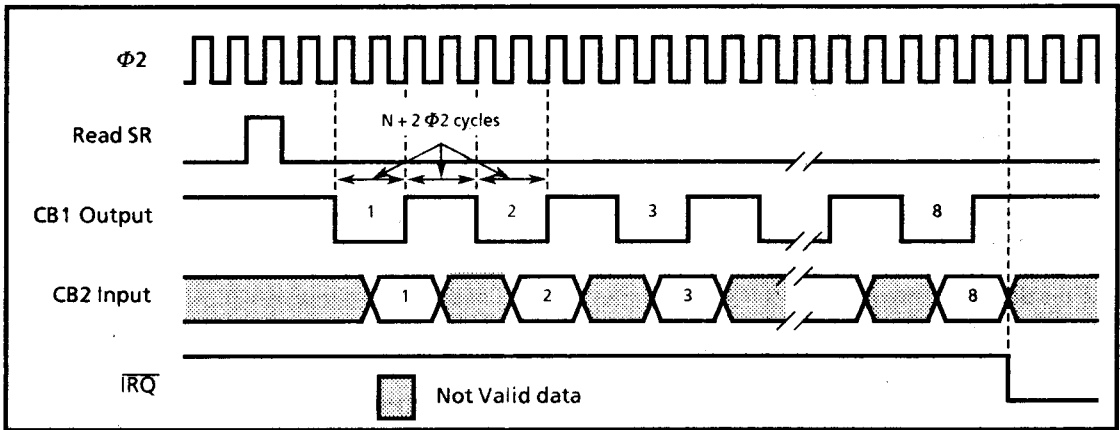


Figure 8. Shift Register timing in mode 1

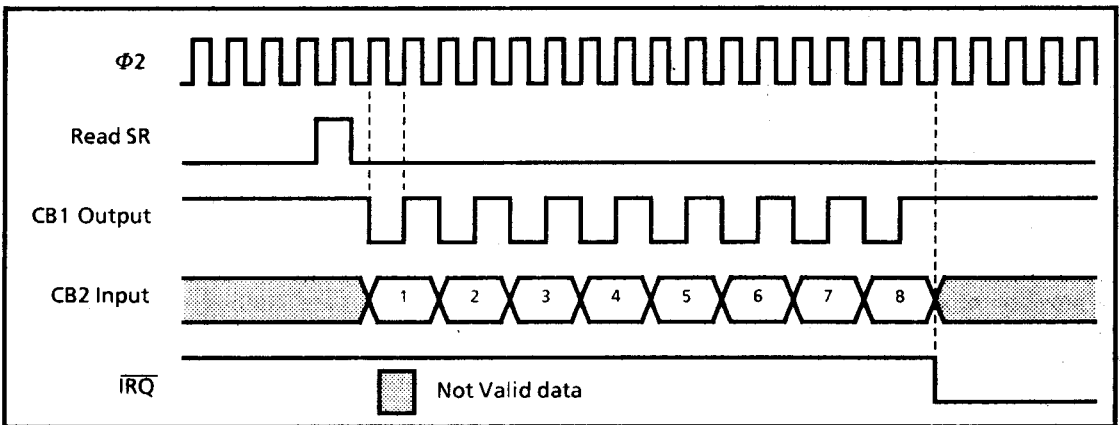


Figure 9. Shift Register timing in mode 2

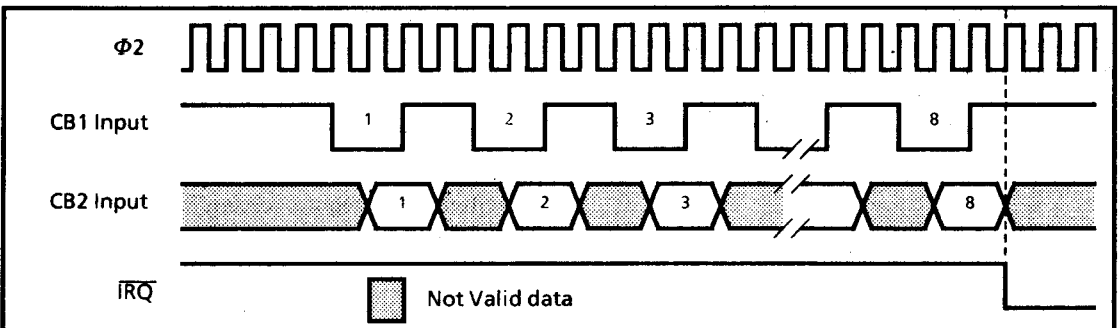


Figure 10. Shift Register timing in mode 3

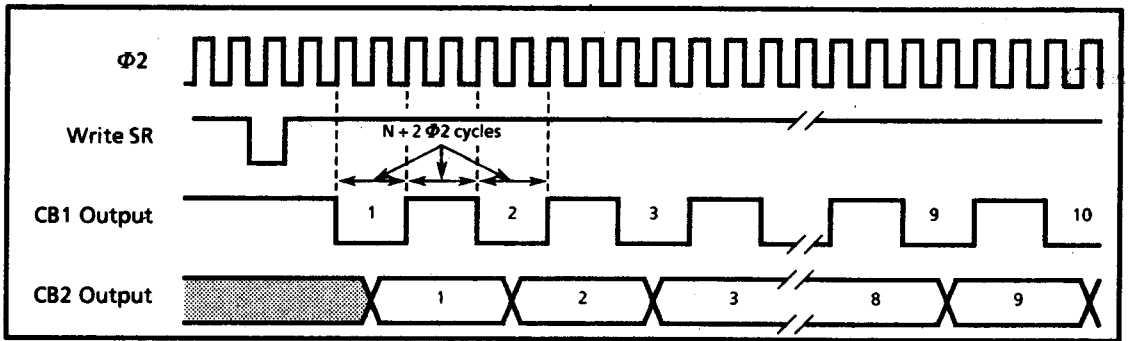


Figure 11. Shift Register timing in mode 4

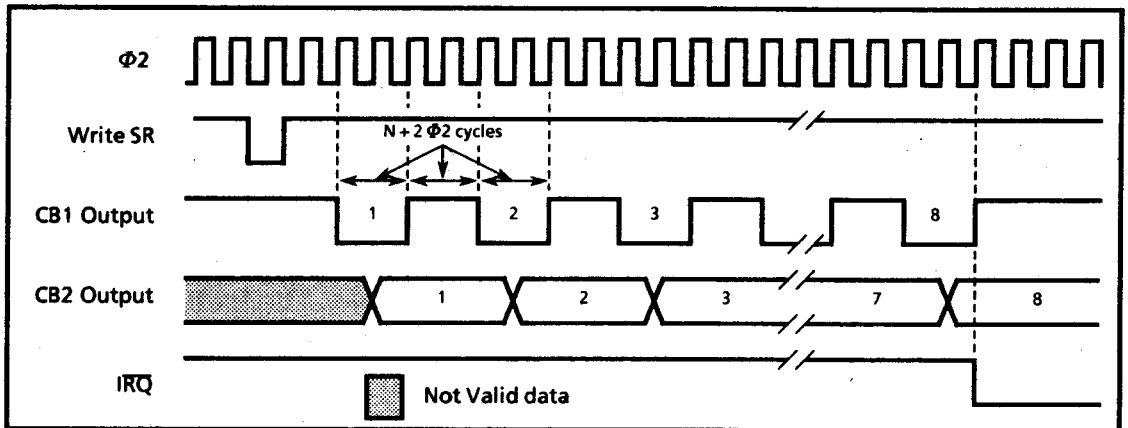


Figure 12. Shift Register timing in mode 5.

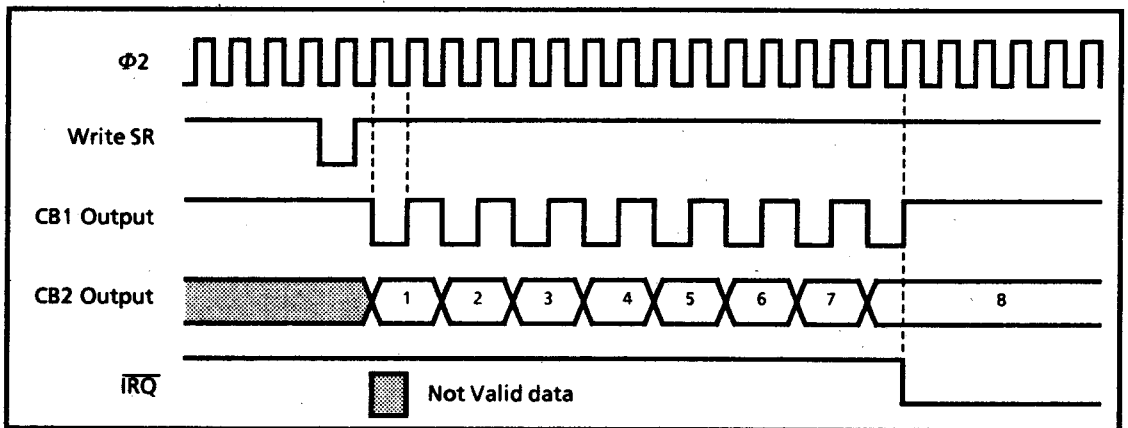


Figure 13. Shift Register timing in mode 6

Note: Shift register mode 7 has similar timing characteristics to mode 6 except CB1 is an input, and is not dependent $\Phi 2$. IRQ goes low on the next rising edge of $\Phi 2$ after the rising edge of the eighth CB1 Pulse