

# MSM521216

**65,536-Word × 16-Bit CMOS STATIC RAM**

## DESCRIPTION

The MSM521216 is a 65,536-word by 16-bit CMOS fast static RAM featuring a single 3.3 V power supply operation and direct LVTTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM521216 can be used in the high-speed operation of an access time 20 ns due to adopting a high-performance CMOS technology. In addition, the MSM521216 is provided with a chip enable signal ( $\overline{CE}$ ) suited to the power-down function, an output enable signal ( $\overline{OE}$ ) suited to the I/O bus line control, and a byte select signal ( $\overline{LB}$ ,  $\overline{UB}$ ) that can independently control the input/output of a lower byte and an upper byte.

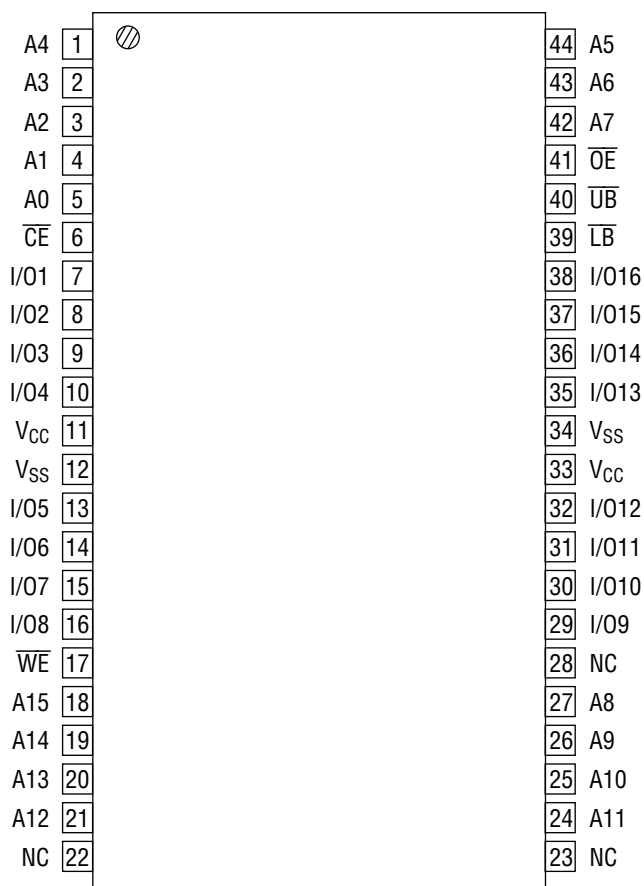
## FEATURES

- 65,536-word × 16-bit configuration
- Single 3.3 V power supply
- Fully static operation
- Operating temperature range: Ta = 0°C to 70°C
- Power dissipation
  - Standby: 2 mA (Max.)
  - Operation:
    - 20 220 mA (Max.)
    - 25 200 mA (Max.)
    - 30 180 mA (Max.)
- Access time:
  - 20 20 ns (Max.)
  - 25 25 ns (Max.)
  - 30 30 ns (Max.)
- (Input/Output) LVTTL compatible
- Power-down function by chip enable signal
- 3-state output
- Lower and upper bytes can be controlled independently
- Package:
  - 44-pin 400 mil plastic TSOP (Type II) (TSOPII44-P-400-0.80-K) (Product: MSM521216-xxTS-K)  
xx indicates speed rank.

## PRODUCT FAMILY

| Family       | Access Time (Max.) | Package                    |
|--------------|--------------------|----------------------------|
| MSM521216-20 | 20 ns              | 400 mil<br>44-pin TSOP(II) |
| MSM521216-25 | 25 ns              |                            |
| MSM521216-30 | 30 ns              |                            |

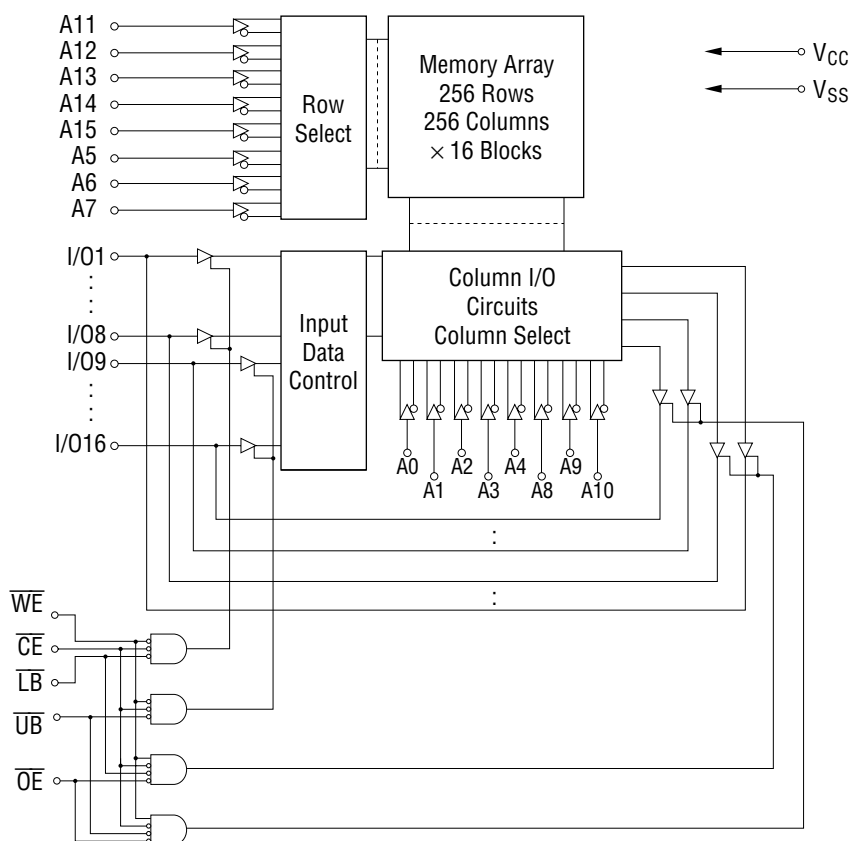
## PIN CONFIGURATION (TOP VIEW)



44-Pin Plastic TSOP (II)  
(K Type)

| Pin Name                          | Function          |
|-----------------------------------|-------------------|
| A0 - A15                          | Address Input     |
| I/O1 - I/O16                      | Data Input/Output |
| $\overline{CE}$                   | Chip Enable       |
| $\overline{WE}$                   | Write Enable      |
| $\overline{OE}$                   | Output Enable     |
| $\overline{LB}$ , $\overline{UB}$ | Byte Data Select  |
| V <sub>CC</sub> , V <sub>SS</sub> | Power Supply      |
| NC                                | No Connection     |

### BLOCK DIAGRAM



## FUNCTION TABLE

| Operating Mode | $\overline{\text{CE}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | $\overline{\text{LB}}$ | $\overline{\text{UB}}$ | I/O1 - I/O8 | I/O9 - I/O16 | Power Mode |
|----------------|------------------------|------------------------|------------------------|------------------------|------------------------|-------------|--------------|------------|
| Non Selectable | H                      | X                      | X                      | X                      | X                      | High-Z      | High-Z       | Standby    |
| Read Cycle     | L                      | H                      | H                      | X                      | X                      | High-Z      | High-Z       | Active     |
|                | L                      | H                      | L                      | L                      | L                      | Data Read   | Data Read    | Active     |
|                | L                      | H                      | L                      | L                      | H                      | Data Read   | High-Z       | Active     |
|                | L                      | H                      | L                      | H                      | L                      | High-Z      | Data Read    | Active     |
|                | L                      | H                      | L                      | H                      | H                      | High-Z      | High-Z       | Active     |
|                | L                      | L                      | X                      | L                      | L                      | Data Write  | Data Write   | Active     |
| Write Cycle    | L                      | L                      | X                      | L                      | H                      | Data Write  | High-Z       | Active     |
|                | L                      | L                      | X                      | H                      | L                      | High-Z      | Data Write   | Active     |
|                | L                      | L                      | X                      | H                      | H                      | High-Z      | High-Z       | Active     |

\*Don't Care ("H" or "L")

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

| Parameter             | Symbol    | Condition                               | Rating                     | Unit             |
|-----------------------|-----------|-----------------------------------------|----------------------------|------------------|
| Power Supply Voltage  | $V_{CC}$  | $T_a = 25^\circ\text{C}$ , for $V_{SS}$ | -0.5 to 4.6                | V                |
| Pin Voltage           | $V_T$     |                                         | $-0.5^*$ to $V_{CC} + 0.5$ | V                |
| Power Dissipation     | $P_D$     | $T_a = 25^\circ\text{C}$                | 1.0                        | W                |
| Operating Temperature | $T_{opr}$ | —                                       | 0 to 70                    | $^\circ\text{C}$ |
| Storage Temperature   | $T_{stg}$ | —                                       | -55 to 125                 | $^\circ\text{C}$ |

\* -2.0 V Min. for pulse width less than 10 ns.

### Recommended Operating Conditions

| Parameter            | Symbol   | Condition                                | Min.  | Typ. | Max.           | Unit |
|----------------------|----------|------------------------------------------|-------|------|----------------|------|
| Power Supply Voltage | $V_{CC}$ | —                                        | 3.0   | 3.3  | 3.6            | V    |
|                      | $V_{SS}$ |                                          | 0     | 0    | 0              | V    |
| Input High Voltage   | $V_{IH}$ | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 2.0   | —    | $V_{CC} + 0.3$ | V    |
| Input Low Voltage    | $V_{IL}$ |                                          | -0.3* | —    | 0.8            | V    |
| Load Capacitance     | $C_L$    | —                                        | —     | —    | 30             | pF   |

\* -2.0 V Min. for pulse width less than 10 ns.

### Capacitance

( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

| Parameter                | Symbol    | Condition              | Min. | Max. | Unit |
|--------------------------|-----------|------------------------|------|------|------|
| Input Capacitance        | $C_I$     | $V_{IN} = 0\text{ V}$  | —    | 8    | pF   |
| Input/Output Capacitance | $C_{I/O}$ | $V_{I/O} = 0\text{ V}$ | —    | 8    | pF   |

Note: This parameter is periodically sampled and not 100% tested.

# DC Characteristics

( $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

| Parameter                         | Symbol     | Condition                                                                                                                                                                            | MSM521216 |      |      | Unit          |
|-----------------------------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|------|------|---------------|
|                                   |            |                                                                                                                                                                                      | Min.      | Typ. | Max. |               |
| Input Leakage Current             | $I_{LI}$   | $V_{IN} = 0 \text{ to } V_{CC}$                                                                                                                                                      | -10       | —    | 10   | $\mu\text{A}$ |
| Output Leakage Current            | $I_{LO}$   | $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or<br>$\overline{WE} = V_{IL}$ or<br>$\overline{UB} = V_{IH}$ or $\overline{LB} = V_{IH}$ ,<br>$V_{OUT} = 0 \text{ to } V_{CC}$ | -10       | —    | 10   | $\mu\text{A}$ |
| Output High Voltage               | $V_{OH}$   | $I_{OH} = -2.0 \text{ mA}$                                                                                                                                                           | 2.4       | —    | —    | V             |
| Output Low Voltage                | $V_{OL}$   | $I_{OL} = 2.0 \text{ mA}$                                                                                                                                                            | —         | —    | 0.4  | V             |
| Standby Power<br>Supply Current   | $I_{CCS}$  | $\overline{CE} \geq V_{CC} - 0.2 \text{ V}$ ,<br>$V_{IN} \leq 0.2 \text{ V}$ or<br>$V_{IN} \geq V_{CC} - 0.2 \text{ V}$                                                              | —         | —    | 2    | mA            |
|                                   | $I_{CCS1}$ | $\overline{CE} = V_{IH}$ , Min. cycle                                                                                                                                                | —         | —    | 20   | mA            |
| Operating Power<br>Supply Current | $I_{CCA}$  | $\overline{CE} = V_{IL}$ ,<br>Min. cycle,<br>$I_{OUT} = 0 \text{ mA}$                                                                                                                | —         | —    | ①    | mA            |

① 521216-20 220 mA  
521216-25 200 mA  
521216-30 180 mA

# AC Characteristics

## Test Conditions

| Parameter                 | Condition                                       |
|---------------------------|-------------------------------------------------|
| Input Pulse Level         | $V_{IH} = 3 \text{ V}$ , $V_{IL} = 0 \text{ V}$ |
| Input Rise and Fall Times | 3 ns                                            |
| Input/Output Timing Level | 1.4 V                                           |
| Output Load               | See Figures                                     |

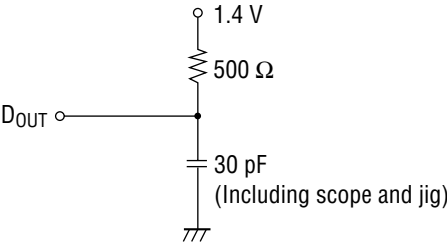


Figure 1 Output Load

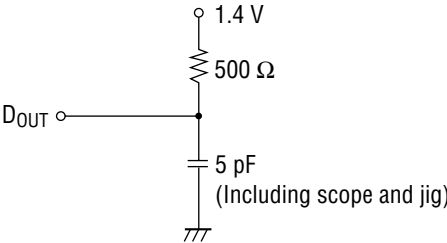


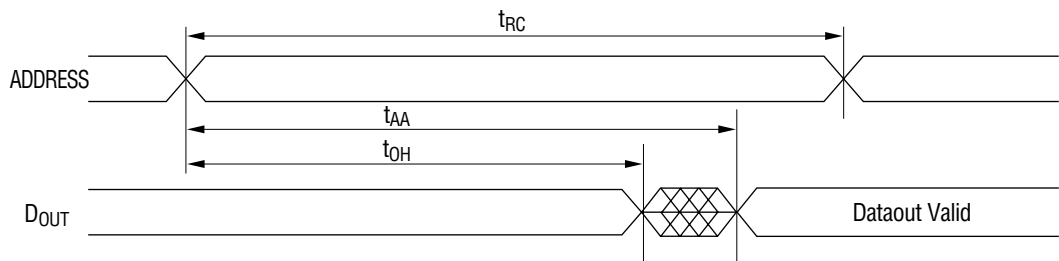
Figure 2 Output Load  
( $t_{OLZ}$ ,  $t_{OHZ}$ ,  $t_{CLZ}$ ,  $t_{CHZ}$ ,  $t_{LBLZ}$ ,  $t_{LBHZ}$ ,  $t_{UBLZ}$ ,  $t_{UBHZ}$ ,  $t_{WLZ}$ ,  $t_{WHZ}$ )

## Read Cycle

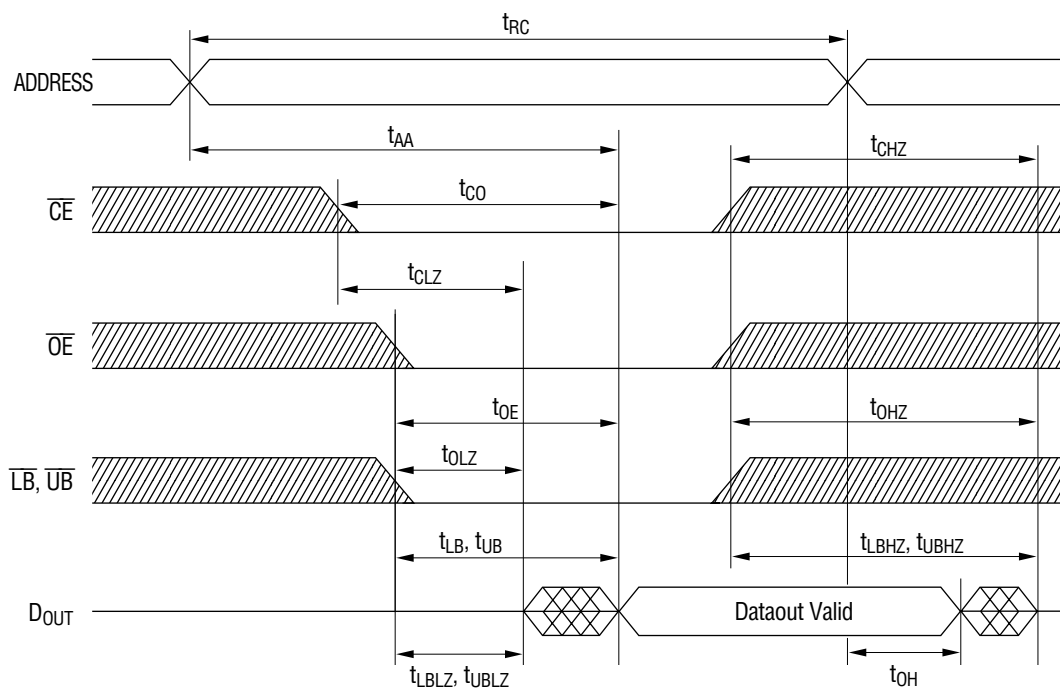
( $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

| Parameter                                             | Symbol                  | MSM521216-20 |      | MSM521216-25 |      | MSM521216-30 |      | Unit |
|-------------------------------------------------------|-------------------------|--------------|------|--------------|------|--------------|------|------|
|                                                       |                         | Min.         | Max. | Min.         | Max. | Min.         | Max. |      |
| Read Cycle Time                                       | $t_{RC}$                | 20           | —    | 25           | —    | 30           | —    | ns   |
| Address Access Time                                   | $t_{AA}$                | —            | 20   | —            | 25   | —            | 30   | ns   |
| $\overline{CE}$ Access Time                           | $t_{CO}$                | —            | 20   | —            | 25   | —            | 30   | ns   |
| $\overline{OE}$ Access Time                           | $t_{OE}$                | —            | 10   | —            | 12   | —            | 15   | ns   |
| $\overline{LB}$ , $\overline{UB}$ Access Time         | $t_{LB}$ , $t_{UB}$     | —            | 10   | —            | 12   | —            | 15   | ns   |
| $\overline{CE}$ to Output in Low-Z                    | $t_{CLZ}$               | 3            | —    | 3            | —    | 3            | —    | ns   |
| $\overline{OE}$ to Output in Low-Z                    | $t_{OLZ}$               | 0            | —    | 0            | —    | 0            | —    | ns   |
| $\overline{LB}$ , $\overline{UB}$ to Output in Low-Z  | $t_{LBLZ}$ , $t_{UBLZ}$ | 0            | —    | 0            | —    | 0            | —    | ns   |
| Output Hold Time from Address Change                  | $t_{OH}$                | 3            | —    | 3            | —    | 3            | —    | ns   |
| $\overline{CE}$ to Output in High-Z                   | $t_{CHZ}$               | —            | 8    | —            | 10   | —            | 12   | ns   |
| $\overline{OE}$ to Output in High-Z                   | $t_{OHZ}$               | —            | 8    | —            | 10   | —            | 12   | ns   |
| $\overline{LB}$ , $\overline{UB}$ to Output in High-Z | $t_{LBHZ}$ , $t_{UBHZ}$ | —            | 8    | —            | 10   | —            | 12   | ns   |

## Address Controlled Read ( $\overline{WE} = H$ , $\overline{CE} = L$ , $\overline{OE} = L$ , $\overline{LB} = L$ or $\overline{UB} = L$ )



**$\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{LB}$ ,  $\overline{UB}$  Controlled Read ( $\overline{WE} = H$ )**

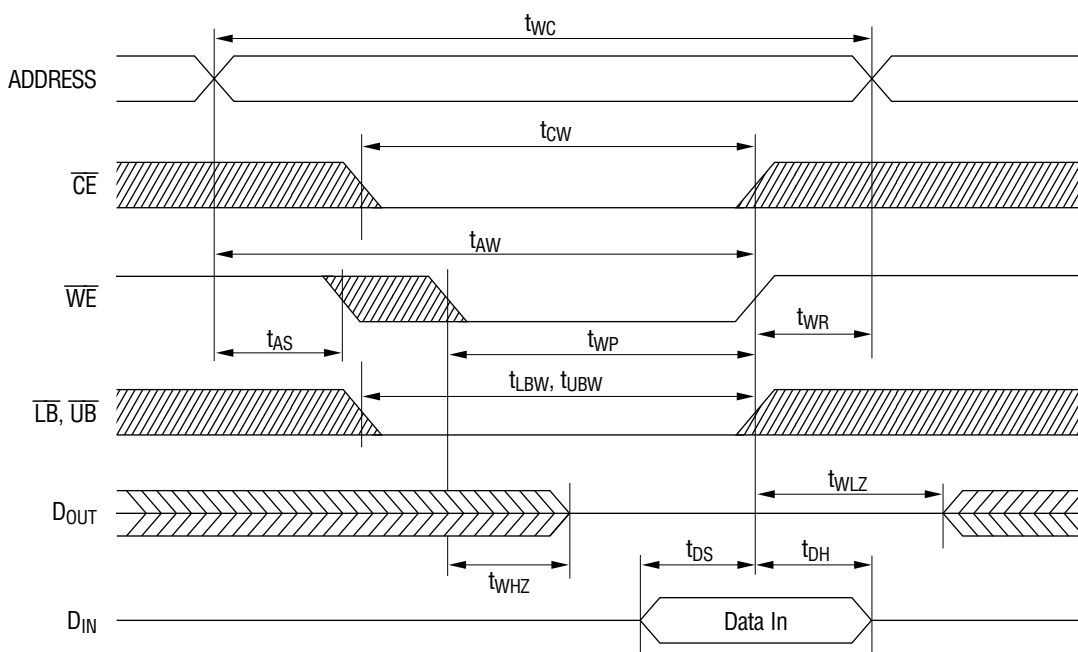


- Notes :
1. A read cycle occurs during the overlap of  $\overline{CE} = "L"$ ,  $\overline{OE} = "L"$ ,  $\overline{LB} = "L"$  (or  $\overline{UB} = "L"$ ) and  $\overline{WE} = "H"$ .
  2.  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{LBHZ}$  and  $t_{UBHZ}$  are specified by the time when DATA is floating, not defined by the output level.

## Write Cycle

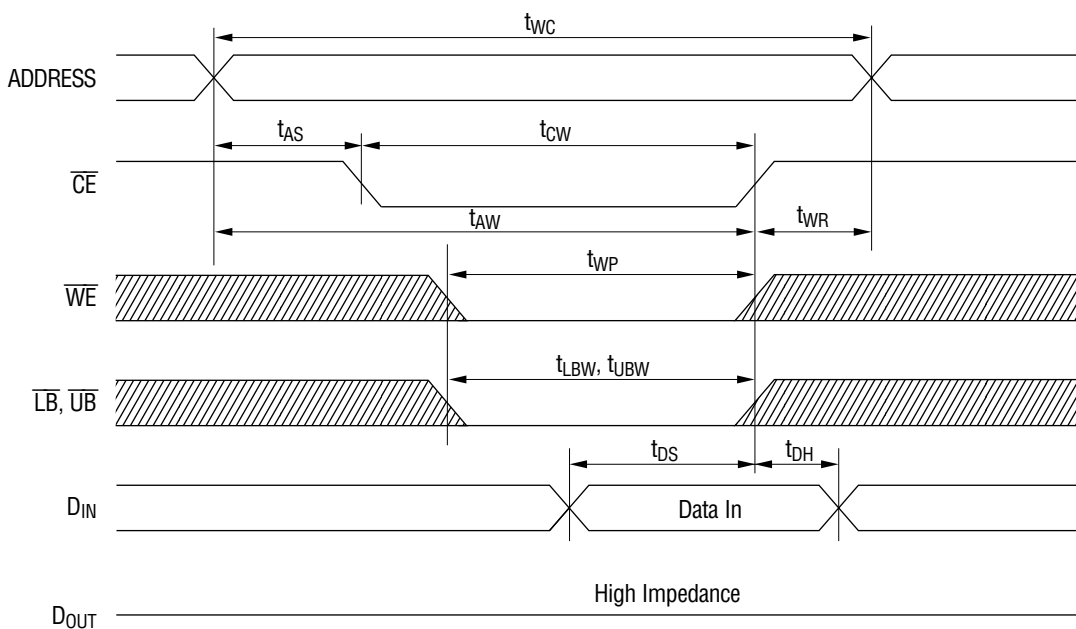
(V<sub>CC</sub> = 3.3 V ±0.3 V, T<sub>a</sub> = 0°C to 70°C)

| Parameter                                         | Symbol                              | MSM521216-20 |      | MSM521216-25 |      | MSM521216-30 |      | Unit |
|---------------------------------------------------|-------------------------------------|--------------|------|--------------|------|--------------|------|------|
|                                                   |                                     | Min.         | Max. | Min.         | Max. | Min.         | Max. |      |
| Write Cycle Time                                  | t <sub>WC</sub>                     | 20           | —    | 25           | —    | 30           | —    | ns   |
| Address Setup Time                                | t <sub>AS</sub>                     | 0            | —    | 0            | —    | 0            | —    | ns   |
| Write Pulse Width                                 | t <sub>WP</sub>                     | 15           | —    | 20           | —    | 25           | —    | ns   |
| Write Recovery Time                               | t <sub>WR</sub>                     | 0            | —    | 0            | —    | 0            | —    | ns   |
| Data Setup Time                                   | t <sub>DS</sub>                     | 10           | —    | 12           | —    | 14           | —    | ns   |
| Data Hold Time                                    | t <sub>DH</sub>                     | 0            | —    | 0            | —    | 0            | —    | ns   |
| $\overline{WE}$ to Output in High-Z               | t <sub>WHZ</sub>                    | —            | 8    | —            | 10   | —            | 12   | ns   |
| $\overline{CE}$ to End of Write                   | t <sub>CW</sub>                     | 15           | —    | 20           | —    | 25           | —    | ns   |
| Address Valid to End of Write                     | t <sub>AW</sub>                     | 15           | —    | 20           | —    | 25           | —    | ns   |
| $\overline{LB}$ , $\overline{UB}$ to End of Write | t <sub>LBW</sub> , t <sub>UBW</sub> | 15           | —    | 20           | —    | 25           | —    | ns   |
| Output Active from End of Write                   | t <sub>WLZ</sub>                    | 0            | —    | 0            | —    | 0            | —    | ns   |

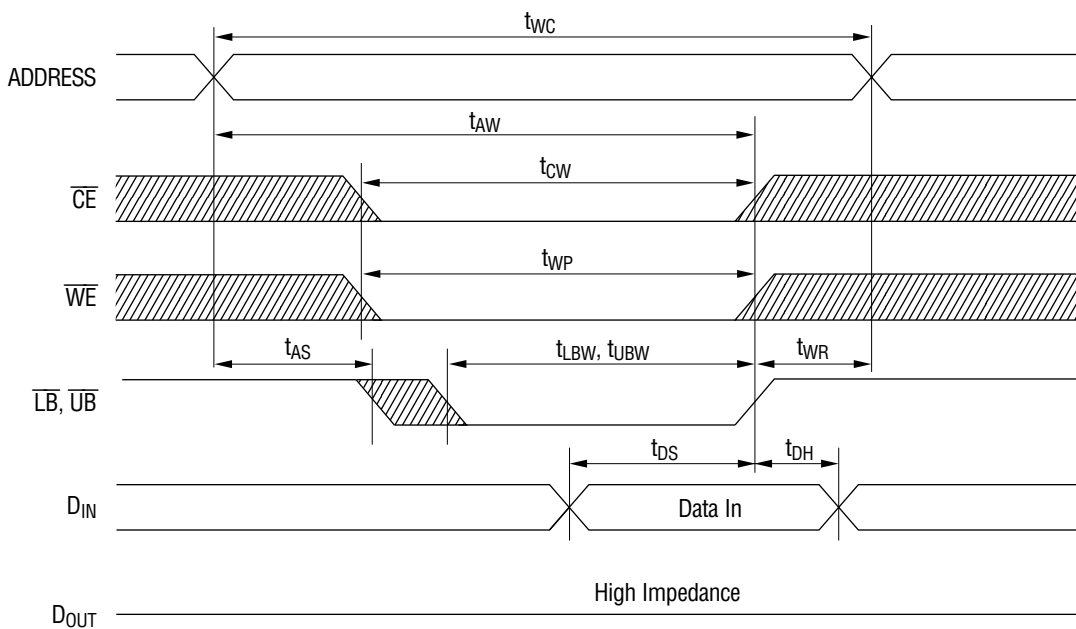
 $\overline{WE}$  Controlled Write ( $\overline{OE} = L$ )



### $\overline{\text{CE}}$ Controlled Write ( $\overline{\text{OE}} = \text{H}$ )



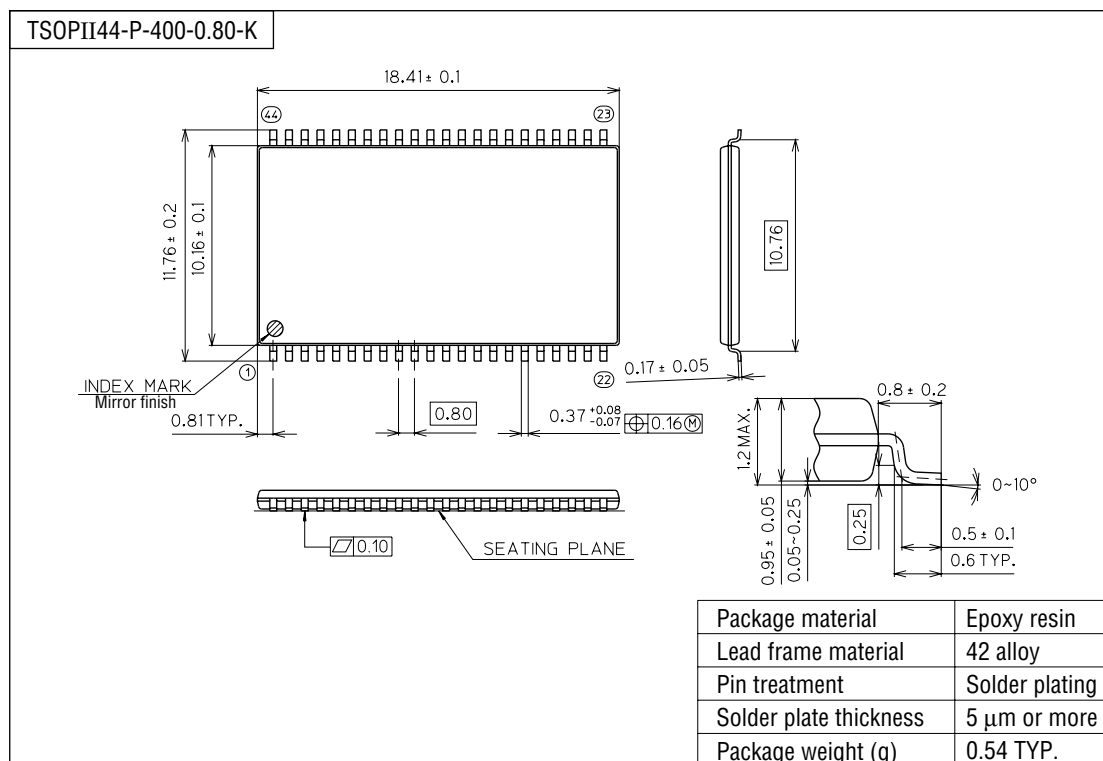
### $\overline{\text{LB}}, \overline{\text{UB}}$ Controlled Write ( $\overline{\text{OE}} = \text{H}$ )



- Notes:
1. A write cycle occurs during the overlap of  $\overline{CE} = "L"$ ,  $\overline{WE} = "L"$  and  $\overline{LB} = "L"$  (or  $\overline{UB} = "L"$ ).
  2.  $\overline{OE}$  may be either of "H" or "L" in the write cycle.
  3.  $t_{AS}$  is specified from  $\overline{CE} = "L"$ ,  $\overline{WE} = "L"$  or  $\overline{LB} = "L"$  (or  $\overline{UB} = "L"$ ) whichever occurs last.
  4.  $t_{WP}$  is an overlap time of  $\overline{CE} = "L"$ ,  $\overline{WE} = "L"$  and  $\overline{LB} = "L"$  (or  $\overline{UB} = "L"$ ).
  5.  $t_{WR}$ ,  $t_{DS}$  and  $t_{DH}$  are specified from  $\overline{CE} = "H"$ ,  $\overline{WE} = "H"$  or  $\overline{LB} = "H"$  (or  $\overline{UB} = "H"$ ) whichever occurs first.
  6.  $t_{WHZ}$  is specified by the time when DATA output is floating, not defined by the output level.
  7. When I/O pins are in the output mode, don't apply the inverted input signal to the output pins.

## PACKAGE DIMENSIONS

(Unit : mm)



## Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).